Sub-Micron InGaAs Esaki Diodes With Record High Peak Current Density

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Tunneling field effect transistors (TFET), which are gated Esaki tunnel junctions (ETD) operating in the Zener regime, have theoretically been predicted to operate with ultra low power supplies (<0.5 V) and steep subthreshold slopes (<60 mV/dec) [1, 2]. However, the majority of these projections have been made based on uncalibrated TCAD modeling. To this end, the authors experimentally demonstrate a pair of InGaAs tunnel diodes with the highest peak current densities ($J_P = I_P$/Area) ever reported for tunnel diodes (975 kA/cm^2 or 9.75 mA/μm^2) [3-5]. Other groups have attempted to experimentally demonstrate these structures, but were limited by a combination of output current and series resistance [6]. The key innovation in this study was a process for testing deep submicron Esaki diodes [7], which mitigates these factors.

Two latticed matched InGaAs ETDs, TD1 (Fig. 1a) and TD2 (Fig. 1b), were grown on separate InP substrates via molecular beam epitaxy and metalorganic molecular beam epitaxy, respectively. Both devices have the same silicon n-type doping concentration of 5×10^{19} cm^{-3} and a 3 nm undoped spacer. However, TD1 has a larger p-type doping of 10^{20} cm^{-3} compared to 5×10^{19} cm^{-3} for TD2. Electron-beam (E-beam) lithography was used to pattern a bi-layer resist stack (PMMA/LOR 5A) for lift-off of Au/Zn/Au (20 nm/20 nm/160 nm) contacts. The diodes were then wet etched with a Citric Acid:H_2O:H_2O_2 mixture, using the contacts as a self-aligned etch mask, Fig. 2. Contact areas and wet-etch undercuts were systematically studied via extensive SEM microscopy in order to accurately estimate junction areas. Then, each sample was planarized with benzocyclobutane (BCB), which is used as an inter-layer dielectric (ILD). The BCB is etched back until the Au/Zn/Au contacts were exposed. Finally, large (20 μm radii) Au pads were aligned on top of the exposed contacts via a second E-beam lithography.

The I-V characteristics for both devices, Fig. 3, exhibit peak-to-valley current ratios (PVCR) up to 3.4 and 6.8 for TD1 and TD2, respectively. It is evident from Fig. 4 that I_P is linearly related to junction area. However, the areas of the smallest devices needed more characterization due process and lithography variation. Therefore, they deviate off of this trend. As a result, the authors speculate that these ETDs are not dominated by surface leakage currents. Fig. 5 presents a J_P histogram for over 200 measured devices for each structure. From the Gaussian fit to each data set J_P is 975 kA/cm^2 and 210 kA/cm^2 for TD1 and TD2, respectively. J_P of TD2 is comparable to the highest Si/SiGe TD current density [5]. However, TD1 has the largest experimentally observed J_P of any tunnel diode [3] as seen in Table 1.

Parasitic resistance can be broken into two types of serially connected resistors; a constant resistance (R_{Const}) and an area dependent resistance ($R_{Area} = \rho_A$/Area). TD1 has a larger R_{Const} of 7.8 Ω compared to 1.6 Ω for TD2, which was extracted from the slope of the best line fit to peak voltage (V_P) vs. I_P plot, Fig. 6. To extract specific resistivity (ρ_A) - which consists of all area dependent resistances including those associated with the contacts, device mesa, and device structure - a voltage (V_I) for each curve is interpolated for a constant current (I_C). This is done for several forward (pre-V_P) and reverse bias currents, resulting in inverse constant current curves ($1/V_I$ vs. Area), Fig. 7. The slope of each line (m) is then used in a second plot of m^{-1} vs. I_C, Fig. 8. Finally, ρ_A is extracted from the slope of this line and is found to be 76.2 Ω-μm^2 and 41.9 Ω-μm^2 for TD1 and TD2, respectively.

In conclusion, the authors have reported the highest current density ever achieved for a tunnel junction with a J_P of 975 kA/cm^2. Furthermore, reducing the p-type doping in TD1 by half (TD2) reduced J_P by 78.5% and doubled the PVCR. These results may be used to calibrate band-to-band tunneling models. The fabrication of sub-micron devices, enabled by E-beam lithography and BCB as an ILD, was key to limiting output current and series resistance. Finally, specific resistivities have been extracted which may be used to compare the use of tunnel junctions as contacts; applications include source/drain regrowth and multi-junction solar cells.

[1] Z. Qin, *et al.*, *IEEE Elec. Dev. Lett.*, vol. 27, pp. 297-300, 2006. [2] S. Mookerjea, *et al., 2009 IEDM Tech. Dig.*, 2009, pp. 949-951. [3] T. P. E. Broekaert, *et al., 1989 IEDM Tech. Dig.*, 1989, pp. 559-562. [4] N. Jin, *et al., Appl. Phys. Lett.*, vol. 83, pp. 3308-3310, 2003. [5] S. Y. Chung, *et al., IEEE Elec. Dev. Lett.*, vol. 27, pp. 364-367, 2006. [6] S. Kabeer, *et al., Proc. 2009 ISDRS*, 2009, pp. 1-2. [7] D. J. Pawlik, *et al., Proc. 2009 ISDRS*, 2009, pp. 1-2.

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(a)

50 nm	$In_{0.53}Ga_{0.47}As$	$p = 10^{19}$ cm^{-3}
10 nm	$In_{0.53}Ga_{0.47}As$	$p = 10^{20}$ cm^{-3}
3 nm	$In_{0.53}Ga_{0.47}As$	undoped
10 nm	$In_{0.53}Ga_{0.47}As$	$n = 5\times10^{19}$ cm^{-3}
300 nm	$In_{0.53}Ga_{0.47}As$	$n = 10^{19}$ cm^{-3}
S. I. InP		

(b)

60 nm	$In_{0.53}Ga_{0.47}As$	$p = 5\times10^{19}$ cm^{-3}
3 nm	$In_{0.53}Ga_{0.47}As$	undoped
60 nm	$In_{0.53}Ga_{0.47}As$	$n = 5\times10^{19}$ cm^{-3}
10 nm	InP	$n = 10^{19}$ cm^{-3}
200 nm	$In_{0.53}Ga_{0.47}As$	$n = 3\times10^{19}$ cm^{-3}
50 nm	InP	$n = 10^{19}$ cm^{-3}
n^{++} InP		

Fig. 1. Schematic diagrams of structures (a) TD1 and (b) TD2.

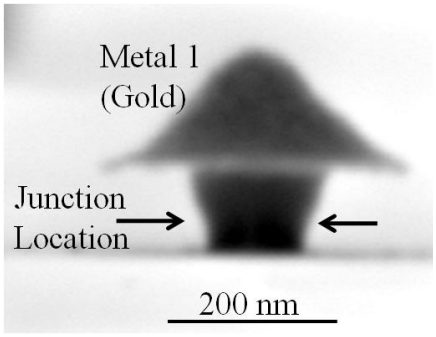

Fig. 2. SEM micrograph cross-section of sub-micron ETD (TD2) after mesa isolation etch. The metallurgical tunnel junction has been highlighted by the dopant dependent etch.

Table I: Comparison of high current density tunnel diodes with TD1 and TD2 of this work. TD1 is a world record J_P.

Study	Structure	J_P (kA/cm^2)	MAX PVCR
Broekaert [3]	InGaAs/AlAs RTD	450	3
Cohen [4]	InGaAs Esaki	93.2	3.8
Chung [6]	Si/SiGe Esaki	218	1.5
This Work TD2	InGaAs Esaki	210	6.8
This Work TD1	InGaAs Esaki	975	3.4

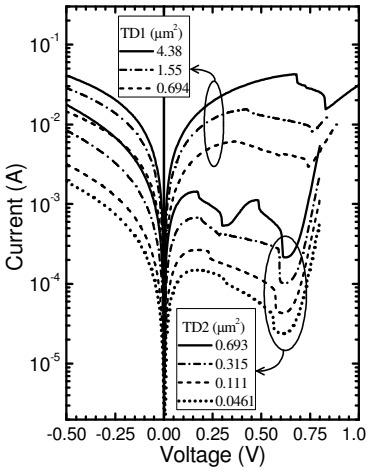

Fig. 3. I-V curves which show that TD1 has a larger current density and series resistance compared to TD2.

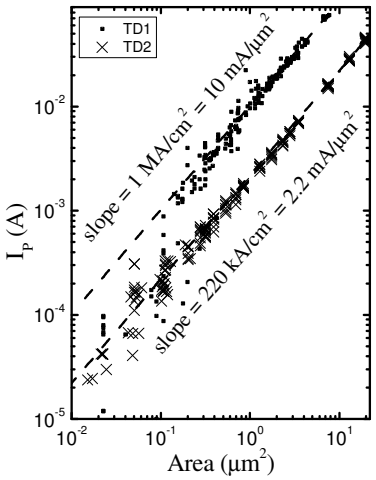

Fig. 4. Linear relationship between I_P and area indicates that TD1 and TD2 are not dominated by surface affects.

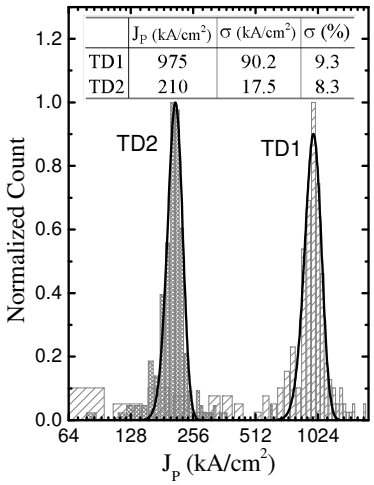

Fig. 5. J_P histograms for TD1 and TD2 with Gaussian fits used to calculate J_P and std. dev. (σ).

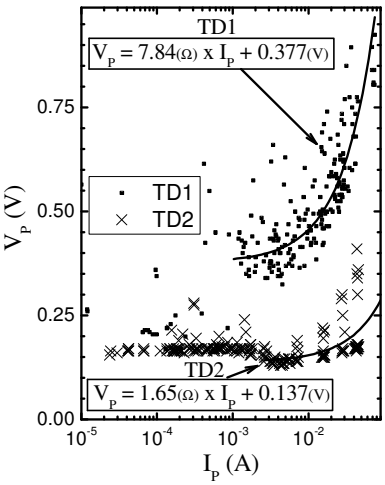

Fig. 6. V_P vs. I_P for TD1 and TD2. Linear fits are used to extract R_{Const}.

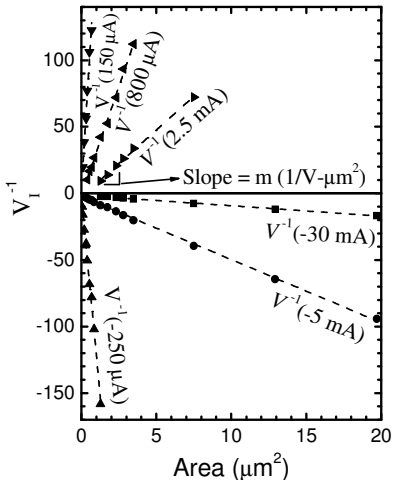

Fig. 7. Inverse constant current curves for TD2. Slopes (m) are used for ρ_A extraction seen in Fig. 8.

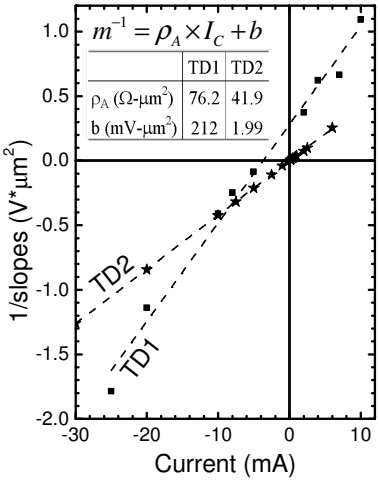

Fig. 8. Extracted specific resistivity for TD1 and TD2