Implications of Record Peak Current Density $In_{0.53}Ga_{0.47}As$ Esaki Tunnel Diode on Tunnel FET Logic Applications

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Inter-band tunnel field effect transistors (TFETs) have recently gained a lot of interest because of their ability to eliminate the 60mV/dec sub-threshold slope (STS) limitation in MOSFET. This can result in higher I_{ON}-I_{OFF} ratio over a reduced gate voltage range, thus predicting TFETs superior for low supply voltage ($V_{DD} \leq 0.5V$) operation. Unlike Si and Ge, III-V semiconductors like $In_{0.53}Ga_{0.47}As$ have smaller tunneling barrier and tunnelling mass, thus making them a design choice to eliminate drive current (I_{ON}) limitations in TFETs [1-2]. In this work, (i) we present the experimental demonstration of record peak current density (J_{PEAK}) $In_{0.53}Ga_{0.47}As$ Esaki tunnel diode, formed using MBE grown in-situ doped epitaxial layers [4]. (ii) Using a non-local tunneling model in Sentaurus device simulator [3], the measured current-voltage characteristics (J-V) is modeled and the model parameters are calibrated. (iii) Novel $In_{0.53}Ga_{0.47}As$ ultra thin body (7nm)-double gate-TFET (UTB-DG-TFET) design to boost I_{ON} is discussed using the calibrated non-local tunneling model. (iv) Pulse transient response of the novel $In_{0.53}Ga_{0.47}As$ TFET inverter is presented and compared with Si based MOSFET inverters at a supply voltage of 0.5V.

Fig. 1(a) shows the schematic of the fabricated Esaki tunnel diode. E-beam lithography was used to pattern and form sub-micron radius tunnel diodes. BCB (Benzo-Cyclo-Butane) was then spin coated for planarization and to form an inter-layer dielectric [4]. Fig. 1(b) shows representative Scanning Electron Micrograph (SEM) image of the fabricated device taken before BCB planarization, with an effective junction radius of 771 nm. Fig. 2 shows the measured and modeled J-V at room temperature. J_{PEAK} is 0.975MA/cm^2 with a peak to valley current ratio (PVCR) of 1.94. This is the highest value of J_{PEAK} ever achieved amongst Esaki diodes on any chosen substrate as shown in Fig. 3. For numerical modeling, a non-local band-to-band tunneling model [3] was used with the following model parameters and values: gc=gv=0.1 and mc=0.07m$_o$, mv=0.05m$_o$. Abrupt, uniform and active p and n type junction doping of 8x10^{19}/cm^3 and 4x10^{19}/cm^3 were used. Fig 4(a) shows components of the modeled characteristics. Net series resistance (R_S) of 20Ω was used to match the measured forward and reverse (Zener) side of the J-V. The agreement between numerical band-to-band tunneling (J_{BTBT}) component and analytical J_{BTBT}[5] validates calibration. Fig. 4(b) shows the Zener side characteristic with and without R_S. At -0.5V, the intrinsic current density is greater than 10 MA/cm^2 which is again a record value and has important implications for $In_{0.53}Ga_{0.47}As$ TFET design. Post valley excess current was modeled using gap state assisted tunneling [6].

Fig. 5 shows novel $In_{0.53}Ga_{0.47}As$ UTB-DG-TFET design with 32nm gate length (L_G) and 2.5nm high K (HfO_2) gate dielectric (EOT=0.5nm). Three different source channel configurations are considered for analysis: (a) i-TFET with an intrinsic $In_{0.53}Ga_{0.47}As$ channel. (b) δ-TFET with a 2nm thin heavily doped n-type (δ-N+) layer adjoining the source [7] and finally, (c) δ-HTFET with a thin (3nm) layer of narrow band-gap material (p+-InAs) at the tunneling junction (Hetero-junction) with an adjoining δ-N+ layer as used for δ-TFET. For 3nm InAs, quantized band-gap of 0.5eV and conduction band offset of 0.1eV (Type-I) with $In_{0.53}Ga_{0.47}As$ were considered. Fig. 6 shows transfer characteristics (I_D-V_{GS}) for each of them along with same EOT single gate intrinsic channel $In_{0.53}Ga_{0.47}As$ tunnel FET (SG-i-TFET) [2] and Si MOSFETs with low and high threshold voltages (V_T)**.** Clearly, tunnel FETs have significant I_{ON} advantage at lower gate voltages due to their inherent steep STS. Table (I) summarizes I_{ON} and I_{ON}/I_{OFF} ratio. I_{ON} in i-TFET and SG-i-TFET is lower than high V_T MOSFET, while, δ-TFET and δ-HTFET show higher I_{ON} for the entire gate voltage range. The primary reason for current enhancements over i-TFET can be inferred from the band-diagrams in Fig. 7. Presence of a depleted δ-N+ layer reduces tunneling width and presence of lower band-gap InAs reduces tunneling barrier. With an additive effect of both, δ-HTFET shows maximum I_{ON}.

Fig. 8 compares unloaded inverter pulse transient response with a rise time of 0.2 ps. Fall delay (τ_{INT}), switching power (P_{SW}) at 1GHz frequency and leakage power (P_{LEAK}) are listed in Table-I. It can be inferred from the table that TFETs have a 1000X and 5x10^6 X lower P_{LEAK} compared to high and low $\mathbf{V_T}$ Si MOSFETs respectively. Most noticeably, $In_{0.53}Ga_{0.47}As$ based δ-HTFET exhibits the lowest τ_{INT} and P_{SW} values, the primary reasons being efficient tunneling at the source-channel junction (reduced tunneling barrier height and width as discussed before) and a reduced effective output capacitance resulting from lower density of states in the channel [8]. Thus UTB-DG δ-HTFET is a promising candidate for the replacement of Silicon CMOS transistors in low power and high performance logic applications.

[1] S. Mookerjea et al., *66th Dev. Res. Conference Digest*, 47, (2008). **[2]** S. Mookerjea et al., *IEEE IEDM Tech. Dig.,* Dec. 2009. **[3]** Sentaurus Users Guide, Ver. Z-2007.3 **[4]** D. J. Pawlik, et al., *Proc. 2009 ISDRS*, pp. 1-2, 2009,. **[5]** H. Flietner, *Physica Status Solidi (B),* 54, 201, Feb 2006. **[6]** Chynoweth et al., *Phys. Rev.,* 121, pp. 684-694, Feb. 1961. **[7]** V. Nagavarapu et al., *IEEE Trans. Elect. Dev*., 55, 1013, April 2008 **[8]** S. Mookerjea et al., *IEEE Trans. Elect. Dev.*, 56, 2092, Sept. 2008.

(a)

500nm Au (Level 2)		
BCB	200nm Au (Level 1)	BCB
50nm P+ C-1x10^19 cm^-3 $In_{0.53}Ga_{0.47}As$		
10nm P++ C-1x10^20 cm^-3 $In_{0.53}Ga_{0.47}As$		
3 nm Un-doped $In_{0.53}Ga_{0.47}As$ spacer		
10nm N++ Si-5x10^19 cm^-3 $In_{0.53}Ga_{0.47}As$		
300 nm N+ Si-1x10^19 cm^-3 $In_{0.53}Ga_{0.47}As$		
S.I. InP		

Fig. 1 (a)-Fabricated Esaki diode structure (b) Representative SEM image of the fabricated device before BCB planarization.

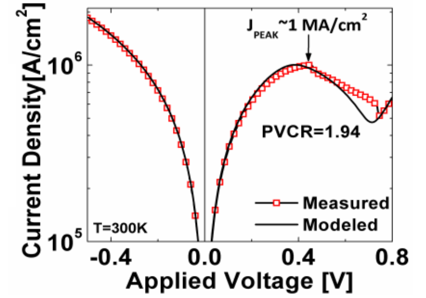


Fig. 2-Measured and Modeled J-V

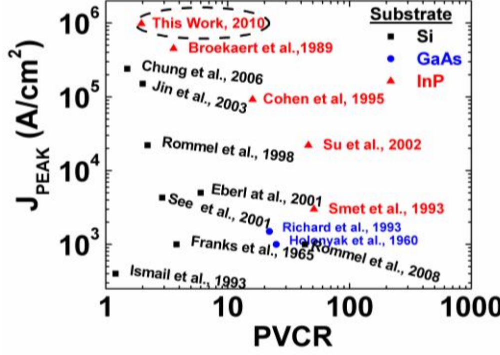
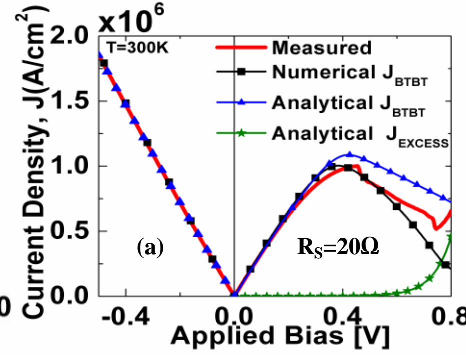


Fig. 3-Record J_{PEAK} shown amongst high J_{PEAK} values reported till date on different substrates.



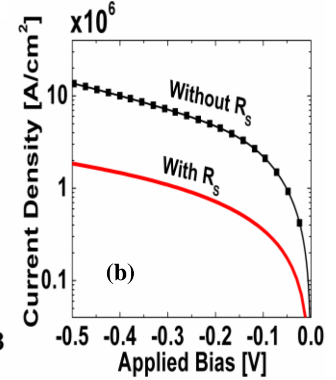


Fig. 4(a)-Numerically modeled J_{BTBT} components. Also shown analytical model for comparison[5]. **(b)** Zener side J_{BTBT} with and without series resistance (R_S).

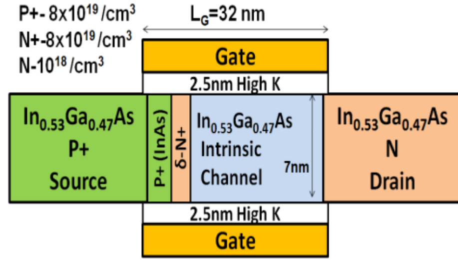


Fig 5-UTB-DG-TFET structure (δ-HTFET)

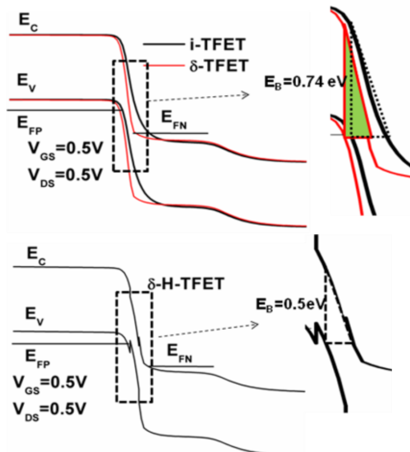


Fig. 7-Band-diagrams at V_{DS}=V_{GS}=0.5V. Compared to i-TFET, δ-TFET has lower tunneling width while δ-HTFET has lower tunneling width and barrier height.

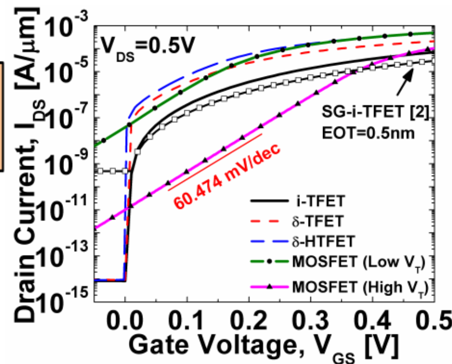


Fig. 6-Simulated transfer characteristics for the three different UTB-DG-TFET structures, SG-i-TFET[2] and Si MOSFETs with high and low V_T (as discussed in text) at V_{DS}=0.5V.

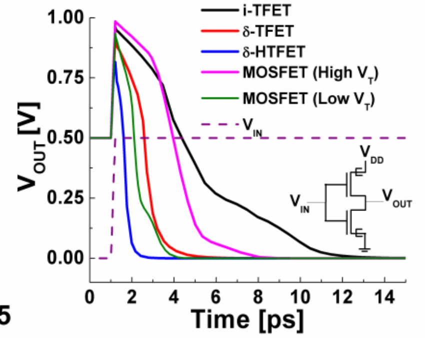


Fig. 8-Un-loaded transient response of UTB-DG-TFET and Si-MOSFET inverters. (Input pulse rise time=0.2ps)

Table I- Transfer characteristics and inverter transient response chart for $In_{0.53}Ga_{0.47}As$ UTB-DG-TFET and Si-MOSFET.

Type	I_{ON} - μA/μm	I_{ON}/I_{OFF}	τ_{INT} - psec	P_{SW} - μW/μm	P_{LEAK}- pW/μm
SG-i-TFET[2]	30	$6.25x10^4$	-	-	-
i-TFET	71	$8x10^9$	5.13	0.92	0.0022
δ-TFET	211	$2.4x10^{10}$	1.78	0.56	0.0022
δ-HTFET	493	$5.5x10^{10}$	0.63	0.42	0.0022
Si-MOSFET (Low V_T)	493	$4.93x10^6$	1.28	0.86	12500
Si-MOSFET (High V_T)	104.67	$2.1x10^3$	3.15	0.78	2.5