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Numerical study of reduced contact resistance via nanoscale topography at metal/semiconductor interfaces

B P Downey[1], S Datta[2] and S E Mohney[1,3]

[1] Department of Materials Science and Engineering, The Pennsylvania State University, University Park, PA 16802, USA
[2] Department of Electrical Engineering, The Pennsylvania State University, University Park, PA 16802, USA

E-mail: mohney@ems.psu.edu

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Abstract
Reduction in contact size via scaling leads to an increase in parasitic contact resistance, which can be a limiting factor in aggressively scaled high-frequency transistors. Using numerical modelling, we predict that nanoscale topography at the metal/semiconductor interface can reduce the effective specific contact resistance by 25% or more using features 10 nm or less in width, even for doping densities as high as 10^{20} cm^{-3}. Previous studies have shown that these features cause an increase in tunnelling current for lightly doped semiconductors. However, we have found that for heavy doping or low barrier heights, the main factor reducing contact resistance is increased interfacial area.

1. Introduction

One limiting factor for high-frequency transistor performance is the increase in parasitic contact resistance due to the reduction in ohmic contact size as device dimensions continue to scale. This is not only true in conventional Si logic transistors [1], but also in high-speed compound semiconductor technology [2]. Ideally, low resistance ohmic contacts can be produced by minimizing the barrier height at the metal/semiconductor interface through appropriate choice of metal work function, along with heavily doping the semiconductor to reduce the barrier width [3]. However, Fermi level pinning [3] and limitations in doping concentration due to solid solubility limits can inhibit the reduction of ρ_c, or specific contact resistance, which relates contact area to resistance. An alternate approach to reducing ρ_c has been shown for lightly doped n-GaN [4]. In this study, nanoscale features were intentionally etched into the semiconductor surface, using a porous alumina etch mask, creating an array of pits prior to metal deposition. The nanoscale features cause an increase in tunnelling current due to a decreased barrier thickness, and therefore, an increase in electric field and tunnelling probability [5, 6]. However, significant increases in tunnelling current occur only as the feature curvature approaches the barrier thickness, or depletion width. In heavily doped semiconductors, the depletion width may be on the order of only nanometres, making an increase in tunnelling current difficult to achieve. However, an increase in metal/semiconductor interfacial area may still lead to a smaller contact resistance. In this study, we examine the effect of nanometre scale features on the reduction in contact resistance for heavily doped semiconductors using a numerical modelling approach. The influence of feature size, feature spacing, doping density, barrier height and contact size on the reduction of ρ_c will be presented. The reduced ρ_c is actually an effective ρ_c as it will be determined from the nominal area of the contact opening, not the actual metal/semiconductor area accounting for the additional features at the metal/semiconductor interface.

2. Device structure and simulation

Two-dimensional (2D) numerical simulations were performed using the Sentaurus TCAD software [7] by Synopsys, Inc. A three-dimensional rendering of the 2D structure used for the simulations is shown in figure 1. The structure consists of a 300 nm long by 300 nm deep semiconductor layer

[3] Author to whom any correspondence should be addressed.

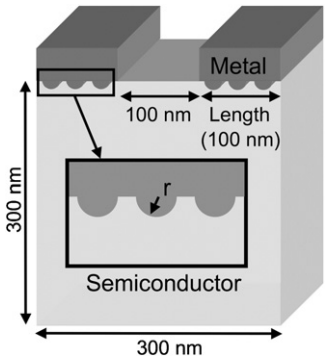

Figure 1. Three-dimensional depiction of the structure used for the simulations, showing the circular features at the metal-semiconductor interface. In three dimensions, the circular features become rods running the width of the contact.

with two 100 nm long metal contacts on the top and a 100 nm gap separating the contacts. Circular metal features, cylinders in three dimensions, were used to examine the effect of nanotopography on contact resistance. The features were varied in size, number and spacing and placed at the metal/semiconductor interface as shown in figure 1. The features allow for a constant radius of curvature and provide a feature width of $2r$ and a feature depth of r. Due to the small depletion width for heavily doped semiconductors, the feature radius was chosen to be 5, 2 or 1 nm.

The device is simulated by applying a dc bias across the top of the metal contacts, leading to lateral current flow through the semiconductor. Bulk semiconductor carrier transport was modelled by self-consistently solving Poisson's equation and the electron continuity equation using drift-diffusion physics. The nonlocal tunnelling model in Sentaurus, from Ieong *et al* [8], was used to simulate carrier transport across the metal/semiconductor interface. A current–voltage (I–V) plot was used to determine the resistance of the contacts (the bulk semiconductor resistance was obtained in a separate simulation), and an effective ρ_c was calculated. This approach is valid since the observed transfer length of the contact, or the measure of current crowding at the front of the contact for lateral current flow, was larger than the contact length.

3. Results and discussion

Although this technique is applicable to many semiconductors, n-type Si and $In_{0.53}Ga_{0.47}As$ are used as examples here. The values of ρ_c determined for the planar contact geometry (true ρ_c) was in the low 10^{-8} to low 10^{-7} Ω cm^2 range, which is on the order of ρ_c values published for these semiconductors [9, 10]. While the addition of multiple features provided a maximum reduction in effective ρ_c of 35 or 45% for 5 or 2 nm features, it is essential to understand how isolated individual features affect contact resistance. The plots in figures 2(a) and (b) show the per cent decrease in effective ρ_c, compared to contacts with no features (planar), for the addition of one feature in the middle of each 100 nm contact as a function of feature size. The plot in figure 2(a) illustrates that for a constant barrier height, 0.365 eV for Si and 0.2 eV for

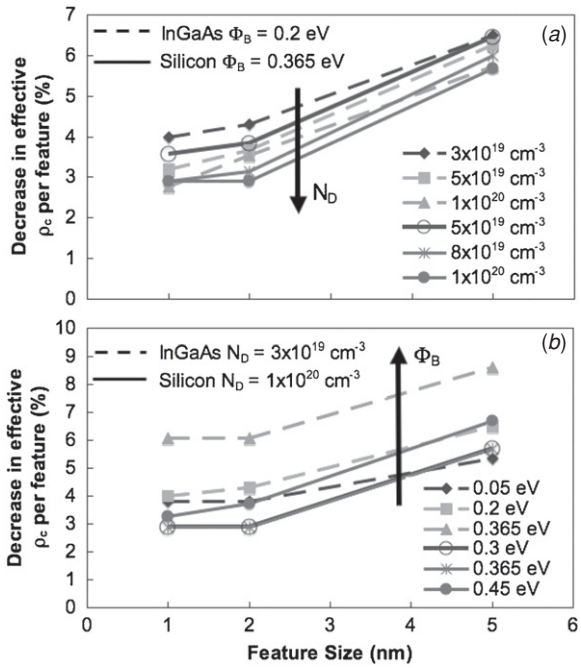

Figure 2. The reduction in effective ρ_c at (a) constant barrier height and (b) constant doping for a 5, 2 or 1 nm feature on each 100 nm contact.

InGaAs, as the doping density increases, the reduction in effective ρ_c decreases for a given feature size. In contrast, at a constant doping density, 1×10^{20} cm^{-3} for Si and 3×10^{19} cm^{-3} for InGaAs, as the barrier height increases, a larger reduction in effective ρ_c is shown. It should be noted that the *normalized* decrease in effective ρ_c relative to the planar geometry is greater for higher Schottky barrier heights. However, a lower barrier height is still preferable and leads to a smaller contact resistance when identical geometries are compared. A reduction between 5 and 9% per feature is observed for 5 nm features, while the reduction is less than 6% for 1 nm features. These trends are explained by plotting the tunnelling rate or electric field, which is proportional to tunnelling current, as a function of position in the structure (not shown). As expected from theory, a larger increase in tunnelling occurs around the curved features compared to the planar parts of the contact, particularly as the feature size decreases, doping density decreases, or barrier height increases. There is also a larger increase in tunnelling for the negatively biased contact due to the increase in the depletion width to feature size ratio.

The reduction in ρ_c due to tunnelling is plotted in figures 3(a) and (b) for constant barrier height and constant doping. These plots are similar to the ones shown in figure 2, except that the reduction in contact resistance due to increased interfacial area is excluded by taking into account the actual increased interfacial area when calculating ρ_c. In this case, any further reduction must be from increased tunnelling. The plots show that the majority of the reduction in effective ρ_c is due to increased interfacial area for higher doping densities, lower barriers and larger features.

The plots in figures 4(a) and (b) illustrate the reduction in effective ρ_c when multiple, evenly spaced features are

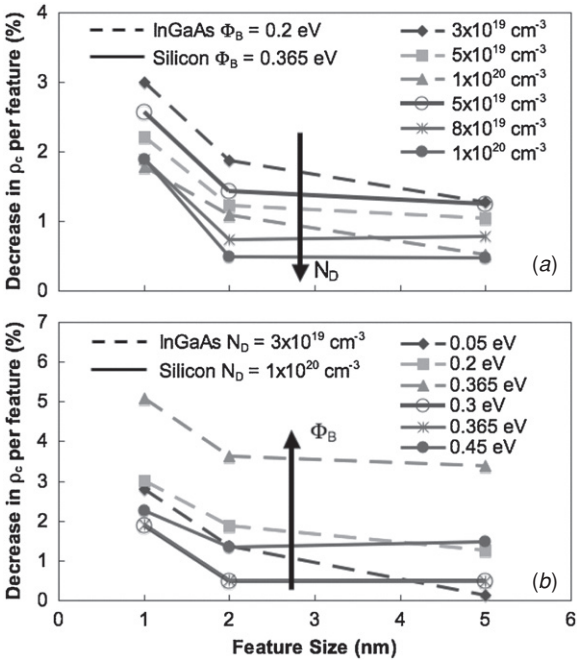

Figure 3. The reduction in ρ_c due to *only* tunnelling at (*a*) constant barrier height and (*b*) constant doping for a 5, 2 or 1 nm feature on each 100 nm contact.

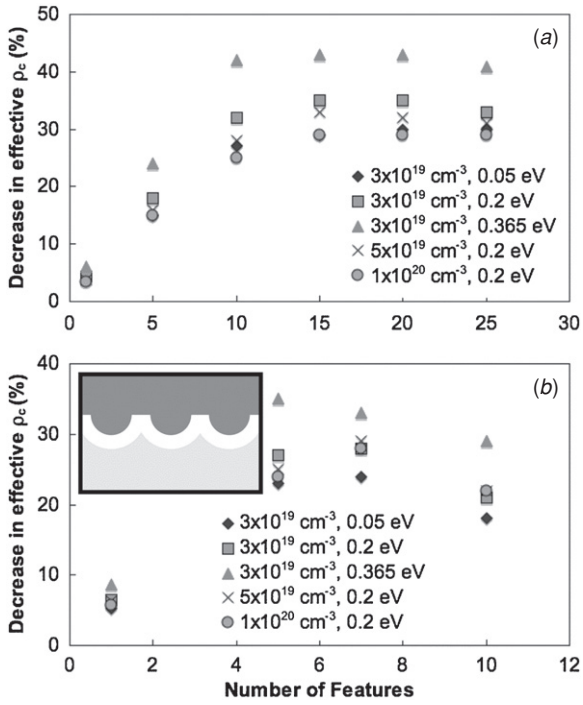

Figure 4. The decrease in effective ρ_c for multiple (*a*) 2 nm and (*b*) 5 nm features per 100 nm contact using n-$In_{0.53}Ga_{0.47}As$ as an example. The inset in (*b*) illustrates how the depletion region (white area around features) can overlap as feature spacing decreases, reducing the effective tunnelling area.

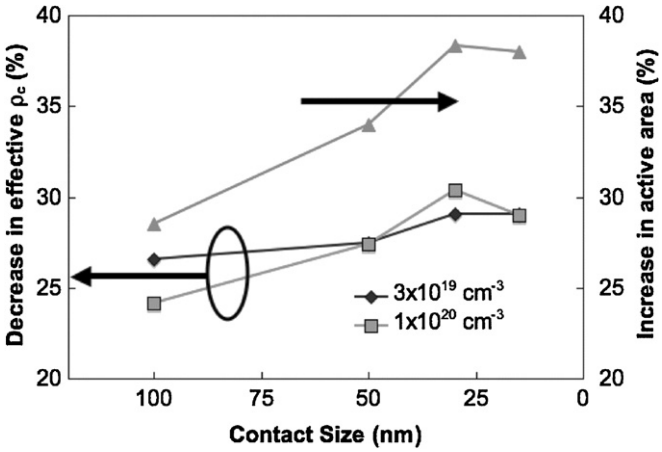

Figure 5. The effect of contact opening size on the decrease in effective ρ_c for 5 nm features spaced 10 nm apart using n-$In_{0.53}Ga_{0.47}As$ with a barrier height of 0.2 eV as an example. The plot also shows the increase in interfacial area for each contact size. The 100, 50, 30 and 15 nm contacts contain 5, 3, 2 and 1 feature per contact, respectively.

added on each 100 nm contact for 2 or 5 nm features using n-type $In_{0.53}Ga_{0.47}As$ as an example. Although initially the decrease appears to be additive per feature, the reduction in ρ_c eventually levels out or even declines, with a maximum decrease in effective ρ_c of between approximately 30 to 45% and 25 to 35% for 2 and 5 nm features, respectively, depending on the doping and barrier height. This trend occurs because as the features become more closely spaced, about two depletion widths apart, the depletion regions between the features start to overlap. The overlap decreases the amount of tunnelling in those areas, decreasing the active area of the contact, as depicted in the inset in figure 4(*b*). The largest decrease is observed for the highest barrier. The difference in effective ρ_c reduction for the other barrier heights, 0.2 and 0.05 eV, is a few per cent. This point is important since Schottky barriers have been shown to be inhomogeneous [11], and the distribution of barrier heights can shift depending on the chemical pretreatment performed prior to metal deposition [12]. A distribution of barrier heights should not significantly alter the prediction of a decrease in effective ρ_c through nanoscale topography, and an overall reduction in the barrier height, as shown in some cases in [12], should be advantageous.

The scalability of this technique to reduce effective ρ_c in future transistors with very small contacts is illustrated for two donor concentrations, 3×10^{19} and 1×10^{20} cm^{-3}, in the plot in figure 5 for n-type $In_{0.53}Ga_{0.47}As$ with a barrier height of 0.2 eV. Using a 5 nm feature size and a constant spacing of 10 nm, the number of features per contact for each contact is 5, 3, 2 and 1 for a 100, 50, 30 and 15 nm contact opening, respectively. In this case, the reduction in effective ρ_c becomes relatively independent of contact size, settling between approximately 25 and 30%. The difference between the two doping concentrations is also minor as increased interfacial area is the main reason for the contact resistance reduction, particularly in the more heavily doped case. For longer contacts where the entire length of the contact is not active, features outside the transfer length will not have much effect on the decrease in contact resistance. Even for the cases with the heaviest doping and lowest barrier, a decrease of 25% was observed for a reasonable feature size of

10 nm wide and 5 nm deep. Increasing the feature depth, and thus the interfacial area, should further decrease the contact resistance. For example, when the same 10 nm wide features were increased to 10 nm in depth, an approximately 50% decrease in effective ρ_c was observed using 100 nm contacts for n-type $In_{0.53}Ga_{0.47}As$ with a barrier height of 0.2 eV and a doping density of 1×10^{20} cm^{-3}.

4. Conclusion

In conclusion, we have shown, through numerical modelling, that the addition of nanoscale features at the metal/semiconductor interface can reduce the contact resistance, even for heavily doped semiconductors with low barrier heights. In this case, the increase in interfacial area dominates the reduction in contact resistance, whereas for lower doping or higher barrier heights, the increase in tunnelling is the most important factor. A large increase in tunnelling occurs only when the feature curvature approaches the depletion width. As features become closely spaced, around two depletion widths apart, their depletion regions overlap, decreasing the actual area over which tunnelling occurs. This phenomenon causes a maximum in the reduction of effective ρ_c as a function of the number of features per contact. This technique has the potential to reduce contact resistance, even when semiconductor doping concentration limits have been reached due to solid solubility limits or thermal budget constraints and when surface Fermi level pinning prevents elimination of a finite Schottky barrier. This finding is significant for engineering the nanotopography at the interface between nanoscale contacts and the semiconductor source-drain regions in order to minimize the contact resistance in future high-speed transistors.

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