Small Signal Response of Inversion Layers in High Mobility In_{0.53}Ga_{0.47}As MOSFETs Made with Thin High-к Dielectrics

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Abstract—Ultra-high mobility compound semiconductor-based MOSFETs and quantum-well FETs could enable the next generation of logic transistors operating at low supply voltages since these materials exhibit excellent electron transport properties. While the long channel $In_{0.53}Ga_{0.47}As$ MOSFETs exhibit promising characteristics with unpinned Fermi level at the InGaAs-dielectric interface, the high field channel mobility as well as sub-threshold characteristics needs further improvement. In this work, we present a comprehensive equivalent circuit model that accurately evaluates the experimental small signal response of inversion layers in $In_{0.53}Ga_{0.47}As$ MOSFETs fabricated with LaAlO₃ gate dielectric and enables accurate extraction of the interface state profile, the trap dynamics and the effective channel mobility.

Index Terms—High-k Dielectric, InGaAs, Interface States, Small Signal Admittance Modeling, Split Capacitance Voltage

I. INTRODUCTION

ULTRA-HIGH mobility compound semiconductor-based (e.g. Indium antimonide, Indium arsenide and $In_xGa_{1-x}As$) MOSFETs and quantum-well FETs could enable the next generation of logic transistors operating at low supply voltages since these materials exhibit excellent low-field and high-field electron transport properties [1]-[3]. Effective channel mobility as a function of the transverse effective electric field or inversion carrier density is an important metric for characterizing the performance of $In_{0.53}Ga_{0.47}As$ based MOSFETs since it not only affects the long channel MOSFET performance directly but also determines indirectly the short channel MOSFET performance in the non ballistic regime by influencing the source side injection velocity [4]. The split C-

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V measurement of the MOSFET inversion capacitance is the standard technique of extracting the effective channel mobility of MOSFETs, which involves direct estimation of the mobile inversion charge density (N_{inv}) through the gate to channel capacitance (C_{gc}) as a function of the gate to source voltage (V_g) as given by

$$Q_{inv} = \int_{ac}^{V_g} C_{gc}(V) dV.$$
(1)

While this method is reliable and highly accurate for most Silicon based MOSFETs including the high-k/metal-gate Si MOSFETs, it is less straight forward in the case of In_{0.53}Ga_{0.47}As MOSFETs. In InGaAs-based MOSFETs, the complex nature of the semiconductor-dielectric interface with relatively high density of interface states, D_{it} , can exhibit a capacitance, C_{it} , that contributes significantly to the measured C_{gc} , even in inversion leading to an over estimation of extracted Ninv. This can lead to incorrect evaluation of the effective channel mobility. In_{0.53}Ga_{0.47}As and high-κ dielectric interfaces are known to possess interface defects. Although the exact origin of the defects is still under debate there is evidence that compound semiconductors exhibit interface states that arise from the native defects, such as Ga or As dangling bonds as well as Ga-Ga or As-As like-atom bonds created by unwanted oxidation during the process of gate dielectric formation. It has been proposed that the As-As anti bonding states due to local excess arsenic created during the gate oxide deposition can lead to a distribution of states that extend into the conduction band [5],[6]. The presence of interface states near the conduction band leads to fast trap response as the Fermi level approaches and enters the conduction band in the inversion regime. Many recent publications of III-V MOSFETs have reported split C-V measurements and the resultant mobility calculated from those measurements [7]–[9]. Frequency dispersion due to C_{it} as well as lumped and distributed resistance effects in the inversion regime has strongly influenced the C_{gc} vs V_g (or C-V) curves resulting in incorrect mobility calculations.

In this paper we will outline a novel technique that self consistently solves the capacitance-voltage (C-V) and conductance-voltage (G-V) measurement data as a function of gate bias and small signal AC frequency to uniquely determine the D_{it} response as well as the true inversion carrier response

for a given voltage. This technique enables us to extract the true inversion capacitance (C_{inv}) as a function of temperature and gate bias in the inversion regime. The impact of parameters such as oxide capacitance, tunnel conductance, fixed series resistance, distributed channel resistance and interface state capacitance and conductance on the extraction of true inversion carrier density is systematically studied using the experimental data. Various methods have been reported in the literature to correct for interface state density. The method proposed by Hinkle et al in [10] requires the low temperature C-V to be free from dispersion due to D_{ii} . The method proposed by Zhu et al in [11] compares the measured C-V data with the simulated ideal C-V to account for the stretch out in the C-V and the output conductance (g_{ds}) characteristics. This method also assumes that the experimental inversion response of the carriers is free from frequency dispersion due to interface states, which may be applicable for Silicon and Germanium based materials where the inversion carrier densities are high due to high density of states (DOS) but not for III-V systems. Martens et al [12] proposed the full conductance technique which is suitable for extracting the interface state density across the entire band gap for any material system. However, Martens' approach requires detecting the exact location of the conductance peak due to interface states, which depends on the measurement AC frequency and the temperature. Also, the technique does not allow direct extraction of the inversion carrier density. Unlike the first two approaches [11], [12], our work does not assume a priori that a low temperature and high frequency C-V data is necessarily free from D_{it} effect. Instead, our technique directly extracts the interface state density, trap time constant and the frequency independent inversion channel capacitance by directly solving an equivalent circuit model from the measured admittance values. Another key difference in our proposed method from the commonly used full conductance technique [12, 13] is that, we do not need information about the peak position in the measured conductance (G_{it}/ω) versus frequency; we rather solve the conductance and the capacitance contributions of D_{it} in a self consistent manner over the entire frequency and voltage range. This allows us to extract the D_{it} distribution over a wider range of energy than given by the peak conductance method for a given frequency range of the impedance measuring instrument at a given temperature. This also allows extraction of the true C_{inv} free from any frequency dispersion. Extracting the true inversion charge as a function of gate voltage also enables us to link the gate voltage directly to the surface potential in the presence of a "frequency dependent threshold voltage (V_t) and flat band voltage (V_{fb}) shift", whereas in [12] it is not possible to obtain the surface potential to gate voltage relationship unless V_t or V_{fb} is known precisely. Another common approach in literature to obtain energy location of the traps is from the interface trap time constant by assuming a particular capture cross-section [16]. However capture cross section values discussed in literature vary orders of magnitude $(1 \times 10^{-12} \text{ to } 1 \times 10^{-19} \text{ cm}^2)$ and assuming a particular capture cross-section for energy estimation is susceptible to errors. Further, in our model we

also consider effects of series resistance (distributed channel resistance and lumped contact resistance) and gate leakage in addition to the D_{it} response while solving the equivalent circuit model. Solving the capacitance data together with the conductance data gives more accuracy in extracting the D_{it} and N_{inv} as the capacitance data is relatively less sensitive to parasitic resistance and gate leakage effects than the conductance data.

II. FACTORS AFFECTING SPLIT C-V MEASUREMENTS

In this section, we systematically explain the impact of distributed channel resistance, gate leakage and interface states on the admittance behavior of an $In_{0.53}Ga_{0.47}As$ MOS transistor biased in weak and strong inversion.

A. Effect of Distributed Channel Resistance

Since the interface states in the upper half of the semiconductor band gap can respond to small signal AC frequencies in the split capacitance measurement, one minimizes the error either a) by increasing the small-signal measurement frequency or b) by lowering the temperature of measurement so that the interface traps cannot follow the fast changing AC signal. However, the distributed nature of the channel resistance comes into play at higher frequencies which causes the measured capacitance to be lower than the true capacitance, resulting in an under-estimation of N_{inv} . This is illustrated in Fig. 1(a) where the frequency dispersion in both C-V and G-V data is caused solely by the channel resistance. Physically, the distributed channel resistance accounts for the energy loss during the minority carrier transport between the source/drain at any given position in the channel. As the channel length increases the dispersion in C-V and G-V increases due to the increased channel resistance.



Fig. 1. Effect of distributed channel resistance on (a) the C-V, and (b) the G-V characteristics. (c) Equivalent circuit of a MOSFET in strong inversion incorporating the channel resistance and ignoring the effects of interface states and gate leakage.



Fig. 2. Effect of tunnel conductance due to gate to channel leakage on (a) the C-V, and (b) G-V characteristics. (c) Equivalent circuit of a MOSFET in strong inversion incorporating the tunnel conductance and the distributed channel resistance.

B. Effect of Gate Leakage

In the case of ultra thin gate dielectric with significant gate leakage, we need to consider the effect of the tunnel conductance that shunts the oxide capacitance as well as the interface state capacitance. A direct impact of this increased tunnel conductance which appears in series with the channel and series resistance is shown in Fig. 2(a) where an increasing percentage of the AC test voltage appears across the channel resistance as gate leakage increases with higher V_g leading to a droop in the C-V characteristics. In Fig. 2(b), we show the effect of increased tunnel conductance on the G-V data where there is a linear monotonic increase in the measured conductance as the gate voltage is increased.

C. Effect of Interface States

Here we analyze the effect of interface states on the split C-V characteristics. The frequency dispersion in the C-V data

caused by the D_{ii} effect is shown in Fig. 3(a). A constant D_{ii} distribution $(1 \times 10^{13} / \text{cm}^2/\text{eV})$ across the upper half of the bandgap is assumed as an illustrative example in this case to calculate the frequency dispersion in the C-V and G-V. The presence of D_{ii} causes a frequency dependent "threshold voltage shift" in the C-V characteristics. At lower frequencies, the capacitance rises at lower V_g due to strong contribution from the midgap states, while at higher frequencies the midgap states cannot respond and the contribution comes primarily from the band edge states which are active at higher V_g . The conductance peak will also shift to higher V_g 's with higher frequencies as the band edge states get activated.

D. Effect of Channel Resistance, Gate Leakage, and Interface States

Finally, we show the combined effects of series contact resistance, distributed channel resistance, gate leakage and interface states on the C-V and G-V characteristics in the inversion regime in Figs. 4(a) and (b). We identify the various regimes marked as A, B, C and D in the G-V-f characteristics. In region A, at high gate voltage and low frequency, the measured conductance values are directly related to the tunneling conductance estimated from the DC gate leakage measurements. In region B, at high gate voltage and high frequency the series resistance (from contact resistance and distributed channel resistance) effect markedly increases the frequency dispersion of the measured conductance. It should be noted that in the high gate voltage regime as the Fermi level moves deep inside the conduction band the interface state conductance is negligible and the measured conductance is only the tunneling conductance modified by the series resistance and the measurement frequency. In region C, at lower gate voltage and lower frequency, the conductance peak exhibits strong frequency dependence due to contribution from the near midgap states. In region D, at intermediate gate voltage and higher measurement frequency the conductance contribution comes from the band edge states. The equivalent circuit model is described comprehensively in the next section.



Fig. 3. Effect of interface states, D_{it} on (a) the C-V characteristics, and (b) the G-V characteristics. The equivalent circuit model in inversion incorporating the effect of D_{it} is shown in the inset of (a).



Fig. 4. Effect of interface states, series resistance (contact and channel), and tunnel conductance on (a) the C-V characteristics, and (b) the G-V characteristics.

III. THE EQUIVALENT SMALL SIGNAL MODEL

A standard LCR meter (HP4285A) was used to measure the capacitance (Split C-V) and conductance of $In_{0.53}G_{0.47}As$ n-MOSFETs with LaAlO₃ gate dielectric, as a function of frequency and voltage for a range of temperature from 300K till 35K. Measurements were made in parallel mode with a small signal AC amplitude of 25 mV. The equivalent model in inversion including all the effects is shown in Fig. 5.

The model incorporates several features which are currently absent in recent publications while extracting the true N_{inv} and D_{it} especially when the channel is close to inversion or inverted. For example, the first step in the formulation of the model is the inclusion of the fixed series resistance, $R_{contact}$, at the two ends of the channel. Also, due to the distributed nature of the inversion channel resistance, R_{ch} , we create a transmission line model to accurately reflect the effect of R_{ch} as well as the tunnel conductance of the oxide, G_{tunnel} , arising from gate leakage. The gate oxide or insulator capacitance, C_{ox} , is estimated from the maximum capacitance measured in accumulation on a MOS capacitor. We verify the validity of our C_{ox} estimation by comparing with physical measurements (cross section TEM) as well as from minimizing the error between the calculated and measured C-V / G-V data points across the frequency range during the extraction process. A closed form equation was derived to model the admittance of the circuit shown in Fig. 5.

The measured admittance between the gate and source/drain for the circuit shown in Fig. 5 is given by (2),

$$Y_m = G_m + j\omega C_m \tag{2}$$

where G_m and C_m are the measured conductance and capacitance respectively. C_m and G_m are given by (3) and (4),

$$C_{m} = \operatorname{Re}[C' \tanh \lambda / \lambda] + (G_{ii} / C_{I} \omega) \operatorname{Im}[C' \tanh \lambda / \lambda] + (G_{tunnel} / \omega) \operatorname{Im}[\tanh \lambda / \lambda] \quad [F / cm^{2}]$$

$$G_{m} = \operatorname{Im}[C' \tanh \lambda / \lambda] + (C_{I} / C_{I} \omega) \operatorname{Re}[C' \tanh \lambda / \lambda]$$
(3)

$$\frac{-m}{\omega} = -\operatorname{Im}[C' \tanh \lambda / \lambda] + (G_{ii} / C_{i}\omega) \operatorname{Re}[C' \tanh \lambda / \lambda]$$

$$+ (G_{max} / \omega) \operatorname{Re}[\tanh \lambda / \lambda] \quad [F / cm^{2}]$$
(4)

respectively. Here $C' = [C_{ox}C_I]/[C_{ox} + C_I + G_{it}/j\omega], C_{ox}$ is



Fig. 5. Equivalent circuit model of MOSFET in weak and strong inversion: C_{ox} = oxide capacitance, G_{tunnel} = tunnel conductance, C_{it} = interface trap capacitance, G_{it} = interface trap conductance, C_{inv} = semiconductor inversion capacitance, R_{ch} = the gate bias dependent inversion channel resistance, $R_{contact}$ = series resistance associated with implanted source/drain regions, contacts and metal pads.

the oxide capacitance in F/cm^2 , $C_I = C_{inv} + C_{it} [F/cm^2]$, $\lambda = \gamma L/2$, $\gamma^2 = r_1 [j\omega C' + C'G_{it}/C_I + G_{tunnel}]$, $r_1 = (W/L)/g_{ds}$ [Ω], $G_{tunnel} = [\partial I_g / \partial V_g]/[WL] [S/cm^2]$, and

 $g_{ds} = [\partial I_{ds} / \partial V_{ds}] [\Omega]$. The above model is derived based on [15] after including the effects of C_{it} and G_{it}.

The admittance due to a distribution of interface traps is given by the capacitance, C_{it} , and the conductance, G_{it} , given by (5) and (6) respectively [13].

$$C_{it} = q \int_{-\infty}^{\infty} \frac{D_{it}}{\omega \tau} \tan^{-1} \omega \tau P \sigma_s, E dE [F/cm^2]$$
(5)

$$\frac{G_{it}}{\omega} = \frac{q}{2} \int_{-\infty}^{\infty} \frac{D_{it}}{\omega \tau} \ln 1 + \omega^2 \tau^2 P \sigma_s, E dE [F/cm^2]$$
(6)

A random spatial distribution of interface defects causes a spatial distribution in the band bending which is accounted by the integrand in (5) and (6) where, τ is the interface trap time constant, σ_s is the surface potential fluctuation and *P* is a Gaussian distribution with variance of σ_s^2 .

The effect of surface potential fluctuation was not considered in our analysis of C_{it} and G_{it} . The transmission line equivalent circuit model was solved for τ , D_{it} and C_{inv} using the algorithm explained below. The measured conductance and capacitance data from the split C-V measurement are converted to measured admittance data, $Y_{measured}$. This admittance data is further corrected for contact resistance (obtained from transfer length method) as given by $1/Y_{corrected} = 1/Y_{measured} - R_{contact}/2$. The factor 2 in the above expression is due to the symmetry between source and drain in the split C-V measurement. This corrected data is now solved to obtain D_{ib} τ and C_{inv} over the entire frequency range as given by (7), at a particular bias point.

$$\sum_{\text{frequency}} Y_{\text{corrected}} - Y_m(D_{it}, \tau, C_{inv}) = 0$$
(7)



Fig. 6(a) Experimental C-V, and (b) experimental G-V data at 300K compared to the modeled data using the proposed equivalent circuit model.

Here $Y_m(D_{it}, \tau, C_{inv})$ is the set of all possible solutions as per (2) for the range of D_{ib} , τ and C_{inv} considered. The channel conductance, g_{ds} , and the tunnel conductance, G_{tunneb} used in (2) are obtained from Id-Vd and Ig-Vg measurements respectively. This process is repeated over the entire bias points to obtain D_{ib} , τ and C_{inv} , as a function of voltage. Obtaining true inversion charge as a function of Vg enables a natural translation from gate bias to surface potential even in the presence of frequency dependent V_t and V_{fb} shift. This allows us to accurately express D_{it} as a function of energy. Figs. 6(a) and (b) show the 300K experimental C-V and G-V data compared to the solution obtained from our model which shows excellent agreement.

IV. EXTRACTING $D_{IT} \tau$ And N_{INV}

Having confirmed the validity of the proposed equivalent circuit model, we proceed to extract the interface state density, its response time and the true inversion carrier density as a function of gate voltage. We apply our technique to a wide range of operating temperatures of the $In_{0.53}Ga_{0.47}As$ MOSFET to extract the D_{it} , τ and true N_{inv} from 300K down to 35K.

Unlike the full conductance method, we can quantitatively extract the D_{it} over a wide range of energy at room temperature even though the precise location of the conductance peak, $(G_{it} / \omega)_{peak}$ is outside the measurement frequency range. Fig. 7 shows the equivalent parallel conductance of the interface traps as a function of gate bias and frequency. It can be seen that a subset of conductance peaks particularly at low gate bias which corresponds to midgap trap response is outside the measurement frequency range. However, on solving the equivalent circuit model, the D_{it} data is precisely extracted for low gate bias. The extracted D_{it} and τ are shown in Figs. 8 (a) and (b). Fig. 8(b) also reveals the typical Λ -shaped characteristic of the interface trap time constant, $\tau(E)$. It is noteworthy that the D_{it} profile extracted independently from the measured C-V and G-V data at 3 different temperatures are consistent with each other. The D_{it} profile could be interpreted as sum of two Gaussian distributions with high and low peak values. The Gaussian



Fig. 7. Equivalent parallel conductance of the traps (G_{it}/ω) as a function of gate bias and frequency. The trace of the conductance peaks (shown in dotted red line) reflects the Fermi level movement.



Fig. 8. (a) Extracted interface state density versus energy, and (b) the extracted trap response time versus energy.



Fig. 9. (a) Extracted trap response time versus energy compared to the theoretical response time. (b) Experimental and theoretical (without D_{ii}) sub-threshold slope and the interface state density extracted from the experimental sub-threshold slope as a function of temperature.

with the high peak spans across the midgap of the $In_{0.53}Ga_{0.47}As$ semiconductor and is responsible for the subthreshold slope (SS) degradation commonly observed in In_{0.53}Ga_{0.47}As based MOSFETs [14]. The second Gaussian distribution with lower peak extends towards and into the conduction band. Since this peak is much reduced, high on current in inversion is expected and has been experimentally reported for In_{0.53}Ga_{0.47}As MOSFETs [7]. In Fig. 9(a), we compare the extracted time constant at 3 different temperatures with the theoretical value calculated using the expression $\tau_e = N_c \sigma v_t^{-1} \exp(\Delta E/kT)$ [13], where N_c is the effective conduction band density of states, σ is the capture cross section, vt is the thermal velocity of electrons and $\Delta E = E_c - E$ is the energy location of the trap with respect to the conduction band. Since we are analyzing the device in inversion we need to only account for the exchange of carriers with the minority band (i.e. conduction band for the p-type substrate). We get a strong agreement between the measured time constant and its theoretical estimate over a large range of energy and temperature, further validating our extraction



Fig. 10. Measured C-V and extracted true C-V characteristics of $In_{0.53}Ga_{0.47}As$ MOSFETs at 300K , 200K and 77K.

approach. Fig. 9(b) compares the sub-threshold slope (*SS*) obtained from the measured transfer characteristics of In_{0.53}Ga_{0.47}As MOSFETs and the theoretical *SS* without D_{it} as a function of temperature. The expression for the *SS* is given by $SS = [2.3kT/q][1+(C_d + C_{it})/C_{ox}]$, where C_{ox} is the oxide capacitance, and C_d is the semiconductor depletion layer capacitance and C_{it} is the capacitance due to interface states. The interface state density obtained from the experimental *SS*, plotted in Fig. 9(b), is around 1.5 x 10^{13} cm⁻²eV⁻¹. This is consistent with the range of the midgap D_{it} concentration profile we extracted from the small signal admittance modeling (Fig. 8(a)) where the D_{it} ranges from 1 x 10^{13} to 3 x 10^{13} cm⁻²eV⁻¹.

Fig. 10 shows the measured C-V characteristics exhibiting the effects described above and the extracted true inversion capacitance characteristics for 3 different temperatures. The true mobile inversion charge density as a function of gate voltage, V_g , is plotted in Fig. 11(a). The slope of each of the curves is roughly equal to 0.49 µF/cm² which is equivalent to the series combination of the In_{0.53}Ga_{0.47}As inversion channel capacitance (limited by density of states) and the insulator capacitance which is 0.65 µF/cm² (EOT of 5.45 nm). Finally, the effective inversion channel mobility of In_{0.53}Ga_{0.47}As MOSFETs is extracted (Fig. 11 (b)) using the low field drain conductance and the inversion charge extracted using the model.



Fig. 11. (a) Extracted N_{inv} from the C-V and G-V measurements, and (b) measured effective mobility as a function of inversion charge density.

V. CONCLUSIONS

In summary, we have presented here a comprehensive equivalent circuit model to analyze the true small signal response of inversion carriers in $In_{0.53}Ga_{0.47}As$ MOSFETs with high- κ gate dielectric. Our approach attributes the frequency dispersion commonly observed in the C-V and the G-V measurement data of $In_{0.53}Ga_{0.47}As$ MOSFETs quantitatively to various contributing factors such as the interface states, contact resistance, distributed channel resistance and the tunnel conductance. This allows us to self consistently solve for the frequency dependent interface state response and the frequency independent true inversion carrier density for a range of gate bias.

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