Low Power Loadless 4T SRAM cell based on Degenerately Doped Source (DDS) $In_{0.53}Ga_{0.47}As$ Tunnel FETs

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We propose a Loadless 4T SRAM cell using degenerately doped source (DDS) p-channel $In_{0.53}Ga_{0.47}As$ Tunnel FETs (TFETs) as dual purpose access/load devices and low leakage steep sub-threshold n-channel TFETs as drive devices. A Loadless 4T CMOS SRAM cell [1] has the requirement that the leakage current of the PMOS access transistors should be larger than the leakage current of the NMOS drive transistors to maintain state. In this paper, we introduce a p-type TFET with a degenerately doped source, which has a kT/q sub-threshold slope, compared to an n-type TFET which has a sub-kT/q slope. This difference in sub-threshold behaviour of the DDS PTFET and DDS NTFET helps to maintain the I_{OFF} ratio which is required for cell stability. We explain the temperature dependent sub-threshold characteristics of the $In_{0.53}Ga_{0.47}As$ (DDS) p-TFET by analyzing the position of the Fermi level in the source of the p-TFET as a function of source doping. Further, the asymmetric source drain architecture of the TFETs is exploited to solve the adjacent bit flip problem of unselected Loadless 4T SRAM cells during a column write operation. Finally, we include a comparison of the leakage energy and cell access time of the TFET based SRAM cell and benchmark its performance relative to state-of-the-art CMOS based 6T SRAM cells.

By modeling the measured forward and reverse bias characteristics of an $In_{0.53}Ga_{0.47}As$ Esaki tunnel-diode (Fig 1) using Sentaurus TCAD [2], non-local band-to-band tunnelling model parameters (m_C=0.07m_0, m_V=0.05m_0, g_C=g_V=0.1 and E_G=0.74) were extracted. An ultra-thin-body double gate NTFET (Fig 2A) and a complementary PTFET, with identical but reversed doping profiles (Fig 2B), are proposed to maximize drive current. It was observed during simulations that a kT/q dependent sub-threshold slope occurs for the PTFET (Fig 3A) unlike the steep sub-threshold for the NTFET (Fig 3B). Because of the different effective density of states for the conduction band (N_C = 2.1e17 cm^{-3}) and the valence band (N_V = 7.7e18 cm^{-3}) in $In_{0.53}Ga_{0.47}As$, the Fermi level ($E_{F,S}$) in the n+ DDS region (N_D = 8e19 cm^{-3}) of the PTFET is 1.442 eV above the conduction band edge ($E_{C,S}$) (Fig 4A), where as the Fermi level ($E_{F,S}$) is only 0.14 eV below the valence band edge ($E_{V,S}$) in the p+ DDS region (N_A = 8e19 cm^{-3}) of the NTFET (Fig 4B). We consider a simplified band diagram model (Fig 5A/5B), and evaluate the band-to-band tunnelling integral shown in Fig 6 [3]. Fig 7A shows that in a DDS PTFET, due to $E_{C,S}$ being 1.442 eV below the $E_{F,S}$ in the source region, a large portion of the temperature dependent part of the Fermi difference function |fd(E)-fs(E)| occurs in the window between $E_{V,Ch}$ and $E_{C,S}$ when a negative gate voltage sweep is done, leading to a temperature dependent sub-threshold slope (Fig 7B). Fig 7C shows that for a DDS NTFET, only a small part of the temperature dependent tail of the function |fd(E)-fs(E)| occurs in the window between $E_{C,Ch}$ and $E_{V,S}$ when a positive gate voltage sweep is done, leading to a temperature independent sub-threshold slope for the NTFET (Fig 7D). Thus, the sub-threshold characteristic of a TFET is highly dependent on the position of the Fermi level with respect to the band edge in the DDS region, because this relative position affects how much of the temperature dependent part of |fd(E)-fs(E)| is cut-off [2].

Fig 8A shows the schematic of a Loadless 4T TFET SRAM cell and Fig 8B shows the transfer characteristics of 32nm CMOS (High Perf /Low Standby Power) and 30nm $In_{0.53}Ga_{0.47}As$ (DDS) TFETs. Fig 9A shows a comparison of the access delay of various minimally sized SRAM cells. Because of the I_{OFF} ratio requirement, the NMOS drive transistor of the Loadless 4T CMOS cell has a higher V_{TH} than its PMOS access transistor – this hampers the ON current of the SRAM cell during read access. Since the drive transistor of the Loadless 4T TFET cell is an $In_{0.53}Ga_{0.47}As$ (DDS) NTFET with a steep sub-threshold, it is capable of delivering high I_{ON} while simultaneously satisfying the I_{OFF} ratio requirement. As a result, the Loadless 4T TFET cell is 4-50x faster than the Loadless 4T CMOS cell in the V_{CC} range 0.3 to 0.15 Volts. However, the Loadless 4T TFET cell, whose ON current is limited by the lower I_{ON} of the DDS PTFET access transistor, is observed to be 4-10x slower than a 6T CMOS (HP) SRAM cell, which has HP NMOS for both access and drive transistors. The leakage power of the 4T CMOS cell and the 4T TFET cell are identical and are caused mostly by the PMOS and PTFET access transistors which have a kT/q sub-threshold slope. Fig 10A illustrates how the bit-flip during column write is averted due to the asymmetric drain-source architecture of the PTFET access transistor. Fig 10B shows that the retention time of Loadless 4T TFET cell is 100 times that of the Loadless 4T CMOS in a bit-flip condition at V_{CC} 0.5 Volts.

In conclusion, by taking advantage of the DDS PTFET and its temperature dependence, as well as the source-drain asymmetry of TFETs, we have introduced a 4T TFET SRAM cell which is 100 times faster than an LSP CMOS 6T SRAM cell and shows 3 times lower standby power consumption than a HP CMOS 6T SRAM cell.

[1] Noda, et al, *IEEE Tran. Electron Dev*, **48**, pp 2851-2855, (2001) [2] Sentaurus Users Guide, Ver. Z-2007.3 [3] J. Knoch, et al., *Solid State Electronics.*, **51**, pp 572-578, (2007).

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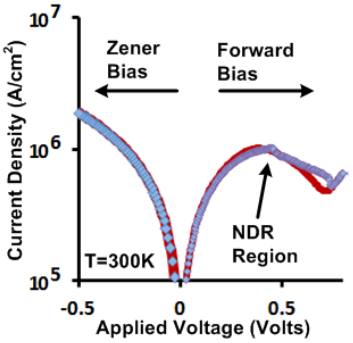

Fig 1 Measured and modeled current density for $In_{0.53}Ga_{0.47}As$ tunnel-diode

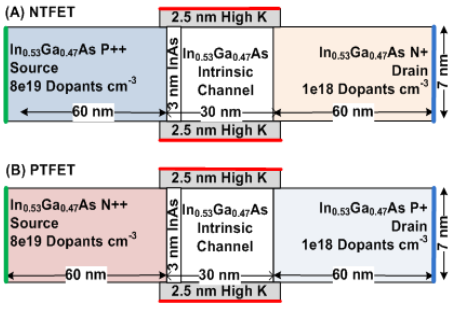

Fig 2. (A) Proposed design of $In_{0.53}Ga_{0.47}As$ (DDS) NTFET and (B) $In_{0.53}Ga_{0.47}As$ (DDS) PTFET

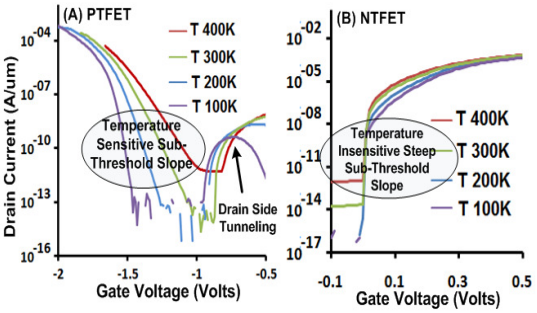

Fig 3. Sub-Threshold Slopes for the proposed DDS NTFET and DDS PTFET at a Drain Bias of 0.5 Volts

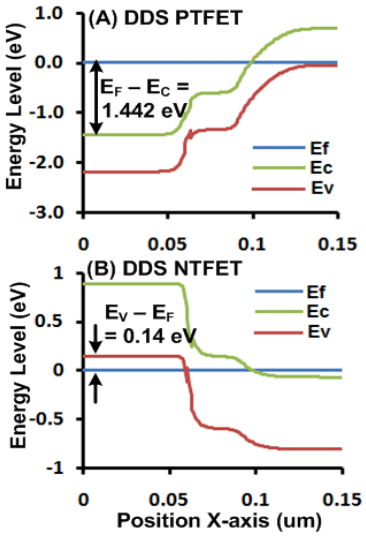

Fig 4. Band Diagrams (neutral bias conditions) for (A) DDS PTFET ($E_{V,Ch}$ and $E_{C,S}$ aligned initially) (B) DDS NTFET ($E_{C,Ch}$ and $E_{V,S}$ aligned initially)

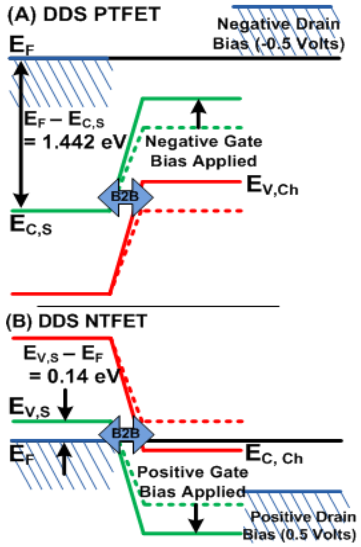

Fig 5. Simplified Band Diagrams for (A) the DDS PTFET and (B) the DDS NTFET under applied bias

$$I_d = \frac{2q}{h}\left(\int_{E_V^{ch}}^{E_C^s} dE.T_{WKB}(E).(f_s(E) - f_d(E))\right) \quad \left.\begin{array}{l} E_V^{ch} > E_C^s \\ E_V^{ch} < E_C^s \end{array}\right\}$$

$$I_d = 0$$

$$T_{WKB} \approx exp\left(\frac{4\lambda\sqrt{2m^* E_g^3}}{3q\hbar(E_V^{ch} - E_C^s + E_g)}\right)$$

$E_g(Band\,Gap) = 0.74eV$
$m^*(Tunneling\,Mass) \approx 0.05m0$
$q\ (Charge\,of\,Electron) = 1.602 * 10^{-19}C$
$\lambda\ (Initial\,Barrier\,Width) = 2.5nm$

Fig 6. The Tunneling Integral specification for PTFET and NTFET

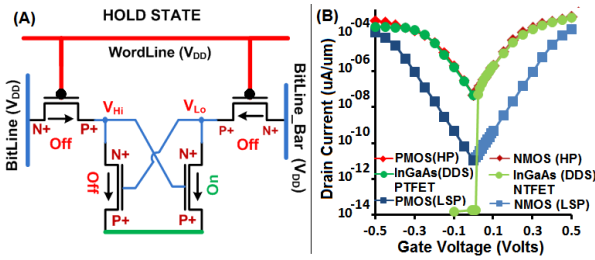

Fig 8 (A) 4T Loadless $In_{0.53}Ga_{0.47}As$ SRAM Cell in Hold State (B) Id-Vg Characteristics of various devices

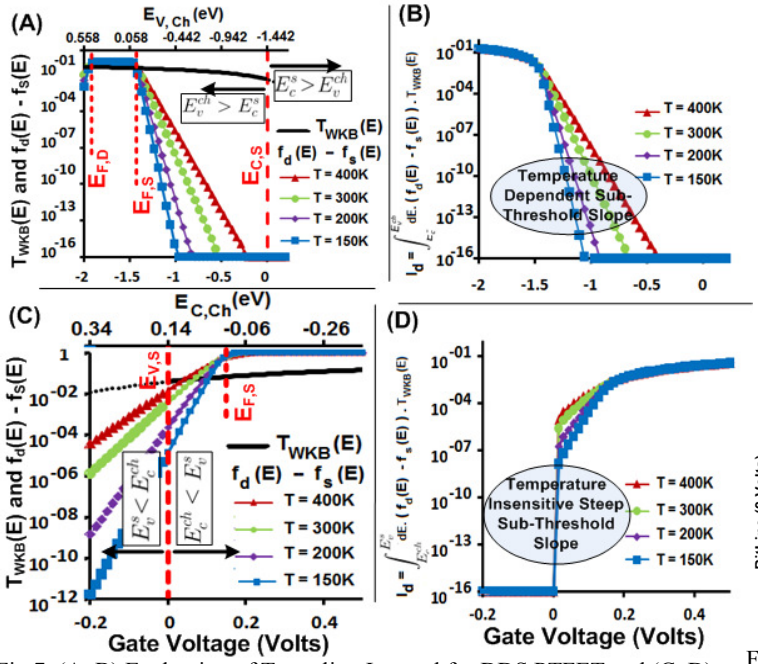

Fig 7. (A, B) Evaluation of Tunneling Integral for DDS PTFET and (C, D) DDS NTFET

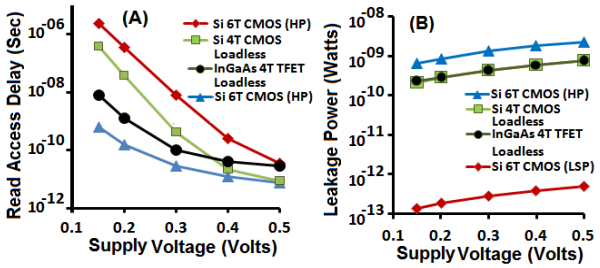

Fig 9 Comparison of (A) Delay and (B) Leakage of SRAM Cells

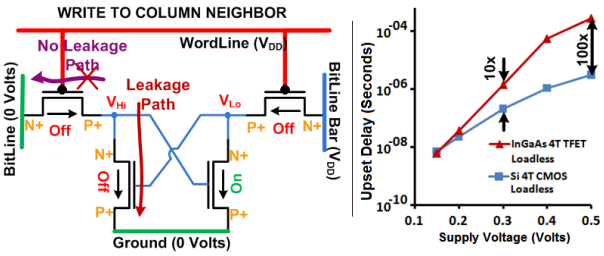

Fig 10 Improvement of cell upset due to write operation to a column neighbor