Analyzing Energy-Delay Behavior in Room Temperature Single Electron Transistors

***Abstract*—This paper presents Single Electron Transistor (SET) devices operating at room temperature as an attractive option to implement low energy consumption circuits with low-to-moderate performance requirements. Currently, such circuits are implemented using CMOS technologies operating at low supply voltages. CMOS is usually leakage dominated at such a low voltage regime and various optimizations are necessary to design low energy circuits. By discussing the energy-delay trade-offs for SET devices and comparing them to those of contemporary CMOS technology, we present an argument that SET devices may be more favorable compared to CMOS from the energy and delay standpoints at low supply voltages.**

***Index Terms*—Energy Efficient, Single Electron Transistor, Energy-Delay Trade-Off**

I. Introduction

Attaining low energy operation with low-to-moderate performance (10KHz-100MHz) is a desirable goal for a number of applications such as environmental monitoring sensors and biological implants. Such systems are typically characterized by very infrequent activity cycles with energy drawn from a built–in battery. For such applications it is important to minimize energy consumption, not only in the active mode but also in the stand-by mode, in order to maximize the life of the system. In commonly used voltage mode logic, the main form of energy consumption during the dynamic operation of circuits is through the charging and discharging of gate and parasitic capacitances in the circuit. In order to minimize dynamic energy consumption, which is given by E = QV/2, it is necessary to minimize not just the supply voltage but also the amount of charge that is transferred during the switching activity. The theoretical minimum switching energy for CMOS, kT*ln*2 occurs when a supply voltage of kT*ln*2/*q* drives a charge of *q* in order to cause an output switch [1]. In order to reduce standby energy consumption it is important to reduce the leakage charge that flows in a circuit during the duration of standby.

Minimizing energy using supply voltage scaling for traditional CMOS has been a significant challenge. On one hand scaling down supply voltage reduces the dynamic energy but not without sending the MOSFET into its sub-threshold region where the static leakage energy starts dominating. As a result, minimizing energy for CMOS devices involves determining the optimal supply and threshold voltage necessary for minimum energy operation for a given activity factor and performance [2]. Other solutions involve selecting the optimal technology for low energy operation [3] and intentional selection of older low leakage technology in the standby mode to reduce leakage energy consumption (for memory) [4].

In general, in order to attain low energy operation it is preferable to have a device which is capable of operating at room temperature at a few kT/q supply voltage. It is also preferable that the device has low leakage current and very small gate and parasitic capacitances in order to minimize the energy required for switching.

In this paper show that Single Electron Transistor (SET) devices operating at room temperature are an attractive option in order to design low energy logic circuits. A SET device typically consists of a nanodot connected to source and drain contacts through high resistance tunnel barriers. The tunnel barrier resistance R_T is required to be large compared to the fundamental quantum of resistance, h/e^2 (26kΩ), in order to ensure charge quantization on the nanodot. When the single electron charging energy e^2/C_Σ of the nanodot (with capacitance C_Σ) is much larger than the available thermal energy kT, a Coulomb gap (separating the filled and empty energy states) occurs in the nanodot which prevents current from flowing for small drain bias voltages – a phenomenon known as Coulomb blockade. Early experiments using SETs involved large nanodots with insignificant single electron charging energies. These devices required ultra low temperature (~ 10 mK) in order to observe the Coulomb blockade phenomenon. More recently due to improvements in fabrication of nanodots there have been many observations of the Coulomb blockade even at room temperature [5] [6]. The feature sizes of such devices are small enough for the single electron charging energy of the nanodot to be dominant even at room temperature.

There have been numerous circuit design efforts [7] [8] [9] in literature which propose different circuit topologies. However, to the best of our knowledge there has not been an effort to understand the energy-delay trade offs involved in SET based circuits. Our main intent in this paper is to understand the energy-delay trade-offs for SETs at room temperature operation and compare them to the energy-delay trade-offs for sub-threshold CMOS circuits at different activity factors. In section II we discuss the transconductance characteristics of SETs (at 0 K and at 300 k) and derive the expressions for gate voltages at which peak and valley currents occur for a single SET. By understanding the transconductance characteristics we discuss appropriate ways to apply input voltages to an SET device in order to design a switch. We also discuss the transconductance characteristics for arrays of SET devices. In section III we discuss the energy-delay trade-off characteristics of SET devices and compare them to the energy-delay trade-offs for 32 nm CMOS. We show that for SET devices it is possible for delay

to decrease as supply voltage is decreased making it preferable to scale the supply voltage as low as possible (noise margins permitting) in order to minimize both energy and delay. We show that SET devices are in-principle capable of exhibiting a better energy-delay performance compared to CMOS making them an attractive option compared to sub-threshold CMOS.

II. Understanding I-V Charateristics of Room Temperature SETs

A. The Device Model and I-V Characteristics

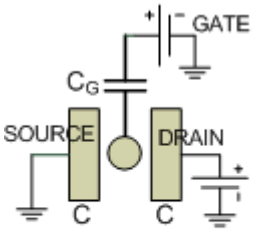

FIGURE 1 - A Simple Model of a Three Terminal SET Device

We use a simple three-terminal model of an SET device as shown in Figure 1 and use the Monte Carlo simulator SIMON [10] to obtain its transconductance characteristics. The parameters of the model are the gate capacitance C_G, the tunnel barrier coupling capacitance C and the tunnel barrier resistance R_T. The total capacitance C_Σ of the device is given by $C_G + C + C$ (assuming that both source and drain tunnel barriers have identical coupling capacitance). Room temperature SETs have been shown to have a Coulomb gap in the range 150 to 200 mV [5] [6]. In order to obtain a Coulomb gap in this range the self capacitance, C_Σ, of the device has to be in the range 0.4 aF to 0.53 aF. We set the value of C_Σ to 0.4 aF for the simulation. Typically the source and the drain contacts are coupled poorly to the nanodot whereas the gate contact is coupled more tightly to the nanodot - thus, we set the gate capacitance-to-barrier capacitance ratio (C_G/C) to 10. We also set the tunnel barrier resistance value R_T to a nominal value of 1 MΩ ($38\times h/e^2$). The transconductance characteristics of an SET device show characteristic Coulomb oscillations as shown in Figure 2.

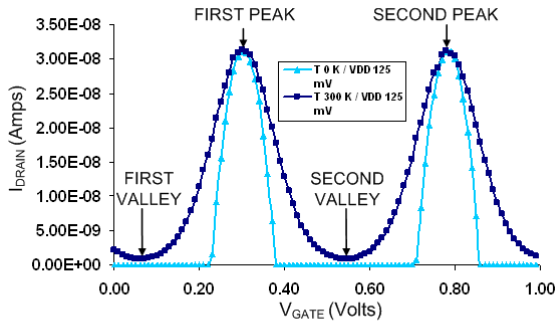

FIGURE 2 - Transconductance Characteristics of an SET Device with Drain bias 125 mV at T = 0K and T = 300K

As Figure 2 shows, the transconductance plot of a SET device consists of current peaks and valleys. It is useful to obtain derivations for the voltages at which current peaks and valleys occur. We use electrostatics, the band diagram of an SET device, and empirical observations to determine the gate voltages at which peak and valley currents occur. Figure 3A shows the band diagram of a three-terminal SET with its source and drain terminals grounded, with no gate voltage applied. The filled and empty energy states in the channel are separated by a Coulomb gap whose width equals the self charging energy, $U_0 = e/C_\Sigma$, of the nanodot.

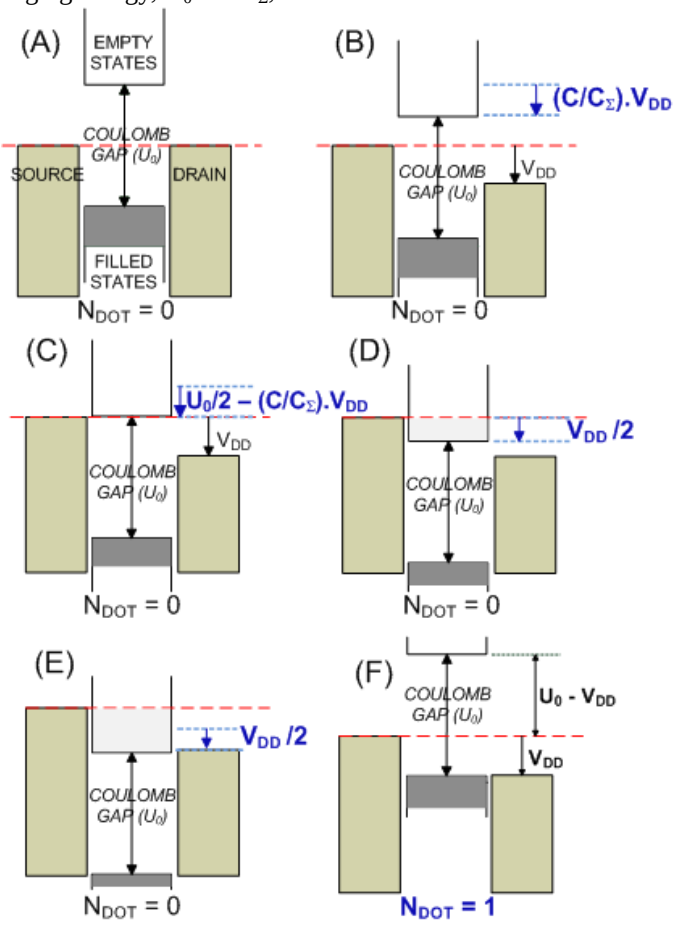

FIGURE 3 - Band Diagrams of an SET Device at Different Gate Voltages

When the drain is biased by a voltage V_{DD} the potential of the nanodot is lowered by $(C/C_\Sigma).V_{DD}$, due to the capacitive coupling, C, between the drain and the nanodot, as shown in Figure 3B. We assume that the circuit is at 0 K and the only way for current to flow is to lower the empty states of the nanodot to lie in between the source and drain Fermi levels. Thus, in order for current flow to start, the potential of the nanodot must be lowered by $U_0/2 - (C/C_\Sigma).V_{DD}$ which requires a gate voltage of

$$V_{On} = \left(\frac{U_0}{2} - \frac{C}{C_\Sigma}.V_{DD}\right).\frac{C_\Sigma}{C_G} \qquad (1)$$

When this gate voltage is applied, the empty levels of the nanodot start to enter the region between the source and the drain Fermi levels as shown in Figure 3C, and as a result current flow begins.

Peak current flow occurs when the lowest empty state is midway between the source and the drain Fermi levels as shown in Figure 2D. In order for this to occur, an extra gate voltage (2) must be applied in addition to the gate voltage (1)

$$V_{On \rightarrow FirstPeak} = \frac{V_{DD}}{2}.\frac{C_\Sigma}{C_G} \qquad (2)$$

Hence the gate voltage where the first peak current flow occurs can be approximated as

$$V_{First\ Peak} = \frac{e}{2.C_G} + \frac{V_{DD}}{2} \qquad (3)$$

This provides an approximation of the gate voltage corresponding to the peak current without having to derive it self-consistently taking into consideration the net electron density in the nanodot as current flows. We find that this approximation matches reasonably well with the transconductance graph of an SET that is obtained through Monte Carlo simulation.

In a similar manner we can obtain a derivation for the distance between two current peaks at T = 0K. Assuming that the device is at the first current peak as shown in Figure 3D, by applying the gate voltage shown in (2) we can cause the first empty level to reach the same potential as the drain Fermi level as shown in Figure 3E.

When this happens the first empty level of the nanodot is occupied by an electron, increasing the charge of the nanodot by ***e*** (the charge of an electron). Due to the single electron charging energy of the nanodot, a Coulomb gap occurs between the newly occupied energy level and the next empty level as shown in Figure 3F.

In order for current flow to start again, the potential of the nanodot has to be lowered by $U_0 - V_{DD}$ so that the empty levels in the nanodot are lowered to lie in between the source and drain Fermi levels as shown in Figure 4D. In order to do this an additional gate voltage shown in (4) needs to be applied.

$$V_{Off \rightarrow On} = (U_0 - V_{DD}).\frac{C_\Sigma}{C_G} \qquad (4)$$

Having done this the next current peak will now occur by applying an additional gate voltage shown in (2). Thus, in total the gate voltage sweep from the first peak to the second peak is given by the sum of the terms, (2) multiplied twice and (4). By observation, the distance between any two current peaks is the same. Hence the distance between the first peak and the second peak given by (5) applies for the distance between any two current peaks.

$$V_{FirstPeak \rightarrow SecondPeak} = \frac{e}{C_G} \qquad (5)$$

Figure 2 shows the transconductance characteristics for a SET device biased at 125 mV at T = 0K and T = 300K. We observe that thermal broadening does not change the positions of the peaks, the distance between the peaks and the value of the peak current. Hence, the location of the first peak given by (3) and the distance between any two consecutive current peaks given by (5) can also be used at room temperature.

By observation, each current valley lies exactly in between the current peaks. Thus, we can derive the expressions for the location of the first valley. As shown in (6), the location of the first valley is given by subtracting half the distance of the width between current peaks from the location of the first current peak.

$$V_{First\ Valley} = \left(\frac{e}{2.C_G} + \frac{V_{DD}}{2}\right) - \frac{1}{2}.\frac{e}{C_G} = \frac{V_{DD}}{2} \qquad (6)$$

B. Biasing SET devices

Having derived the voltages at which peak and valley currents occur for an SET device, we now discuss how an SET device can be biased to work as a switch. In general, the common way to turn on a transistor which is biased with a drain voltage V_{DD} is to apply a gate voltage of V_{DD}. The current that then flows through the transistor at gate voltage of V_{DD} Volts is known as the "On" current and the current that flows through the transistor at gate voltage 0 Volts is termed as the "Off" current. However, in the case of a three terminal SET device operating at T = 300 K this method of biasing does not work as intended because the first current valley occurs at a gate voltage of $V_{DD}/2$ starting from gate voltage 0.

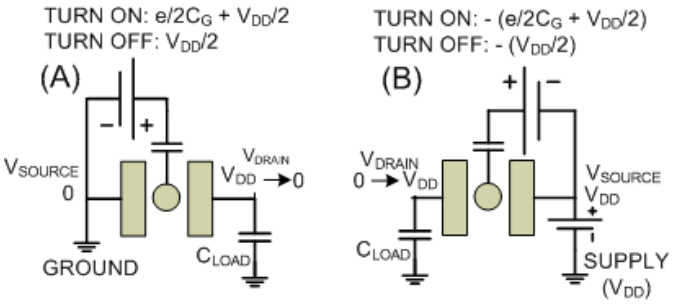

FIGURE 4 – Charging and Discharging a Load Capacitance Using a 3-Terminal SET Device

We would like the device to display a (possibly large) positive transconductance when the gate voltage is changed from the "Off" voltage to the "On" voltage. In the case of a three terminal SET device, the simplest way to do this is to define the "Off" gate voltage of the device as $V_{FirstValley}$, the gate voltage for the first current valley (6), and to define the "On" gate voltage as $V_{FirstPeak}$, the voltage for the first current peak (3).

The bias voltages required to discharge a load capacitance are shown in Figure 4A. A gate voltage of $V_{FirstPeak}$ is used to turn on the SET device so that it can discharge the load capacitance. The drain-source bias of the discharging device then changes from V_{DD} to 0 as the load capacitance discharges.

The bias voltages required to charge a load capacitance are shown in Figure 4B. We would like to mention here that the same SET device can function as both an n-type device and a p-type device due to its symmetric band structure. A gate voltage of $-V_{FirstPeak}$ is used to turn on the SET device which charges the load capacitance. The drain-source bias of the

charging device changes from $-V_{DD}$ to 0 as the load capacitance charges.

C. *Arrays of SET devices*

So far we have discussed the transconductance properties of a simple three terminal SET. Here, we discuss the properties of an array of SET devices. An array of SET devices is different from a series of SET devices in that it consists of nanodots directly coupled to each other through tunnel barriers without being separated by intermediate capacitances. The idea is clarified in Figure 6. Figure 6A shows two 3-terminal SET devices in series, whereas Figure 6B shows an array of two nanodots coupled to each other. SET nanodots in the array configuration are more energy-efficient compared to SET devices in series because of the absence of the intermediate wire capacitances.

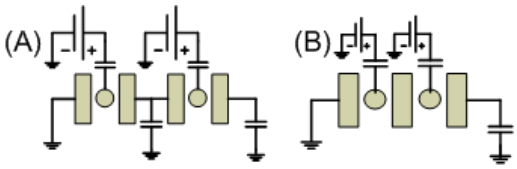

FIGURE 5 – (A) A Series of Nanodots and (B) an Array of Coupled Nanodots

First, we would like to justify why we can treat a coupled nanodot system using individual quantum simulations for each nanodot rather than treating the array of nanodots as an ensemble (which requires full many-body treatment). We borrow conclusions from a large body of theoretical and experimental device research [11] [12] [13] that has been done on coupled nanodots. These studies show that, when the inter-dot resistance, $R_{int,}$ separating two coupled nanodots exceeds $2.5 \times (h/e^2)$ the total number of electrons, $n_{tot,}$ in the ensemble consists of the electrons localized on the first dot, n_1, and the electrons localized on the second dot, n_2. These studies also show that when the inter dot resistance, R_{int}, approaches $0.5 \times (h/e^2)$, the coupled nanodots lose charge localization and behave as if they are one large quantum dot. Thus, if the inter-dot resistance, R_{int}, is large enough (R_{int} is set to $38 \times (h/e^2)$ in our MC simulations), we can consider charge to be localized on individual nanodots and then compute tunneling rates individually for each of the tunnel barriers.

The transconductance of two coupled nanodots is controlled by two gate voltages V_{G1} and V_{G2}. For the parameters chosen in Section II-A, the transconductance contours of the device for different drain voltages can be plotted with respect to the two gate voltages as shown in Figure 6A and 6B. The three dimensional contour of the transconductance with respect to both V_{G1} and V_{G2} is shown in Figure 7 shows that the location of the first peak current flow is a function of both gate voltages.

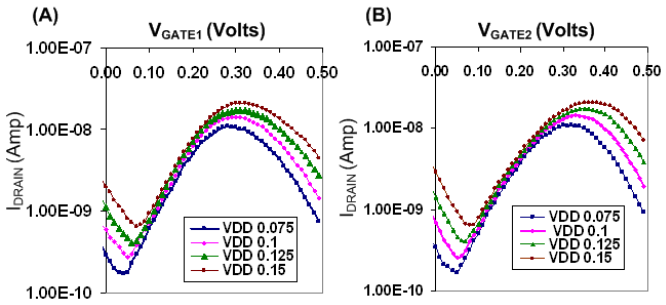

FIGURE 6 - Transconductance Contours of Two Coupled Nanodots as a function of (A) Control Gate of the First Nanodot and (B) Control Gate of the Second Nanodot

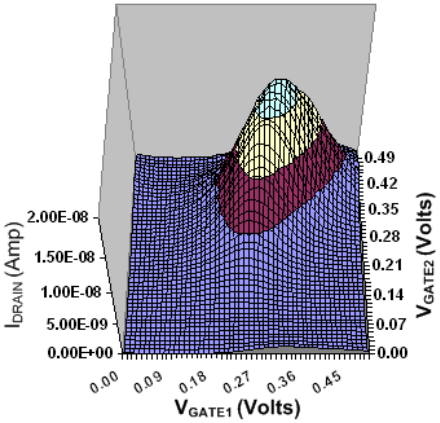

FIGURE 7 - Transconductance Contour of Two Coupled Nanodots

It is cumbersome to derive the gate voltages corresponding to peak current for two coupled nanodots as we did in Section II-B. However, we can understand intuitively that the maximum current flow occurs when the levels of the first dot are 1/3rd of the way between the source and drain Fermi levels, and the levels of the second nanodot are 2/3rd of the way between the source and the drain Fermi levels a shown in Figure 8. By recognizing where the peak current flows, we can come up with expressions (7) and (8) for the gate voltages for the current peak of two coupled nanodots.

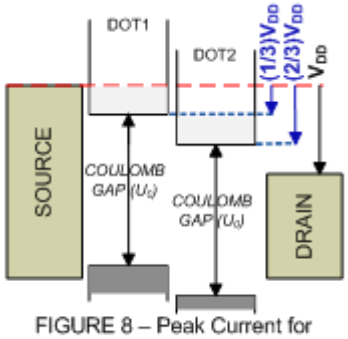

FIGURE 8 – Peak Current for Two Coupled Nanodots

$$V_{Gate1,Peak} = \frac{e}{2.C_G} + \frac{V_{DD}}{3} \qquad (7)$$

$$V_{Gate2,Peak} = \frac{e}{2.C_G} + \frac{2.V_{DD}}{3} \qquad (8)$$

These expressions match reasonably well with the simulated curves for the parameters chosen in Section II-A. Since it is too cumbersome to use different gate voltages for different

SET devices in series we use the following expressions to operate coupled nanodot devices (The peak current does not vary significantly when (9) is used instead of (7) and (8)).

$$V_{Turn\,On} = \frac{e}{2.C_G} + \frac{V_{DD}}{2} \qquad (9)$$

$$V_{Turn\,Off} = \frac{V_{DD}}{2} \qquad (10)$$

D. Implementing Binary Decision Diagram (BDD) Based Logic Circuits

The 3-terminal SET device described in Section II-A and the SET nanodot arrays described in Section II-C can be used to implement BDD based logic circuits. Binary Decision Diagrams can be used to represent logic functions in a minimal way [14]. Fabrications of BDD based SET circuits [15] [16] have also been done. In contrast, we propose using coupled nanodots to implement functions rather than using individual wire coupled SET devices (please refer to Figure 5).

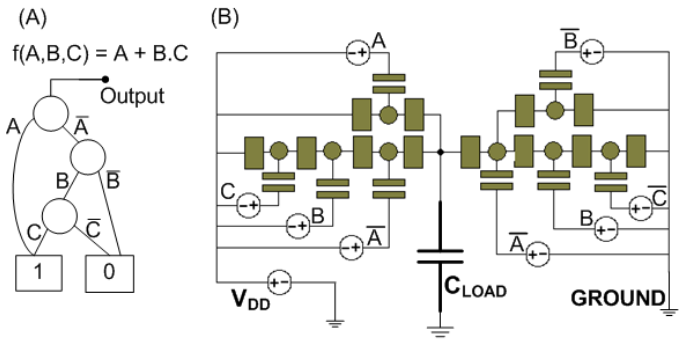

FIGURE 9 – (A) The BDD of an Arbitrary Function and (B) The Implementation of the BDD Using SET nanodots

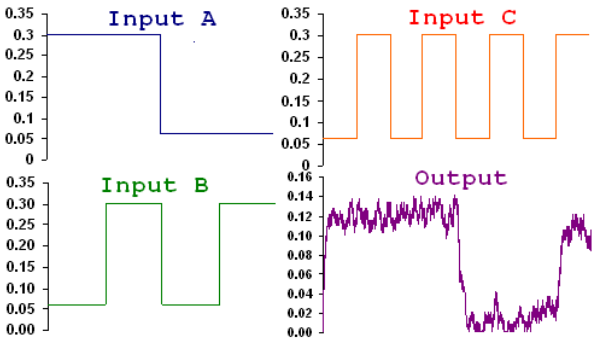

FIGURE 10 – The Output of the BDD Circuit with Supply Voltage (V_{DD}) 125 mV

We give an example to illustrate how the BDD of a logic function can be implemented using the circuits that have been described here. Figure 9A shows an arbitrary 3-input logic function and its corresponding BDD. Figure 9B shows how the BDD is implemented using arrays of coupled nanodots.

The output of the BDD tree is captured through a load capacitance. The paths of the BDD tree which connect the output and the logic value 1 are implemented as coupled nanodot-based circuit paths which connect the load capacitance and the supply voltage VDD. The paths of the BDD tree which connect the output and logic values 0 are implemented as circuit paths which connect the load capacitance and the ground. Based on the input the load capacitance is charged to V_{DD} when the output evaluates to logic value 1, or is discharged to ground when the output evaluates to logic value 0. The inputs to the BDD circuit and the corresponding output are shown in Figure 10.

III. Understanding Energy-Delay Characteristics of Set Devices

In the previous section we have discussed the transconductance characteristics of room temperature SET devices and various ways of biasing the devices to operate them as switches. We also discussed how coupled nanodots can be used to implement BDD based circuits. It is useful to understand the energy-delay trade-off characteristics of these circuits as the supply voltage is scaled. In this section we consider this important aspect of circuit design using SET devices.

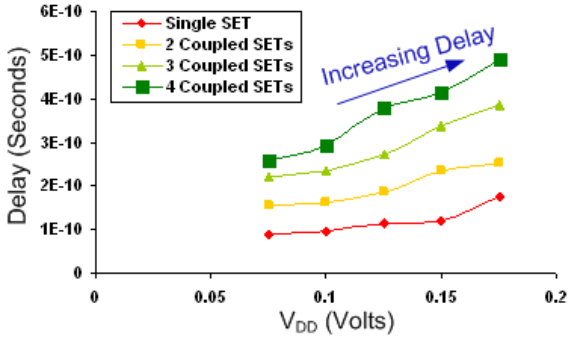

FIGURE 11 – Delay of SET Devices with Supply Voltage V_{DD}

Figure 11 shows the delay trend with supply voltage scaling for different SET devices (driving a load capacitance of 10aF). We observe a trend where the delay of the device increases as supply voltage is increased.

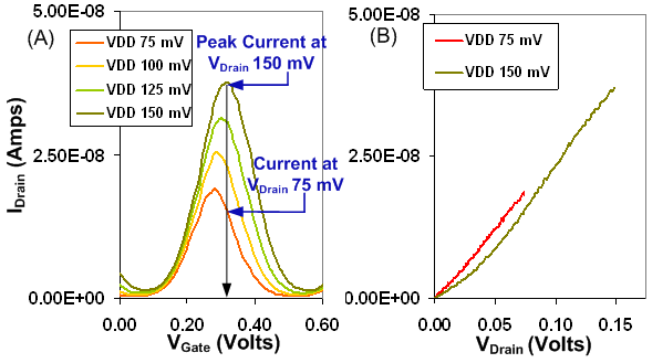

FIGURE 12 – (A) Transconductance and (B) Output Conductance of a 3-Terminal SET Device for Different V_{DD}

In order to understand why we see such a trend, we observe from the transconductance graph of a single SET device shown in Figure 12A that, the peak current increases as V_{DD} increase. As a result we would expect this increase in peak current to translate to higher performance. However, as Figure 12B shows, for a larger V_{DD}, the fraction of the drain voltage away from the peak current also increases. Consequently the

second phenomenon dominates causing an increase in delay.

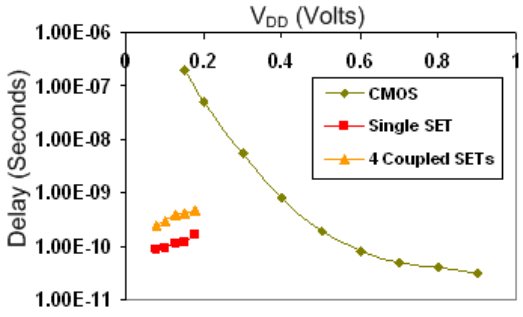

FIGURE 13 – Comparison of Delay of 32 nm CMOS with Delay of SET Devices

We also compare the Energy and Delay trends of an SET device with those of a CMOS device. Figure 13 compares the delay of 32nm CMOS (V_{TH} 0.16 Volts) with that of SET devices. The CMOS device is loaded with one gate capacitance (30 aF) and the SET devices are loaded with a load capacitance of 10 aF. As the supply voltage of the CMOS device is lowered, the CMOS device enters into its sub-threshold region and the delay increases exponentially. However, the delay of the SET becomes lower because of the trend explained above.

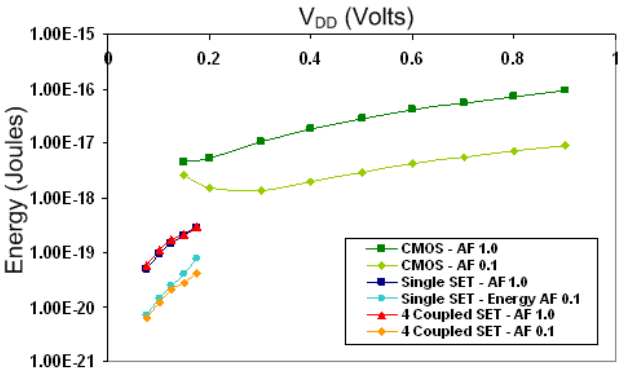

FIGURE 14 – Comparison of Energy of 32 nm CMOS with Energy of SET Devices

Figure 14 shows the energy trend with supply voltage scaling for SET and CMOS devices at two different activity factors (AF 1.0 and AF 0.1). As supply voltage is decreased, CMOS shows a trend of increasing energy once it enters the sub-threshold region due to domination by leakage energy. However, SET devices are not leakage energy dominated. Leakage energy is kept very low due to the high resistance tunnel barriers. As a result SET devices show a trend of decreasing energy as supply voltage is scaled down.

From these trends it can be argued that for SET devices it may be most advantageous to scale down voltages. However, there is a limit as to how low the supply voltage can be scaled down. Since we use SET devices operating at room temperature to build digital logic circuits which require two clearly distinguishable output regions representing Boolean 0 and 1, we need two noise margins which are at least kT wide to distinguish between a 0 and a 1 output. As a result the supply voltage V_{DD} cannot be scaled below 50 mV (2kT) at room temperature.

IV. Conclusion

As the energy-delay trends in section III show, it is advantageous to operate SET devices at low voltages. SET devices operated by applying input voltages as described in Section II-B and Section II-C show a trend of decreasing delay with decreasing supply voltage. Also, SET devices are not leakage dominated at low supply voltages and show a trend of decreasing energy with decreasing supply voltage. As a result of these trends it is most advantageous to operate SET devices at as low a supply voltage as noise margins permit.

Due to these energy-delay trade-off characteristics exhibited by SET devices operating at room temperature we believe that it may be advantageous to utilize SET devices to implement low energy circuits operating at low supply voltages.

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