Flicker-Noise Improvement in 100-nm L_g $Si_{0.50}Ge_{0.50}$ Strained Quantum-Well Transistors Using Ultrathin Si Cap Layer

Feng Li, Se-Hoon Lee, Zhao Fang, Prashant Majhi, Qiming Zhang, Sanjay K. Banerjee, *Fellow, IEEE*, and Suman Datta, *Senior Member, IEEE*

***Abstract*—This letter presents a record low flicker-noise spectral density in biaxial compressively strained p-channel 100-nm L_g $Si_{0.50}Ge_{0.50}$ quantum-well FETs (QWFETs) with ultrathin Si (∼2 nm) barrier layer and 1-nm EOT hafnium silicate gate dielectric. The normalized power spectral density of I_d fluctuations (S_{Id}/I_d^2) in $Si_{0.50}Ge_{0.50}$ QWFETs exhibits significant improvement by ten times over surface channel unstrained Si pMOSFETs at high V_g due to strong confinement of holes within the high-mobility QW and strong quantization in the ultrathin Si barrier layer enabled by low-thermal-budget device processing. The noise behavior in strained QW devices is found to evolve from being correlated mobility fluctuation dominated across most of V_g range to being Hooge mobility fluctuation dominated at very high V_g.**

***Index Terms*—Flicker noise, hole confinement, SiGe quantum-well FETs (QWFET), surface channel MOSFETs.**

I. INTRODUCTION

NOVEL channel architectures incorporating strained quantum wells are expected to enhance the performance and energy efficiency of future CMOS transistors [1]. High-performance short-channel PMOS transistors have been demonstrated using biaxial compressively strained SiGe quantum well with Ge mole fraction $\geq 50\%$ [2], [3]. As logic transistors continue to scale following Moore's law, the more than Moore initiative calls for functional diversification in addition to scaling advances. One such application is the direct integration of magnetoelectric sensors with CMOS transistors for developing chip-scale ultrasensitive magnetometers [4]. Since sensitivity depends on the input gate noise of the readout transistor amplifier, the quantum-well FET (QWFET) architecture is a promising option toward improving sensor performance. Superior noise performance for Si/$Si_{1-x}Ge_x$ pMOSFETs has been reported by several groups [5]–[10] with varying Ge mole fractions and Si cap layer thicknesses, albeit at long gate lengths (L_g). However, most report loss of advantage at high V_g due to surface channel formation in the Si cap layer. Thinning of Si cap layer to prevent parasitic channel formation leads to increased D_{it}, which, in turn, increases noise [11]. In this letter, we report on record low flicker-noise characteristics in strained p-channel $Si_{0.50}Ge_{0.50}$ QWFETs with ultrathin Si (∼2 nm) cap layer, 1-nm EOT $HfSiO_x$ high-κ dielectric/metal gate stack and 100-nm L_g. The noise improvement is demonstrated at high V_g due to the absence of parasitic surface channel formation in the Si cap layer resulting from 50% Ge concentration and minimal Ge out-diffusion stemming from low-thermal-budget processing [3]. The noise characteristics are comparable to Si near threshold due to the influence of the interface state density D_{it}, which is maintained at an acceptable level with 2-nm-thick Si cap layer.

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F. Li, Z. Fang, Q. Zhang, and S. Datta are with the Department of Electrical Engineering, The Pennsylvania State University, PA 16802 USA (e-mail: sdatta@eng.psu.edu).

S.-H. Lee is with International Sematech, Austin, TX 78741 USA, and also with The University of Texas at Austin, TX 78758 USA.

P. Majhi is with International Sematech, Austin, TX 78741 USA.

S. K. Banerjee is with The University of Texas at Austin, TX 78758 USA.

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II. FLICKER-NOISE CHARACTERISTICS

$Si_{0.50}Ge_{0.50}$ p-channel QWFETs were fabricated at Sematech using a metal gate first CMOS flow [3]. A 5-nm-thick epitaxial $Si_{0.50}Ge_{0.50}$ layer was pseudomorphically grown on Si substrate with a 2-nm-thick Si cap using ALD $HfSiO_x$ dielectric. The millisecond annealing of source–drain junctions was used to limit the thermal budget and suppress the diffusion of Ge into Si cap layer and gate stack [3]. Unstrained surface channel Si pMOSFETs were also fabricated as control samples to quantify the mobility and noise improvement. Noise measurements were performed at room temperature on QWFETs and pMOSFETs with gate length and width of 100 nm and 10 μm, respectively, using SRS 570 low-noise preamplifier and HP35670A dynamic signal analyzer. Fig. 1 shows the measured effective hole mobility in the $Si_{0.50}Ge_{0.50}$ QWFET compared with the Si MOSFET versus inversion hole density along with a schematic of the QWFET device structure. The hole mobility in strained $Si_{0.50}Ge_{0.50}$ QWFETs improves by $2\times(100\%)$ compared to Si over a wide range of hole density. A six-band $k\cdot p$ simulation predicts a hole effective mass reduction by five times from the strain-induced warping of the heavy hole band along the $\langle 110\rangle$ direction. The lower than expected enhancement, at low field, is due to Coulomb scattering caused by higher D_{it} away from the valence band edge, as shown by charge pumping measurements in Fig. 1(c). Fig. 2(a) and (b) shows the measured room temperature normalized power spectral density (NPSD) (S_{Id}/I_d^2) of the drain current (I_d) fluctuations in both the devices in the linear region of operation as a function of gate overdrive. The strained $Si_{0.50}Ge_{0.50}$ QWFETs show similar drain current noise spectral density at low gate overdrive but almost an order of magnitude reduction compared to the unstrained Si control devices, at a high gate overdrive of 1.0 V. The series resistance

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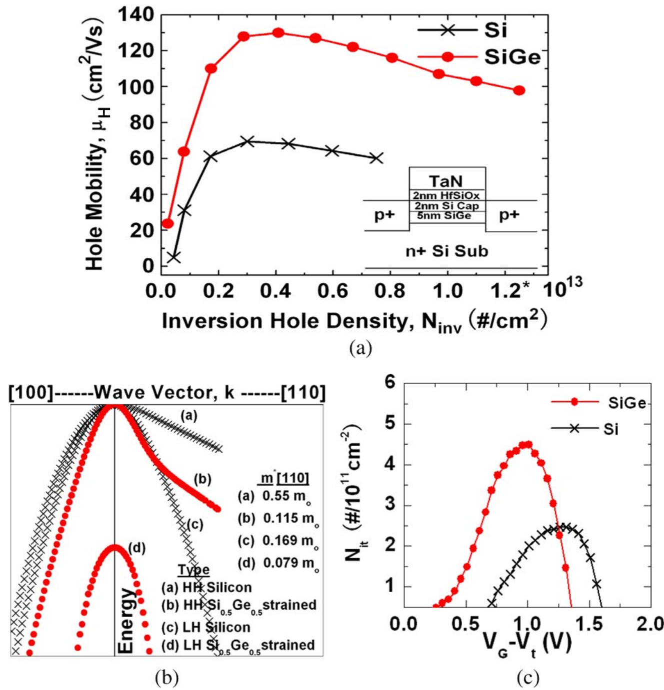

Fig. 1. (a) Measured effective hole mobility as a function of hole density for p-channel $Si_{0.50}Ge_{0.50}$ QWFETs and Si MOSFETs. (b) Six-band $k \cdot p$ simulation of heavy and light hole energy dispersions for strained $Si_{0.50}Ge_{0.50}$ QW and unstrained silicon. (c) Measured interface state profile via charge pumping measurements.

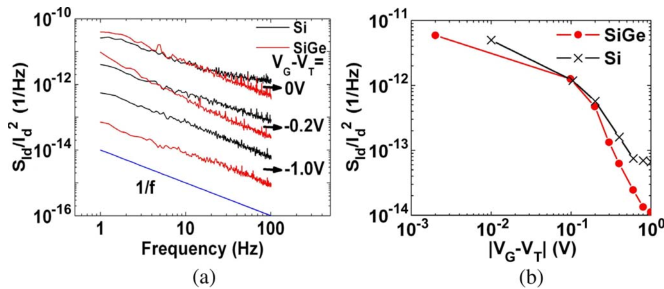

Fig. 2. (a) NPSD of I_d fluctuations (S_{Id}/I_d^2) in unstrained Si pMOSFETs and $Si_{0.50}Ge_{0.50}$ strained QWFETs as a function of gate overdrive voltage. The drain voltage is -50 mV, and $L_g = 100$ nm. (b) NPSD of $Si_{0.50}Ge_{0.50}$ strained QWFETs compared against Si pMOSFETs, showing almost ten times improvement in noise spectral density at 10 Hz, particularly at high gate voltage. The drain voltage is -50 mV.

contributions to the total on-resistance are 33% and 20% for the 100-nm L_g Si and $Si_{0.50}Ge_{0.50}$ devices, respectively, thereby not playing a dominant role on noise characteristics even at high overdrive. This is shown in Fig. 2(b), where both the devices show strong V_{gs} dependence, indicating that the noise spectral density is dominated by channel resistance except for the very few last points for the Si case when the noise spectral density flattens off, showing a series resistance effect.

Table I summarizes the normalized input referred noise spectral density S_{VG} and the output drain current noise spectral density S_{Id}/I_d^2, as a function of Ge%, Si_xGe_{1-x} quantum-well thickness, Si cap thickness, dielectric, vertical electric field, and the maximum thermal budget related to device processing. We conclude that the record flicker-noise performance of our devices stems from a combination of high Ge concentration (50%) without strain relaxation, minimal Ge out-diffusion [3], and the thinnest (2 nm) possible silicon cap preventing parasitic channel formation at higher electric field—all enabled by the lowest thermal budget processing attempted to date (by activating the source drain using millisecond flash anneal). We show that our own fabricated devices with higher Ge concentration (75%) processed with higher thermal budget result in higher noise current characteristics due to the out-diffusion of Ge into the cap and dielectric layer (see Table I).

III. Noise Modeling

To understand the physical mechanisms determining the noise performance, we studied the evolution of the equivalent input gate voltage noise (S_{VG}) as a function of the gate bias (Fig. 3) averaged over five devices. The input gate voltage noise caused by carrier number fluctuation (CNF) and mobility fluctuation correlated to number fluctuations [correlated mobility fluctuation (CMF)] was modeled by $S_{\nu g} = S_{\nu fb}[1 - \alpha\mu_0 C_{\text{gate}}(V_g - V_t)]^2$, where $S_{\nu fb} = 3.8 \times 10^{-14}$ (8×10^{-14}) V^2/Hz, $C_{\text{gate}} = 1.9$ (2.0) μF/cm^2, $\mu_o = 153$ (64) $cm^2 \cdot V^{-1} \cdot s^{-1}$, $\alpha = 4 \times 10^3$ (1.5×10^4) $V \cdot s \cdot C^{-1}$, and the Coulomb scattering parameter are used for the strained $Si_{0.50}Ge_{0.50}$ QWFETs (and Si pMOSFETs). The negative sign in front of the Coulomb scattering parameter indicates the presence of acceptor traps which become neutral by trapping holes, resulting in a negative correlation between the hole mobility and carrier fluctuation. At high gate bias, the input gate voltage noise is explained by the Hooge mobility fluctuation

$$S_{\nu g} = \frac{q\alpha_H}{WLfC_{\text{gate}}}(V_g - V_t)\left[1 + \theta_1(V_g - V_t) + \theta_2(V_g - V_t)^2\right]^2$$

where the Hooge parameter $\alpha_H = 10^{-8}$ (10^{-7}) [Fig. 4(b)] and the mobility attenuation coefficients $\theta_1 = 0.4621$ and $\theta_2 = 0$ $(\theta_1 = 0.6;\ \theta_2 = 2)$ for $Si_{0.50}Ge_{0.50}$ QWFETs (and Si pMOSFETs). Our results show important differences between the strained $Si_{0.50}Ge_{0.50}$ QWFETs and the surface channel Si pMOSFETs. The input gate noise in Si pMOSFETs is primarily determined by the mobility-fluctuation-dominated mechanism. In strained $Si_{0.50}Ge_{0.50}$ QWFETs, the input gate noise is reduced by an order of magnitude and limited by the CMF effect up to very high gate overdrive, where the Hooge mobility fluctuation eventually dominates. Fig. 4(a) shows the normalized drain current noise against the drain current for $Si_{0.50}Ge_{0.50}$ QWFETs and Si MOSFETs from subthreshold to strong inversion. At below threshold, for $Si_{0.50}Ge_{0.50}$ QWFETs, the CNF dominates due to interface traps present at the high-κ and ultrathin silicon interface, whereas at above threshold, the CMF dominates $(\sim 1/I_d^2)$. The Hooge mobility fluctuation becomes relevant at very high V_g, but the absolute value still remains low compared to the Si pMOSFETs [Fig. 4(b)]. This result is markedly different from Jiang *et al.* [10], who reported degradation in the noise characteristics in their dual quantum-well $Si_{0.60}Ge_{0.40}$ devices at high V_g due to the formation of a parasitic surface channel in the Si layer. In our strained $Si_{0.50}Ge_{0.50}$ QWFETs, we prevent the formation of parasitic surface channel in the Si layer at high V_g as follows: 1) by aggressively scaling and preserving the top silicon barrier layer to less than 2 nm; 2) by higher Ge mole fraction (50%) in the QW, leading to better confinement of holes; and c) by using millisecond flash anneal activation of dopants with no Ge out-diffusion as confirmed by EDX studies [3]. A previous attempt in integrating ultrathin Si cap with strained SiGe or SiGeC quantum well resulted in degraded noise due to the consumption of the Si cap

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TABLE I
NOISE BENCHMARK TABLE OF CURRENT Si/SiGe DEVICES

	Ge%	t_{SiGe} (nm)	t_{Sicap} (nm)	t_{ox} (nm)	$E=\|V_g-V_t\|/t_{ox}$ (V/cm)	S/D activation anneal	S_{vg} *L * W (um^2*V^2/Hz) @10Hz	S_{Id}/I_d^2 * L *W (um^2/Hz) @10Hz
Si (this work)	N/A	N/A	N/A	2 ($HfSiO_x$)	5×10^6	1100C Flash Anneal	6.02×10^{-13}	6.66×10^{-14}
uniaxial strained Si [12]	25% S/D		N/A	3.6 ($HfSiO_x$)	10^6	1050C spike anneal	1.5×10^{-10}	3×10^{-10}
SiGe (this work)	50	5	2	2 ($HfSiO_x$)	5×10^6	1100C Flash Anneal	2.3×10^{-14}	1.12×10^{-14}
SiGe (this work)	75	3	3	2 ($HfSiO_x$)	5×10^6	RTA S/D Anneal 10s	6.16×10^{-14}	2.72×10^{-14}
SiGe[7]	20	20	7	170 (SiO_2)	0.2×10^6	750C 0.5h Anneal	10^{-7}	10^{-9}
			2.1				2.03×10^{-11}	3×10^{-11}
SiGe[9]	20	20	4.7	7 (SiO_2)	10^6	-	3.75×10^{-11}	4.5×10^{-11}
			6.4				10^{-10}	9×10^{-11}
SiGe[11]	10	20	0	3 (SiO_2)	3.3×10^6	spike anneal 1050 C	-	9.6×10^{-9}
SiGe[13]	25	-	10	(SiO_2)	-	-	-	10^{-12}
SiGe[14]	20	-	0	5 (Al_2O_3)	2×10^6	RTA Anneal 930C 10s	10^{-9}	2×10^{-10}
SiGe[15]	30	-	5	3 (SiO_2)	3.3×10^6	-	-	7×10^{-11}

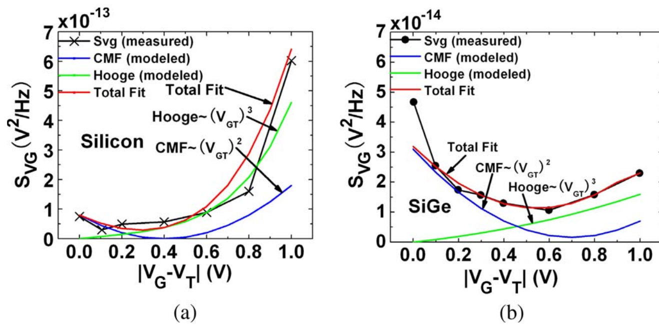

Fig. 3. Equivalent input gate voltage noise characteristics $S_{VG}=S_{Id}/g_m^2$ in (a) unstrained Si pMOSFETs and (b) $Si_{0.50}Ge_{0.50}$ strained QWFETs as a function of gate overdrive voltage. The drain voltage is -50 mV, and $L_g=100$ nm. The models used are CMF model and Hooge mobility fluctuation model.

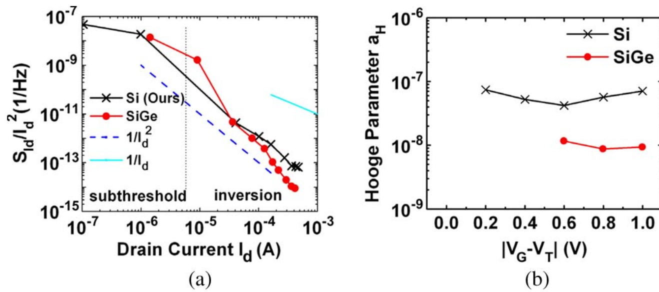

Fig. 4. (a) Normalized drain noise characteristics S_{Id}/I_d^2 in $Si_{0.50}Ge_{0.50}$ strained QWFETs and Si MOSFETs. The drain voltage is -50 mV, and $L_g=100$ nm. (b) Extracted Hooge parameter versus gate overdrive voltage.

during SiO_2 gate stack processing and the disruption of epiquality in the channel from high temperature device processing [11].

IV. CONCLUSION

In summary, we have shown ten times reduction in low-frequency flicker-noise characteristics in strained p-channel high-κ metal gate $Si_{0.50}Ge_{0.50}$ QWFETs with ultrathin (< 2 nm) Si cap layer, low D_{it}, and 1-nm EOT high-κ gate stack compared to surface channel unstrained Si MOSFETs. This improvement persists at high V_g, as the holes are well confined within the $Si_{0.50}Ge_{0.50}$ quantum well and the preservation of the ultrathin Si cap layer due to low-thermal-budget processing.

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