

On Enhanced Miller Capacitance Effect in Interband Tunnel Transistors

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Abstract—We compare the transient response of double-gate thin-body-silicon interband tunnel field-effect transistor (TFET) with its metal–oxide–semiconductor field-effect transistor counterpart. Due to the presence of source side tunneling barrier, the silicon TFETs exhibit enhanced Miller capacitance, resulting in large voltage overshoot/undershoot in its large-signal switching characteristics. This adversely impacts the performance of Si TFETs for digital logic applications. It is shown that TFETs based on lower bandgap and lower density of states materials like indium arsenide show significant improvement in switching behavior due to its lower capacitance and higher ON current at reduced voltages.

Index Terms—Density of states (DOS), InAs, metal–oxide–semiconductor field-effect transistors (FETs) (MOSFETs), Miller capacitance, silicon, tunnel FETs (TFETs).

I. INTRODUCTION

INTERBAND tunnel field-effect transistors (TFETs) with a gate-modulated Zener tunnel junction at the source have recently attracted a great deal of interest [1]–[7]. The major advantage of TFETs in comparison with the metal–oxide–semiconductor field-effect transistors (MOSFETs) is that the reverse biased tunnel junction in the former eliminates the high-energy tail present in the Fermi–Dirac distribution of the valence band electrons in the p+ source region and allows sub- kT/q subthreshold slope device operation near the OFF state. This allows TFETs to achieve, in principle, much higher $I_{ON}-I_{OFF}$ ratio over a specified gate voltage swing compared to MOSFETs, making the former attractive for low- V_{DD} operation.

To date, the published work on TFETs has focused on device level dc transfer characteristics and not on circuit level ac switching performance. In this letter, for the first time, we compare the large-signal switching behavior of silicon-based TFETs with MOSFETs in an inverter configuration using a 2-D numerical device simulator [8]. We reveal that the TFET performance is limited by the enhanced gate-to-drain Miller capacitance (C_{gd}) effect which leads to significant voltage

overshoot and undershoot in its transient response and explain its physical origin from basic TFET device physics. It is shown that the high voltage overshoot/undershoot in TFET inverter characteristics can be mitigated through a reduction in C_{gd} -dominated Miller effect through capacitive loading of the TFET inverter at the expense of increased inverter delay. A promising way to circumvent this problem is to go to lower bandgap materials and lower density of states (DOS) material such as InAs, which provide reduced source side tunnel barrier and reduced Miller capacitance, respectively.

II. CAPACITANCE VOLTAGE CHARACTERISTICS

Fig. 1(a) shows the device structure used for this letter and the dc $I_{DS}-V_{GS}$ characteristics for Si MOSFET and TFET. Both TFET and MOSFET have a double-gate structure with a gate length (L_G) of 30 nm, 2.5-nm-thick HfO_2 gate dielectric, and an intrinsically doped body which is 7 nm thick. Gaussian doping profiles with a peak density of 10^{20} cm^{-3} for Si TFET/MOSFET and 10^{19} cm^{-3} for InAs TFET and doping gradients of 2 nm/dec with an overlap of 2 nm on each side are used for the source/drain regions. The interband tunneling current in the TFET depends on the potential profile along the entire path between two points connected by tunneling. In contrast to the local tunneling models commonly used [9], [10], we use a nonlocal tunneling model [11] which reflects the real space carrier transport through the barrier, taking into account the potential profile along the entire tunneling path. The band edge tunneling masses of $m_c = 0.5m_0$ and $m_v = 0.65m_0$ (where m_0 is the electron rest mass) for silicon and $m_c = m_v = 0.023m_0$ for InAs are used to calculate the local imaginary wavenumbers within the forbidden gap. Kane's two-band model is then used to calculate the tunneling probability. The results presented here are obtained through a drift–diffusion simulation, where the Poisson and carrier continuity equations are solved self-consistently. An interband tunneling component is added to the carrier continuity equation as a generation–recombination (G-R) term. The G-R term contains adjustable scaling factors g_c and g_v kept at values equal to 0.1 and 0.4, respectively, for Si and equal to 1 for InAs, which set the effective Richardson constant. Fig. 2(a) shows the excellent fit of our nonlocal tunneling model with the experimental data from Fair and Wivell [13] for a reverse biased Si Zener diode.

Fig. 1(b) and (c) shows the capacitance voltage characteristics of silicon-based MOSFET with TFETs. For capacitance simulation, a sinusoidal steady-state analysis (S^3A) technique

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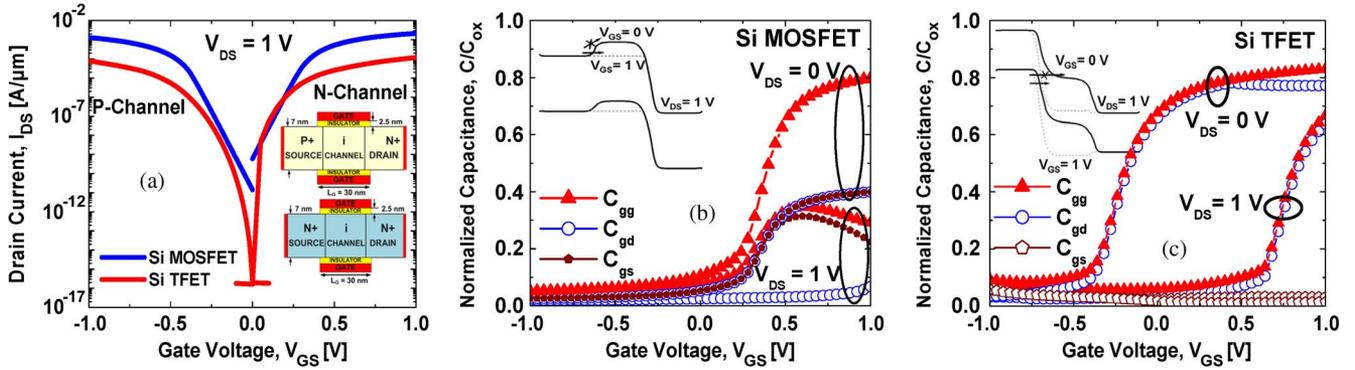


Fig. 1. (a) DC I_{DS} - V_{GS} characteristics for p-type and n-type Si TFET and MOSFET. Inset shows the device schematic; the details are explained in the text. (b) Capacitance-voltage characteristics showing the gate (C_{gg}), gate-to-source (C_{gs}), and gate-to-drain (C_{gd}) capacitances as a function of gate-to-source voltage V_{GS} for (b) Si MOSFET and (c) Si TFET.

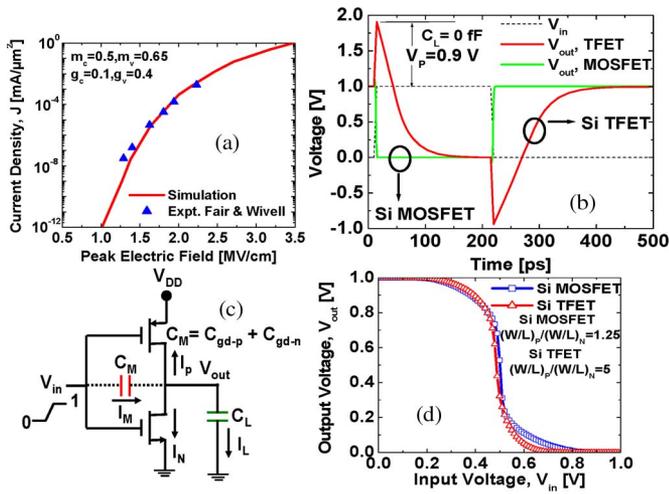


Fig. 2. (a) Simulation of Si Zener diode fitted to experimental data from Fair and Wivell [13]. (b) Transient response characteristics of silicon TFET- and MOSFET-based inverters. The load capacitance C_L is set to zero in this simulation. (c) Inverter schematic showing the origin of the overshoot/undershoot in TFET. (d) Si TFET and Si MOSFET inverter VTCs.

[12] is employed, which applies a sinusoidal voltage perturbation of infinitesimal amplitude to the device terminals in the frequency domain and monitors the terminal currents to yield the admittance matrix containing the capacitance and conductance. The insets in Fig. 1(b) and (c) depict the energy band diagrams for MOSFET and TFET. In the OFF state ($V_{GS} = 0$ V; $V_{DS} = 1$ V), the conduction in MOSFET is limited by the source side p-n junction barrier which prevents the thermionic emission of carriers. In the ON state ($V_{GS} = 1$; $V_{DS} = 1$), the source barrier is negligible, enabling over the barrier thermionic emission. In contrast, TFETs operate by tunneling of carriers from the valence band in the source to the conduction band in the channel. In the OFF state ($V_{GS} = 0$ V; $V_{DS} = 1$ V), transmission probability is low due to the thick depletion region associated with the source to channel tunnel junction, resulting in very low OFF currents. In the ON state ($V_{GS} = V_{DS} = 1$ V), the tunnel barrier shrinks, allowing carriers to tunnel through. Since the TFET ON current is limited by the interband quantum-mechanical tunneling compared to thermionic emission over the barrier, the ON current in silicon TFETs is much lower than MOSFETs. This results in very low gate-to-source capacitance (C_{gs}) in TFETs in the ON state ($V_{GS} = V_{DS} = 1$ V) compared

to MOSFETs [Fig. 1(b) and (c)]. Furthermore, there is very little potential drop between the channel and the drain in TFETs compared to the large reverse bias that exists between the channel and the drain in MOSFETs, as observed from the band diagrams. This results in large gate-to-drain capacitance (C_{gd}) or Miller capacitance in TFETs compared to MOSFETs. It is worthwhile to note that the gate capacitance C_{gg} is entirely reflected by the gate-to-drain capacitance C_{gd} in TFETs under all bias conditions in stark contrast to MOSFETs, where both C_{gs} and C_{gd} contribute. The C_{gd} dominates even near the OFF-state condition in TFETs at $V_{GS} = V_{DS} = 0$ V, since the source-to-channel barrier resistance is large while the channel-to-drain barrier resistance is low. The latter is set by the combination of gate electrode work function (band edge n-type work function gate metal) and 10^{15} cm $^{-3}$ of near intrinsic channel doping. This results in low C_{gs} and high C_{gd} for TFETs at low V_{GS} . On the contrary, in MOSFETs at $V_{GS} = V_{DS} = 0$, the potential barriers for both the source-to-channel and drain-to-channel p-n junctions are approximately equal to $E_g/2$ set by the gate electrode work function (mid-gap workfunction metal) and 10^{15} cm $^{-3}$ of p-type channel doping. This results in both C_{gs} and C_{gd} being equal but small for MOSFETs. This enhanced Miller capacitance (C_{gd}) effect in TFETs over MOSFETs, coupled with low ON currents, has important implications for their large-signal transient response.

III. IMPACT ON TRANSIENT RESPONSE

Fig. 2(b) shows the transient response of silicon TFETs with MOSFET in an inverter configuration to an input ramp voltage (1-V peak voltage and 5-ps rise time). TFETs exhibit very large output voltage overshoot and undershoot peaks when the input voltage pulse begins to transition from 0-1 and 1-0 V, respectively. The overshoot peak arises primarily due to the large C_{gd} (Miller capacitance) in TFETs compared to MOSFETs. The origin of this voltage overshoot is depicted in the circuit schematic of Fig. 2(c), where the input transient voltage is directly coupled to the output node by the high C_{gd} of the load TFET operating in the linear region. The output voltage of the TFET inverter stays at a very high value V_{MAX} at the end of the input 0-1 transition. This continues to keep the pull-down n-TFET in deep saturation (low C_{gd}) while the pull-up p-TFET remains in the linear region (high C_{gd}). Even as the output

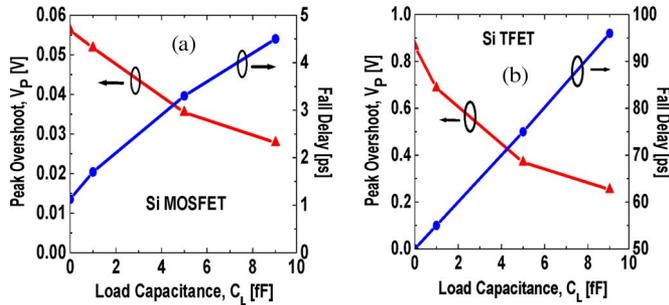


Fig. 3. (a) Peak overshoot and fall time delay as functions of load capacitance C_L for Si (a) MOSFET and (b) TFET inverters. Fall time delay is measured as the time interval between 50% of input (V_{in}) and 50% of output (V_{out}) voltages of the inverter in Fig. 2.

voltage starts transitioning from its peak overshoot value, the C_{gd} for p-TFET decreases while that for n-TFET increases, thereby maintaining a high Miller capacitance all throughout the transient. Fig. 2(d) shows the voltage transfer characteristics of the correctly sized Si-based TFET and MOSFET inverters. In TFETs, the extent of this overshoot can be calculated from the following charge conservation equation [14]:

$$\begin{aligned} C_L V_{MAX} + C_M (V_{MAX} - V_{DD}) &= (C_M + C_L) V_{DD} \\ V_P &= V_{MAX} - V_{DD} \\ &= \frac{C_M}{C_M + C_L} V_{DD} \end{aligned} \quad (1)$$

where C_M is the Miller capacitance connecting the input and output of the inverter comprising the gate-to-drain capacitance of both p-TFET and n-TFET, C_L is the load capacitance external to the device, V_{MAX} is the maximum voltage to which the output voltage rises, V_P is the peak value of the overshoot, and V_{DD} is the supply voltage. This equation clearly shows the impact of higher Miller capacitance on the peak overshoot voltage in TFETs. The effect of this Miller capacitance in TFETs is significantly reduced by loading the TFET inverter with an appropriate load capacitance C_L . However, this leads to degraded fall time delays for TFET. Fig. 3(a) and (b) shows the tradeoff between peak overshoot voltage and fall time delay (time interval between 50% input and 50% output) in silicon MOSFET and TFET inverters as a function of C_L . The fall time delay in silicon TFET inverter is worse by an order of magnitude compared to MOSFET due to the low ON current in Si TFETs (Si TFET $I_{ON} \sim 60 \mu\text{A}/\mu\text{m}$; Si MOSFET $\sim 1.13 \text{ mA}/\mu\text{m}$) and higher C_{gd} . This warrants the need for exploration of an alternate solution, which would fundamentally limit the gate-to-drain capacitance in TFETs and reduce the Miller capacitance effect.

Low bandgap and low effective mass materials such as indium arsenide (InAs) are promising for TFET due to higher tunneling rate through the source side tunnel barrier and higher ON current ($82 \mu\text{A}/\mu\text{m}$) at $V_{DD} = 0.25 \text{ V}$ [7]. Furthermore, the reduced DOS in InAs limits the gate-to-drain capacitance and mitigates the enhanced Miller capacitance effect [Fig. 4(a)]. This suppresses the voltage overshoot/undershoot in the transient switching characteristics and improves the inverter fall time delay significantly by ~ 45 times to 1.1 ps [Fig. 4(b)] from 1.4 times increase in ON current, eight times reduction in C_{gd} , and four times reduction in V_{DD} .

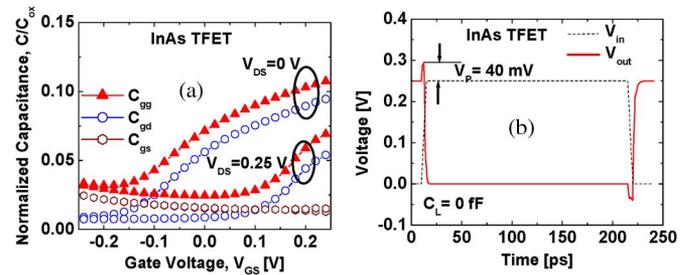


Fig. 4. (a) Capacitance–voltage characteristics of an InAs TFET showing the gate (C_{gg}), gate-to-source (C_{gs}), and gate-to-drain (C_{gd}) capacitances as a function of gate-to-source voltage V_{GS} . Note that the supply voltage is $V_{DD} = 0.25 \text{ V}$. (b) Transient response characteristics of an InAs TFET inverter. InAs TFET exhibits a significantly smaller voltage overshoot/undershoot due to smaller Miller capacitance and higher I_{ON} compared to Si TFETs. The fall time delay is improved significantly to 1.1 ps.

IV. CONCLUSION

In summary, we have shown that the transient performance of TFET inherently suffers from an enhanced Miller capacitance, resulting in large output voltage overshoot/undershoot and increased inverter delay. Following the charge conservation principle, it has been shown that V_P can be reduced by capacitive loading of the TFET inverter at the expense of increased fall time delay. A more promising approach is identified in an InAs-based TFET due to its higher ON current and lower Miller capacitance at reduced supply voltages, stemming from its reduced DOS.

REFERENCES

- [1] W. M. Reddick and G. A. J. Amarantunga, "Silicon surface tunnel transistor," *Appl. Phys. Lett.*, vol. 67, no. 4, pp. 494–496, Jul. 1995.
- [2] K. K. Bhuiwarka, S. Sedlmaier, A. K. Ludsteck, C. Toksdorf, J. Schulz, and I. Eisele, "Vertical tunnel field-effect transistor," *IEEE Trans. Electron Devices*, vol. 51, no. 2, pp. 279–282, Feb. 2004.
- [3] J. Appenzeller, Y. M. Lin, J. Knoch, and P. Avouris, "Band-to-band tunneling in carbon nanotube field-effect transistors," *Phys. Rev. Lett.*, vol. 93, no. 19, pp. 196 805-1–196 805-3, Nov. 2004.
- [4] W. Y. Choi, B.-G. Park, J. D. Lee, and T.-J. K. Lui, "Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec," *IEEE Electron Device Lett.*, vol. 28, no. 8, pp. 743–745, Aug. 2007.
- [5] V. Nagavarapu, R. Jhaveri, and J. C. S. Woo, "The tunnel source (PNPN) n-MOSFET: A novel high performance transistor," *IEEE Trans. Electron Devices*, vol. 55, no. 4, pp. 1013–1019, Apr. 2008.
- [6] P. F. Wang, "Complementary tunneling FETs (CTFET) in CMOS technology," Ph.D. dissertation, Tech. Univ. München, Munich, Germany, 2003.
- [7] S. Mookerjee and S. Datta, "Comparative study of Si, Ge and InAs based steep subthreshold slope tunnel transistors for 0.25 V supply voltage logic applications," in *Proc. 66th Device Res. Conf.*, Jun. 2008, pp. 47–48.
- [8] TCAD Sentaurus Device Manual, Synopsys, Inc., Mountain View, CA, 2007, Release: Z-2007.03.
- [9] G. A. M. Hurkx, D. B. M. Klaassen, and M. P. G. Knuyvers, "A new recombination model for device simulation including tunneling," *IEEE Trans. Electron Devices*, vol. 39, no. 2, pp. 331–338, Feb. 1992.
- [10] A. Schenk, "Rigorous theory and simplified model of band-to-band tunneling in silicon," *Solid State Electron.*, vol. 36, no. 1, pp. 19–34, Sep. 1992.
- [11] M. Jeong, P. M. Solomon, and S. E. Laux, "Comparison of raised and Schottky source/drain MOSFETs using a novel tunneling contact model," in *IEDM Tech. Dig.*, Dec. 1998, pp. 733–736.
- [12] S. E. Laux, "Techniques for small-signal analysis of semiconductor devices," *IEEE Trans. Electron Devices*, vol. ED-32, no. 10, pp. 2028–2037, Oct. 1985.
- [13] R. B. Fair and H. W. Wivell, "Zener and avalanche breakdown in As-implanted low voltage Si n-p junctions," *IEEE Trans. Electron Devices*, vol. ED-23, no. 5, pp. 512–518, May 1976.
- [14] M. Shoji, *CMOS Digital Circuit Technology*. Englewood Cliffs, NJ: Prentice-Hall, 1988, ch. 4, pp. 189–190.