Effective Capacitance and Drive Current for Tunnel FET (TFET) CV/I Estimation

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***Abstract*—Through mixed-mode device and circuit simulation, this paper provides an estimate of the effective output capacitance (C_{EFF}) and drive current (I_{EFF}) for delay ($\tau_f = 0.69 R_{\mathrm{sw}} C_{\mathrm{EFF}}$, where $R_{\mathrm{sw}} = V_{\mathrm{DD}}/2\ I_{\mathrm{EFF}}$) estimation of unloaded tunnel field-effect transistor (TFET) inverters. It is shown that unlike MOSFET inverters, where C_{EFF} is approximately equal to the gate capacitance (C_{gg}), in TFET inverters, the output capacitance can be as high as 2.6 times the gate capacitance. A three-point model is proposed to extract the effective drive current from the real-time switching current trajectory in a TFET inverter.**

***Index Terms*—Indium arsenide (InAs), Miller capacitance, MOSFETs, switching current trajectory, tunnel field-effect transistors (TFETs).**

I. Introduction

Recently, interband tunnel field-effect transistors (TFETs) have been extensively investigated [1]–[5] due to its potential for sub-kT/q subthreshold slope device operation, thus enabling supply voltage reduction for low-power logic applications. Recent work has been done to benchmark the intrinsic delay of the TFETs with MOSFETs. While $C_{\mathrm{ox}} V_{DD}/I_{\mathrm{ON}}$, where C_{ox} is the oxide capacitance, is used in [6], $C_{\mathrm{gg}} V_{\mathrm{DD}}/I_{\mathrm{ON}}$, where C_{gg} is the total gate capacitance of the TFET including the quantum capacitance of the channel, is used in [7]. Reference [8] uses the metric $(Q_{\mathrm{ON}} - Q_{\mathrm{OFF}})/I_{\mathrm{ON}}$ where Q_{ON} and Q_{OFF} are the total charge in the ON and OFF states of the transistor, respectively, thereby taking into account the nonlinear charge–voltage relationship in TFETs. It has been shown in [8] that the intrinsic speed of TFETs can be higher than MOSFETs over a certain range of $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratios because of the smaller charge involved in the entire switching process. However, the intrinsic speed of the transistor could be deceptive in predicting the large-signal switching performance of a digital circuit. To the best of our knowledge, no work has been done before to investigate the circuit-level switching behavior of TFETs and extract the effective output capacitance and drive current in order to correlate the delay of the inverter (CV/I) device metric to the large-signal switching delay ($\tau_f = 0.69 R_{\mathrm{sw}}(C_{\mathrm{EFF}} + C_L)$, where $R_{\mathrm{sw}} = V_{\mathrm{DD}}/2\ I_{\mathrm{EFF}}$) at the circuit level. In this paper, we show that the effective load capacitance for TFET-based unloaded inverters can be more than twice the gate capacitance as a direct manifestation of the enhanced Miller effect and that the effective drive current can be extracted from a simple three-point model tracking the actual switching current trajectory in inverters.

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II. Miller Effects in TFETs

Both MOSFET and TFET device structures used in this simulation study have a double-gate configuration with a body thickness of 7 nm, a physical gate length of 30 nm, and a high-$\kappa(\mathrm{HfO_2})$ gate dielectric thickness of 2.5 nm. A TFET consists of a p^+ source, an intrinsic (i) channel, and n^+ drain, while for the MOSFET, the p^+ source is replaced with n^+, and the channel is p doped to minimize short-channel effects. A nonlocal tunneling model [9] is used for the simulation of tunnel current that accounts for the actual spatial charge transfer across the tunnel barrier by considering the actual potential profile along the entire path connected by tunneling. Fig. 1(a) and (b) shows the Si TFET and MOSFET capacitance versus voltage characteristics at $V_{\mathrm{DS}} = 0$ and 1.0 V, normalized to the gate oxide capacitance, $C_{\mathrm{ox}} (= \varepsilon_{\mathrm{ox}}/t_{\mathrm{ox}})$. It is clearly seen that for TFETs, the gate-to-drain capacitance (C_{gd} – Miller capacitance) reflects the entire gate capacitance (C_{gg}) and the gate-to-source capacitance (C_{gs}) remains very small due to the presence of source-side tunnel barrier. C_{gd} increases at positive gate voltages due to the reduction in channel-to-drain side potential barrier, as depicted in the inset of Fig. 1(a). It is worth noting that even at $V_{\mathrm{GS}} = V_{\mathrm{DS}} = 1$ V, the gate capacitance C_{gg} in Si TFET is dominated by C_{gd}. In TFETs, the pinchoff point is pushed to higher values of V_{DS} for higher V_{GS}'s, as observed in the output characteristics later in Fig. 8. The fundamental reason for this is that at higher V_{GS}, there is higher band bending at the source-channel end in TFETs, which implies a larger percentage of the drain-to-source bias appears on the source side. Thus, for a given gate voltage (e.g., $V_{\mathrm{GS}} = 1$ V), the drain voltage continues to impact the source-side tunnel barrier until $V_{\mathrm{DS}} = 1$ V, beyond which the pinchoff finally starts to set in and C_{gd} starts decreasing. This is clearly seen in Fig. 2(a), which plots the normalized C_{gd} as a function of the drain voltage V_{DS} for different gate voltages V_{gs}. For $V_{\mathrm{GS}} = 1$ V, C_{gd} starts decreasing only at drain voltages (V_{DS}) exceeding 1 V due to delayed pinchoff. In MOSFETs, both C_{gs} and C_{gd} contribute half of the total gate charge in the linear region and C_{gd} becomes negligible in saturation region due to higher potential barrier between the channel and the drain, thus

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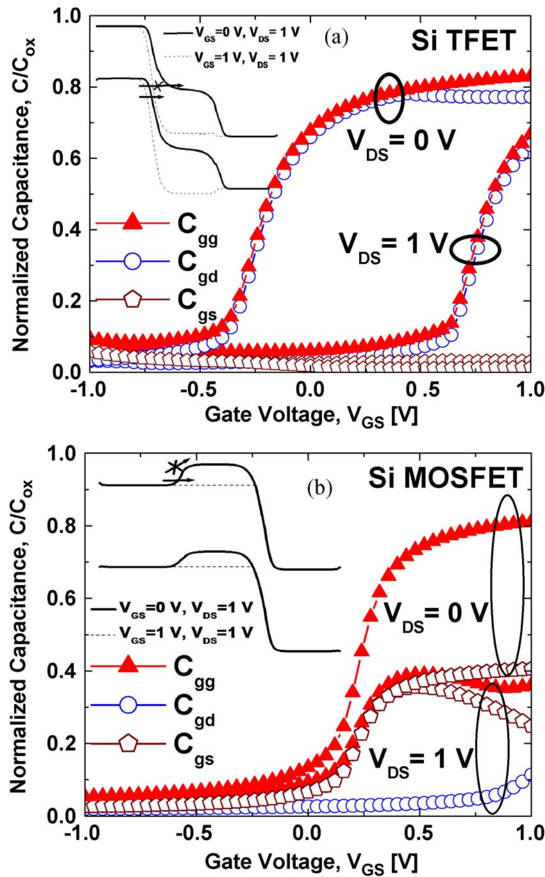

Fig. 1. Capacitance–voltage characteristics showing the gate ($C_{\rm gg}$), gate-to-source ($C_{\rm GS}$), and gate-to-drain ($C_{\rm gd}$) capacitances as a function of gate-to-source voltage $V_{\rm GS}$ for (a) Si TFET and (b) Si MOSFET.

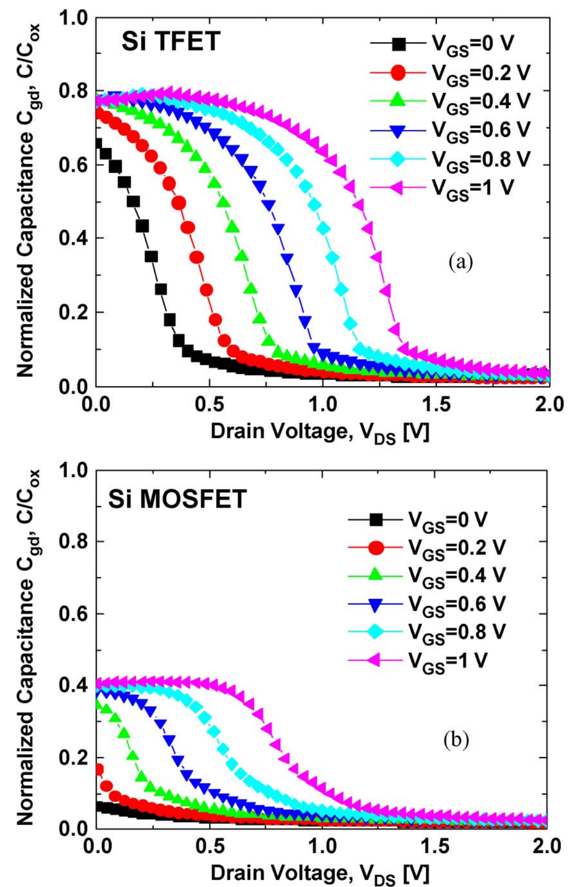

Fig. 2. Normalized gate-to-drain capacitance $C_{\rm gd}$ as a function of drain-to-source voltage $V_{\rm DS}$ for different gate-to-source voltages $V_{\rm GS}$ for (a) Si TFET and (b) Si MOSFET.

causing the majority of the contribution to the gate capacitance to originate from the source ($C_{\rm gs}$). In contrast to TFETs, the pinchoff in MOSFETs takes place at $V_{\rm DS\,SAT}$ given by $V_{\rm GS} - V_T$, and hence, at $V_{\rm GS} = V_{\rm DS} = 1$ V, the channel is well pinched off, and the gate capacitance $C_{\rm gg}$ is mainly dominated by $C_{\rm gs}$. This is, again, more clearly visualized in Fig. 2(b), where $C_{\rm gd}$ in Si MOSFETs for $V_{\rm gs} = 1$ V starts decreasing at a drain voltage $V_{\rm DS}$ of 0.6 V, which is an indication of early saturation.

This high gate-to-drain capacitance ($C_{\rm gd}$) inherent to the TFET device operation has strong implications for its transient response [11]. Fig. 3(a) shows the transient response for Si TFET and MOSFET inverters for an input step voltage with a peak-to-peak voltage of 1 V and a rise time of 5 ps. Si TFETs can be seen to suffer from an output voltage overshoot of 0.9 V (90% of peak input voltage) due to the large Miller feedthrough capacitance originating from its fundamental device operation coupled with its low drive current compared to the MOSFETs. Fig. 3(b) compares the normalized values of the input-to-output capacitance or the Miller capacitance (C_M) for MOSFET and TFET inverters as a function of its input voltage. The contribution to the total Miller capacitance comes from the gate-to-drain capacitance ($C_{\rm gd}$) of both the n- and p-type transistors and is tabulated in Table I. For MOSFET inverters in regions A, B, D, and E, one of the transistors remains in the linear region, resulting in $C_M = C_{\rm gd} = 0.5\, C_{\rm gg}$. The dip seen in the Miller capacitance (region C) is due to both the transistors entering the saturation region during the input ramp from 0 to 1 V. In contrast, in the TFET inverter, both the pull-up and pull-down transistors barely enter saturation (due to delayed pinchoff behavior), and thus, the overall Miller capacitance between the input and output nodes maintains a value of $C_M = C_{\rm gd} = 1.1 C_{\rm gg}$ throughout the entire transition of the input ramp signal. In the Si TFET inverter, where the pull-down device has a very large on-resistance due to poor transmission through the source-to-channel tunnel barrier, the extent of this overshoot can be calculated from the following charge conservation equation [12]:

$$\begin{aligned} C_L V_{\rm MAX} + C_M(V_{\rm MAX} - V_{\rm DD}) &= (C_M + C_L)V_{\rm DD} \\ V_P &= V_{\rm MAX} - V_{\rm DD} \\ &= \frac{C_M}{C_M + C_L} V_{\rm DD} \end{aligned} \tag{1}$$

where C_M is the Miller capacitance connecting the input and output of the inverter comprising the gate-to-drain capacitance of both p-TFET and n-TFET, C_L is the load capacitance external to the device, $V_{\rm MAX}$ is the maximum voltage to which the output voltage rises, V_P is the peak value of the overshoot, and $V_{\rm DD}$ is the supply voltage. This equation clearly shows the impact of higher Miller capacitance on the peak overshoot voltage in silicon-based TFETs.

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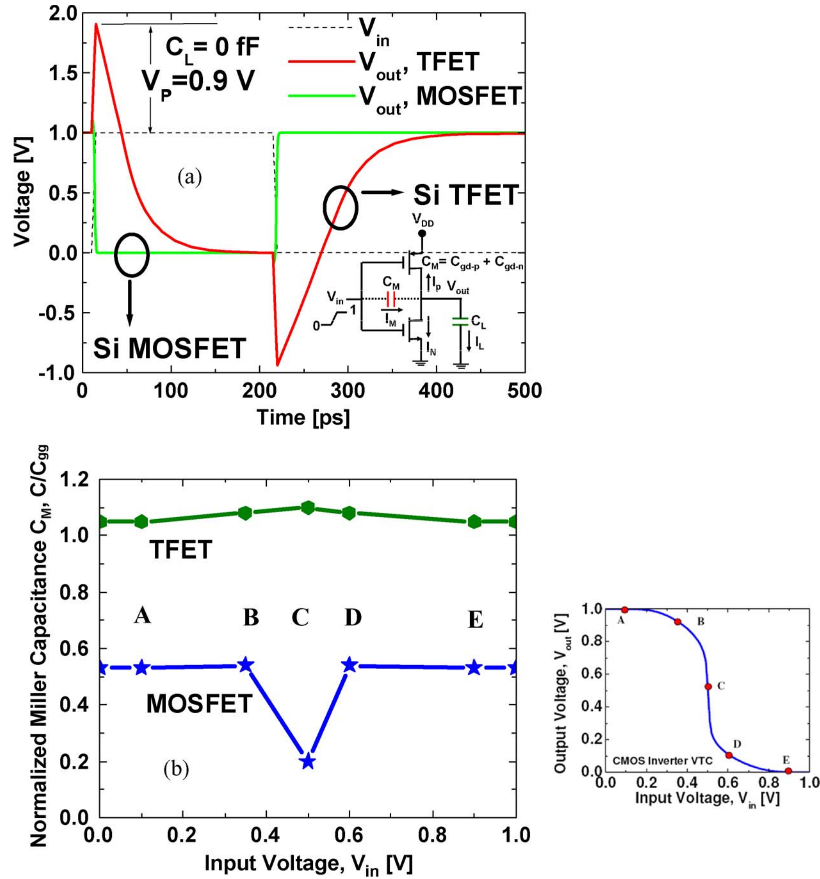

Fig. 3. (a) Transient response of silicon TFET and MOSFET inverters for an input ramp of 0–1 V in 5 ps. The load capacitance C_L is set to zero in this simulation. TFETs exhibit a significantly higher voltage overshoot as well as undershoot due to higher Miller capacitance C_{gd} and lower on-current. (b) Normalized Miller capacitance for TFET/MOSFET inverter as a function of input voltage of the inverter. The demarcated regions A–E are based on the transitions in the device operating point on the MOSFET/TFET inverter dc transfer characteristics.

TABLE I
MILLER CAPACITANCE $C_M = C_{\mathrm{gd},n} + C_{\mathrm{gd},p}$ FOR Si TFET/MOSFET INVERTER FOR VARIOUS POINTS ALONG THE DC TRANSFER CHARACTERISTICS, AS SHOWN IN FIG. 3(b). HERE, $C_{\mathrm{gg}} = 0.8\ C_{\mathrm{ox}}$

	A	B	C	D	E
MOSFET	$0.5C_{gg} + 0.03C_{gg}$ (p-lin, n-cutoff)	$0.5C_{gg} + 0.04C_{gg}$ (p-lin, n-sat)	$0.2C_{gg}$ (p-sat, n-sat)	$0.5C_{gg} + 0.04C_{gg}$ (p-sat, n-lin)	$0.5C_{gg} + 0.03C_{gg}$ (p-cutoff, n-lin)
TFET	$C_{gg} + 0.05C_{gg}$ (p-lin, n-cutoff)	$C_{gg} + 0.08C_{gg}$ (p-lin, n-sat)	$1.1C_{gg}$ (p-sat, n-sat)	$C_{gg} + 0.08C_{gg}$ (p-sat, n-lin)	$C_{gg} + 0.05C_{gg}$ (p-cutoff, n-lin)

Lower bandgap indium arsenide (InAs)-based TFETs have been recently proposed [13] as a promising candidate material for implementing TFET architecture at supply voltages of $V_{\mathrm{DD}} = 0.25$ V. InAs TFETs have high drive current (I_{ON}) at lower supply voltages due to its lower tunnel barrier height and width as well as a lower tunneling mass, and its gate capacitance C_{gg} is limited by the quantum capacitance originating from its reduced density of states (DOS). Fig. 4(a) illustrates the capacitance–voltage characteristics of InAs TFETs showing that the total gate capacitance (C_{gg}) is only 10% of the gate oxide capacitance (C_{ox}). Again, C_{gd} is the dominant contributor to C_{gg} due to the inherent tunnel transistor architecture, but the capacitance value is significantly lower than that of Si TFETs at $V_{\mathrm{DD}} = 1$ V. Further, the on-resistance of the InAs TFETs is considerably lower than that in Si TFETs. This lower feedforward Miller capacitance along with higher drive current provided by the pull-down device at lower input voltages reduces the peak overshoot voltages in InAs TFET inverters to less than 20% of input peak voltage, as shown in Fig. 4(b). Fig. 5 compares the effect of external capacitance loading (i.e., electrical effort) in Si- and InAs-based TFET inverters on the percentage voltage overshoot. Both TFET inverters show a reduction in peak overshoot with increased capacitive loading as expected from (1), but the overshoot is significantly smaller for the InAs-based TFET inverter due to its smaller switching resistance (higher drive current at lower supply voltages) and reduced Miller capacitance C_{gd}.

III. EFFECTIVE OUTPUT CAPACITANCE AND DRIVE CURRENT

Table II compares the actual inverter fall delay obtained from the inverter transient response (Figs. 3 and 4), with some common metrics used to benchmark the MOSFET inverter

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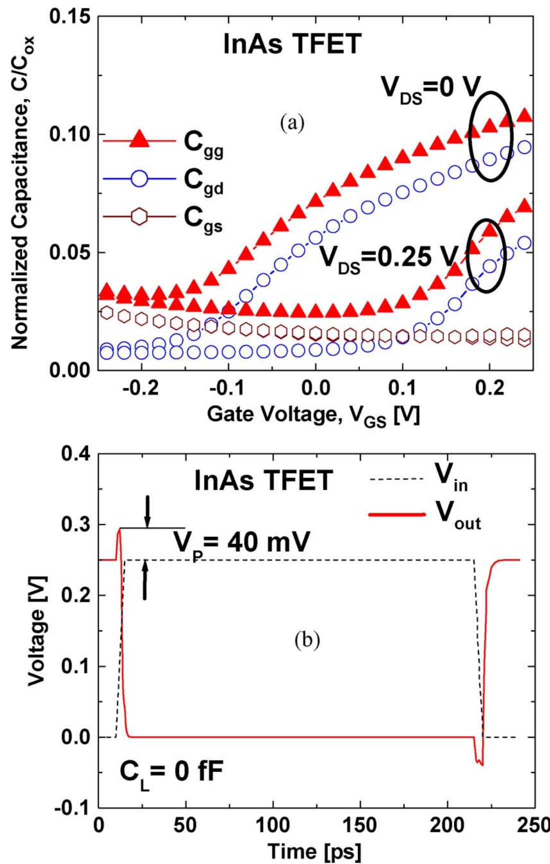

Fig. 4. (a) Capacitance–voltage characteristics of an InAs TFET showing the gate ($C_{\rm gg}$), gate-to-source ($C_{\rm gs}$), and gate-to-drain ($C_{\rm gd}$) capacitances as a function of gate-to-source voltage $V_{\rm GS}$. Note that the supply voltage is $V_{DD} = 0.25$ V. (b) Transient response of an InAs TFET inverter for an input ramp of 0–0.25 V in 5 ps. InAs TFET exhibits a significantly smaller voltage overshoot/undershoot due to smaller Miller capacitance and higher $I_{\rm ON}$ compared to Si TFETs.

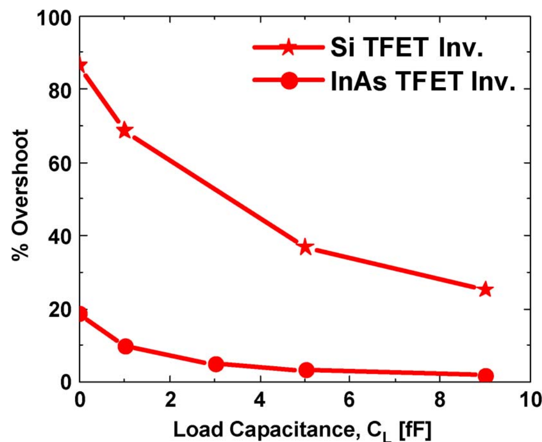

Fig. 5. Percentage overshoot as a function of load capacitance (C_L) for Si and InAs TFET inverters.

delay. For comparison, the same metrics have also been applied to TFET inverters to understand its effectiveness in predicting TFET inverter performance. Here, $C_{\rm gg}$ refers to the gate capacitance in the linear operation region ($V_{\rm GS} = V_{\rm DD}$ and $V_{\rm DS} = 0$ V), including the channel capacitance arising from the DOS limitation and is equal to $0.8C_{\rm ox}$ for the Si TFET/MOSFET and $0.1C_{\rm ox}$ for the InAs TFET, while $I_{\rm ON}$ refers to the saturation drive current, $I_{\rm DSAT}$, at $V_{\rm GS} = V_{\rm DS} = V_{\rm DD}$. The commonly used metrics differ from the actual MOSFET inverter fall delay with an error that is unacceptable for today's scaled CMOS technologies with scaled threshold voltages. It was shown in [14] and [15] that an effective drive current ($I_{\rm EFF}$) needs to be used to predict the actual delay of a MOSFET inverter instead of $I_{\rm ON}$ since the actual switching current could be significantly lower than the saturation current of an individual transistor. Analytical models were also suggested to calculate the average or effective drive current ($I_{\rm EFF}$) by taking into account the actual inverter switching current trajectory. Table II clearly highlights the fact that the commonly used benchmarking metrics applied so far also significantly differ from the TFET inverter performance, and therefore, a need arises to accurately quantify the effective output capacitance and the effective switching current to predict the TFET performance. In this paper, we focus on accurately estimating the CV/I metrics in TFETs in two materials systems, namely, Si and InAs, and present the Si MOSFET results only for comparison. Silicon and InAs are chosen since they represent the high- and low-DOS materials categories, respectively.

We analyze the fall delay (high-to-low transition of the output voltage) to extract the effective load capacitance and the effective switching current. The fall delay is defined as the time interval between 50% of the input voltage ($V_{\rm in}$) and 50% of the output voltage ($V_{\rm out}$) in the transient response. Fig. 6 shows the fall delay for Si TFET, Si MOSFET, and InAs TFET inverters for different values of load capacitance (C_L) obtained through detailed device-level mixed-mode simulations. It is clearly seen that the Si TFET exhibits an order of magnitude higher fall delay compared to the Si MOSFET and InAs TFET due to its low $I_{\rm ON}$ and the additional voltage overshoot due to the Miller feedthrough effect. A simple RC model is often used to calculate the fall delay (τ_f) in CMOS inverters, assuming a total load capacitance ($C_L + C_{\rm EFF}$) discharging through a constant resistor ($R_{\rm sw}$). The fall delay is expressed as

$$\tau_f = 0.69\, R_{\rm sw}(C_{\rm EFF} + C_L) \quad (2)$$

$$R_{\rm sw} = \frac{V_{\rm DD}}{2\, I_{\rm EFF}} \quad (3)$$

where $C_{\rm EFF}$ is the effective output capacitance of the unloaded inverter comprising contributions from the intrinsic gate-to-drain capacitances ($C_{\rm gd}$) of both the n- and p-type transistors, and C_L is the additional load capacitance external to the device. $R_{\rm sw}$ is the effective switching resistance of the n-type TFET/MOSFET through which the total output capacitance ($C_{\rm EFF} + C_L$) discharges, $V_{\rm DD}$ is the supply voltage, and $I_{\rm EFF}$ is the effective switching current through $R_{\rm sw}$, pulling the output node of the inverter to ground. Equation (2) shows that the effective switching resistance ($R_{\rm sw}$) can be extracted from the slope of the fall delay (τ_f) versus load capacitance (C_L), and the y-intercept will be the total capacitance between the output node of the inverter and ground, which is intrinsic to the device ($C_{\rm EFF}$). Once $R_{\rm sw}$ is obtained, the effective drive current $I_{\rm EFF}$ can easily be extracted from (3). These extracted values are tabulated in Table III. It is important to note at this point that the large delay benefit (~45× at $C_L = 0$ fF) obtained

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TABLE II
COMPARISON OF ACTUAL INVERTER DELAY WITH COMMONLY USED BENCHMARKING TECHNIQUES

Delay [ps]	$\frac{C_{ox}V_{DD}}{2I_{ON}}$	$\frac{C_{gg}V_{DD}}{2I_{ON}}$	$\frac{Q_{ON}-Q_{OFF}}{I_{ON}}$	Inverter Fall Delay, τ_f
Si MOSFET	1	0.8	0.63	1.15
Si TFET	18.5	15	8	48
InAs TFET	3.5	0.38	0.3	1.1

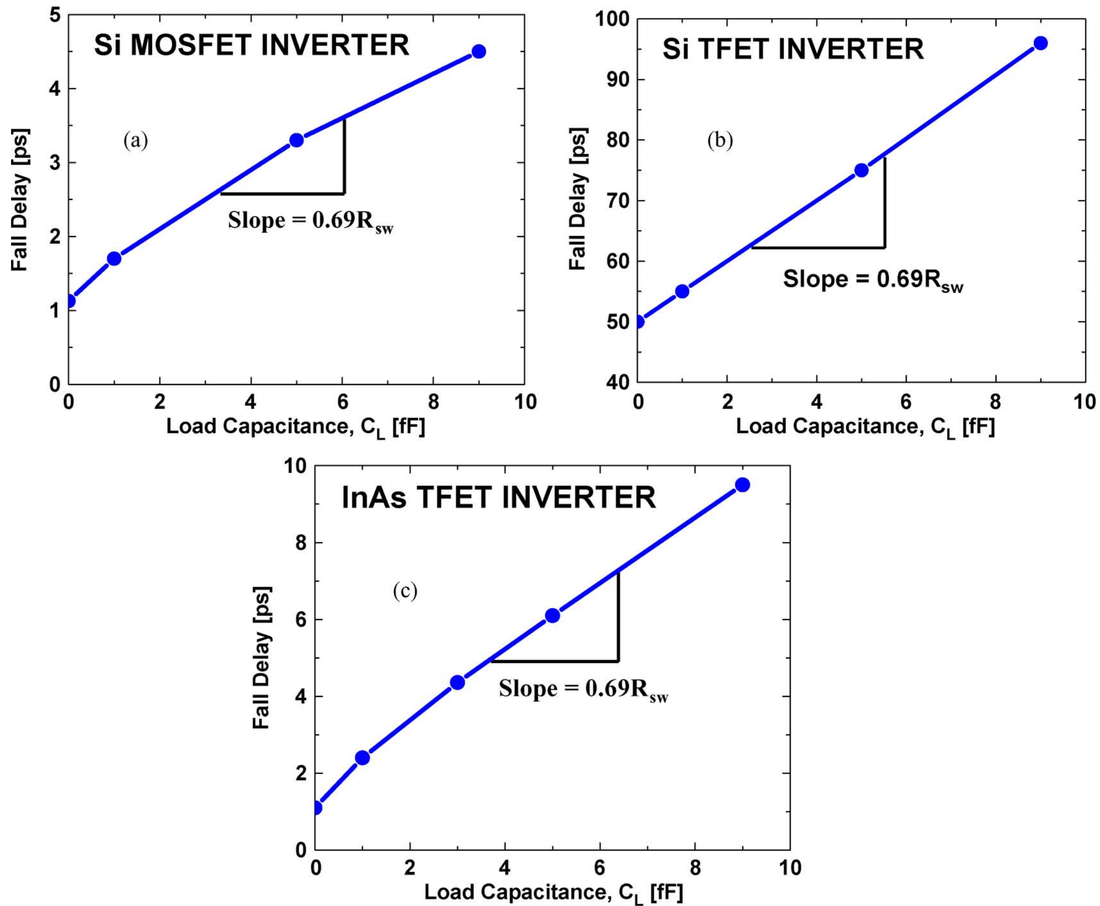

Fig. 6. Fall time delay (τ_f) as a function of load capacitance C_L for (a) Si MOSFET, (b) Si TFET, and (c) InAs TFET inverters. Fall time delay is measured as the time interval between 50% of the input voltage (V_{in}) and 50% of the output voltage (V_{out}) of the inverter in Fig. 2.

TABLE III
SWITCHING RESISTANCE (R_{sw}), EFFECTIVE SWITCHING CURRENT (I_{EFF}), AND OUTPUT CAPACITANCE (C_{EFF}) EXTRACTED FROM FIG. 4 USING THE SIMPLE RC MODEL DEFINED IN (1) AND (2)

Inverter	Switching Resistance, R_{sw}	Effective switching current, I_{EFF}	Effective output capacitance, C_{EFF}
Si MOSFET	0.5 KΩ	0.93 mA	0.9 C_{gg}
Si TFET	7.4 KΩ	68 μA	2.6 C_{gg}
InAs TFET	1.3 KΩ	97 μA	2.6 C_{gg}

in going from Si to InAs TFET inverters (Table II) comes from both the eight times reduced effective output capacitance as well as the 5.7 times smaller switching resistance. The most notable difference between MOSFETs and TFETs shows up in the rightmost column of the effective output capacitance (C_{EFF}) in Table III. The effective output capacitance for Si and InAs TFET inverters shows up as 2.6 times the gate capacitance C_{gg} as opposed to 0.9 times the gate capacitance C_{gg} for Si MOSFETs. The fundamental cause of increased effective capacitance in TFETs is due to the high gate-to-drain capacitance in TFETs, which is enhanced by the Miller effect. A similar Miller effect has also been observed in Si MOSFETs, but the absolute values of gate-to-drain capacitance C_{gd} are much smaller in MOSFETs compared to that in TFETs [16].

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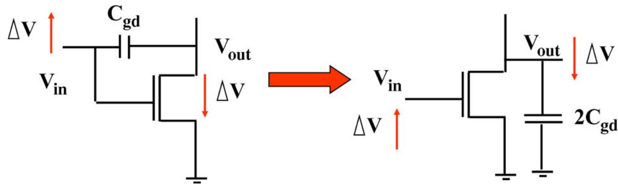

Fig. 7. Capacitor experiencing identical but opposite voltage swings at both its terminal can be replaced by a capacitance to ground whose value is two times the original value. This is called the Miller effect. Due to this Miller effect, the gate-to-drain capacitance contribution toward the effective output capacitance calculation in Section III is doubled.

The concept of this Miller effect is schematically illustrated in Fig. 7. The Miller effect in digital switching arises when time-varying voltages are moving in opposite directions on both sides of a capacitor. This is the case for the gate-to-drain capacitance C_{gd} connected between the input terminal (gate) and the output terminal (drain) of an inverter for both MOSFETs and TFETs. The effective capacitance at the output node is double this input-to-output capacitance C_{gd} due to the Miller effect. It is worth pointing out that $C_{\mathrm{EFF}} \sim 2.6\ C_{\mathrm{gg}}$, as extracted from Fig. 6, is slightly higher than $\sim$2.2 C_{gg} expected from Table I since the capacitances listed in Table I have been extracted at fixed dc bias points under quasi-static assumption along the inverter voltage transfer characteristic [Fig. 3(b)] as opposed to the actual capacitances that change in a non-quasi-static manner during the transient switching of the inverter. Ignoring the impact of this enhanced output capacitance due to the Miller effect would lead to severe underestimation of the TFET effective switching capacitance. Similarly, the correct switching current also needs to be extracted from the output I–V characteristics of the TFET to estimate the fall delay. This current needs to be consistent with the effective current extracted from the simple RC model and enumerated in Table III.

In order to ensure that the I_{EFF} extracted from the simple RC method resembles the actual current flowing through the pull-down transistor, the real-time drive current trajectory of the TFET is analyzed in greater detail. Fig. 8(a) and (b) shows the real-time drive current trajectory for Si and InAs TFET inverters superimposed on its dc I_{DS}–V_{DS} characteristics. Critical differences are seen in the switching current trajectories for the Si and InAs TFETs originating from the marked differences in the amount of the output voltage overshoot due to the capacitive feedforward effect. For the Si TFET inverter, as the input voltage ramps to V_{DD}, the drain voltage of the n-TFET swings to V_{MAX} due the capacitive feedforward Miller effect, forcing it into deep saturation. It is noted that the saturation current I_{ON} at $V_{\mathrm{GS}} = 1$ V and $V_{\mathrm{DS}} = 1$ V discharges the entire drain overshoot voltage in Si TFETs. In contrast, for the InAs TFET inverter, due to the lower overshoot voltage and high on-current, the output drain voltage starts transitioning from V_{DD} before the input gate voltage reaches V_{DD}. Thus, the peak current never reaches the saturation current I_{ON} during switching. In MOSFETs, often, a two-point average [14] is used to approximate the effective drive current trajectory as $(I_H + I_L)/2$, where I_H (high current) is the drain current at $V_{\mathrm{GS}} = V_{\mathrm{DD}} = 1$ V and $V_{\mathrm{DS}} = V_{\mathrm{DD}}/2 = 0.5$ V and I_L (low current) is the drain current at $V_{\mathrm{GS}} = V_{\mathrm{DD}}/2 = 0.5$ V and $V_{\mathrm{DS}} = V_{\mathrm{DD}} = 1$ V. It has been further shown that this two-point average is no longer adequate in predicting the effective drive current for nontraditionally scaled Si MOSFETs (with a low threshold voltage V_T) and novel devices like carbon nanotube FETs [15]. Likewise, due to the large overshoot in the transient response of Si TFETs, a simple two-point model is inadequate, and a three-point model is required to closely predict average current flowing through the switching transistor. We propose the following general three-point model for Si and InAs TFETs, taking into consideration the overshoot effects in the actual current trajectory:

$$I_{\mathrm{EFF}} = \frac{I_L + I_P + I_H}{3} \tag{4}$$

where I_H and I_L have the same definitions as above, while I_P is the peak current in the real-time switching current trajectory. For Si TFETs, I_P occurs at $V_{\mathrm{GS}} = V_{\mathrm{DS}} = 1$, i.e., at $V_{\mathrm{GS}} = V_{\mathrm{DS}} = V_{\mathrm{DD}}$, which is the saturation current (I_{ON}), while for InAs TFETs, I_P is at $V_{\mathrm{GS}} = V_{\mathrm{DS}} = 0.17$ V, i.e., at $V_{\mathrm{GS}} = V_{\mathrm{DS}} = 0.7V_{\mathrm{DD}}$ and is significantly lower than its I_{ON} at $V_{\mathrm{GS}} = V_{\mathrm{DS}} = V_{\mathrm{DD}} = 0.25$ V. As can be seen in Fig. 8, this three-point average along the drive current trajectory approximates the effective current calculated using the simple RC model in (2) and (3) to within 8% for Si TFETs and to within 1% for

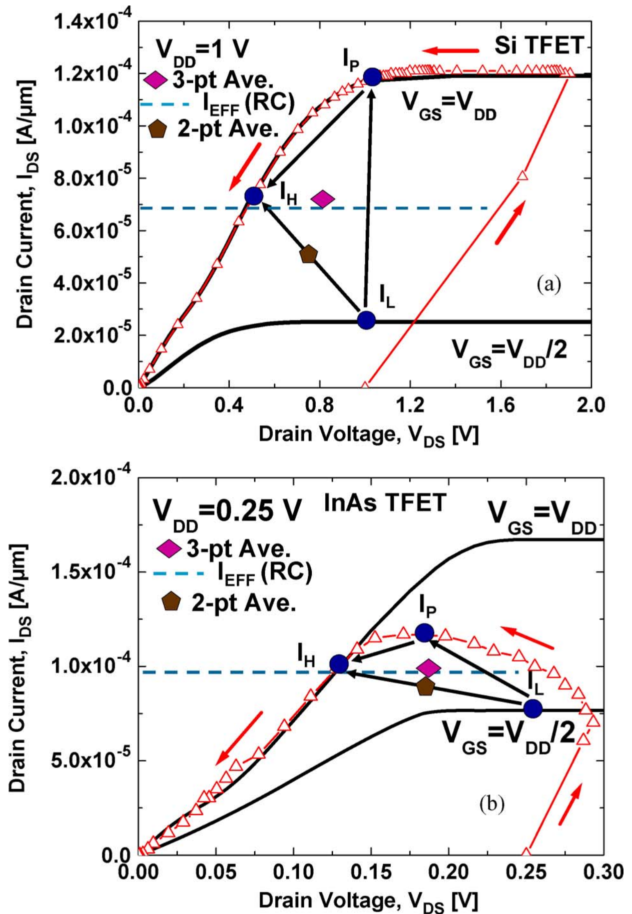

Fig. 8. Real-time drive current trajectory in the n-type TFET during inverter switching (triangles) superimposed on its dc I_{DS}–V_{DS} (black line) characteristics at $V_{\mathrm{GS}} = V_{DD}$ and $V_{\mathrm{DD}}/2$ for (a) Si TFET inverter and (b) InAs TFET inverter. I_L, I_P, and I_H are three points along the current trajectory used to calculate the average switching current as defined in the text.

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InAs TFETs. A two-point model leads to errors greater than 10% for both InAs and Si TFET inverters. It is worth noting in Fig. 8 that the three-point average computed from (4) brings the I_{EFF} close to I_H, but it is more physical to use a three-point average than a single point since it more closely tracks the actual switching current trajectory in the inverter.

IV. Conclusion

In summary, we have shown a simple way to extract the effective output capacitance and effective switching current for an unloaded inverter from the y-intercept and the slope of the fall delay versus load capacitance plot. It is shown that the effective output capacitance (C_{EFF}) of the unloaded TFET inverter is 2.6 times the gate capacitance C_{gg} due to the Miller effect, unlike MOSFETs, where it is approximately equal to the gate capacitance (C_{gg}). The I_{EFF} extracted from the switching resistance R_{sw} reflected by the slope of the delay versus load capacitance plot can be approximated by a three-point average of the actual switching current trajectory for Si and InAs TFET inverters to within 8% and 1% accuracies. The $C_{\mathrm{EFF}} = 2.6 \times C_{\mathrm{gg}}$ and $I_{\mathrm{EFF}} = 0.33 \times (I_L + I_H + I_P)$ thus extracted from the capacitance–voltage and the output I–V characteristics of TFET at the device level can provide a more accurate prediction of its circuit level performance.

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