Experimental Demonstration of 100nm Channel Length $In_{0.53}Ga_{0.47}As$-based Vertical Inter-band Tunnel Field Effect Transistors (TFETs) for Ultra Low-Power Logic and SRAM Applications

S. Mookerjea, D. Mohata, R. Krishnan, J. Singh, A. Vallett, A. Ali, T. Mayer, V. Narayanan, D. Schlom[1], A. Liu[2] and S. Datta
Electrical Engineering, The Pennsylvania State University, University Park, PA 16802, USA;
[1] Materials Science and Engineering, Cornell University, Ithaca, NY 14853, USA; [2] IQE Inc., Bethlehem, PA 18015, USA;
Tel: (814) 865-0519, Fax: (814) 865-7065, Email: sam567@psu.edu

Abstract: Vertical $In_{0.53}Ga_{0.47}As$ tunnel field effect transistors (TFETs) with 100nm channel length and high-k/metal gate stack are demonstrated with high I_{on}/I_{off} ratio (>10^4). At V_{DS} = 0.75V, a record on-current of 20μA/μm is achieved due to higher tunneling rate in narrow tunnel gap $In_{0.53}Ga_{0.47}As$. The TFETs exhibit gate bias dependent NDR characteristics at room temperature under forward bias confirming band to band tunneling. The measured data are in excellent agreement with two-dimensional numerical simulation at all drain biases. A novel 6T TFET SRAM cell using virtual ground assist is demonstrated despite the asymmetric source/drain configuration of TFETs.

Introduction: Inter-band tunnel FETs (TFETs) with a gate-modulated Zener tunnel junction at the source are of interest for MOSFET replacement since the reverse biased tunnel junction in the former eliminates the high-energy tail of the Fermi distribution of valence band electrons in the source region thereby allowing for abrupt turn-on near the OFF state[1]. However, till date, almost all Si and Si_xGe_{1-x} based TFETs exhibit low I_{on} due to high tunnel barrier. We present here improved I_{on} and I_{on}-I_{off} ratios utilizing a vertical $In_{0.53}Ga_{0.47}As$ TFET. A fundamental advantage of the vertical transistor design is that high quality, *in-situ* doped junctions are realized enabling not only observation of room temperature NDR effects but also reduction of off-state reverse biased p+/i/n+ leakage.

Device Fabrication: N-channel $In_{0.53}Ga_{0.47}As$ TFETs were fabricated using MBE grown epitaxial structure on semi-insulating InP substrate. The epitaxial layers comprise of 300nm thick n+ drain region (Si doping of $5x10^{19}$ cm^{-3}), 100nm intrinsic channel region and 60nm thick p+ source region (C doping of $1x10^{20}$ cm^{-3}) (**Fig. 1a**). After source metal (Ti/Pt/Au) evaporation and lift-off, a facet dependent mesa sidewall etch is performed using citric acid and peroxide chemistry exposing the n+ region (**Fig. 1b**). A highly conformal 10nm thick Al_2O_3 is deposited on the mesa sidewall using atomic layer deposition (ALD) followed by gate metallization (Pt/Au) and liftoff (**Figs. 1c-d**). A subsequent lithography step defines source/drain contact openings and the Al_2O_3 film is removed thereof to make direct contact to the source/drain regions, followed by a final isolation etch (**Fig. 1e**). **Figs. 1g-h** show the SEM images of fabricated $In_{0.53}Ga_{0.47}As$ vertical TFET featuring gate air-bridge and conformal gate stack on the sidewall.

Device Results and Discussion: **Figs. 2(a)-(b)** show the measured transfer and output characteristics of the 100nm channel length tunnel transistors at room temperature. The minimum current ("leakage floor") at V_{DS} = 50mV is only 40 pA/μm increasing to 6nA/μm at V_{DS} = 0.75V. The corresponding on currents are 0.5μA/μm (linear) and 20μA/μm (saturation). This translates to I_{on}-I_{off} ratio of ~ 10^4 and $3x10^3$, respectively. Two distinct regions of operation are evident from the output characteristics – a reverse biased zener diode and a forward biased Esaki diode as a function of the gate voltage. **Fig. 3** shows the 2 terminal characteristics of non-gated $In_{0.53}Ga_{0.47}As$ p+/i/n+ diodes fabricated at the same time showing excellent agreement with the modeled data at various temperature. At low reverse bias, SRH generation-recombination dominates the J-V while, at high reverse bias, it is direct band-to-band tunneling. We employed a commercial two dimensional numerical simulator solving non local tunneling self-consistently with the device electrostatics to model the measured TFET transfer characteristics at 50mV/0.75V V_{DS} (**Fig. 4**). The leakage floor agrees with the experimental and modeled reverse biased p+/i/n+ diode J-V and the on-current agrees well with the non-local band to band tunneling model. **Fig. 4** shows the impact of Dit (extracted from the C-V and G-V measurements on control $In_{0.53}Ga_{0.47}As$ MOSFETs (**Fig. 5a-d**)) on the $In_{0.53}Ga_{0.47}As$ TFET turn-on characteristics. While Dit effect on steep switching is negligible due to the limited movement of Fermi level near the channel conduction band edge, trap assisted tunneling (TAT) and subsequent thermal emission has strong effect on TFET turn-on (**Fig. 6a,b**). Temperature dependent measurement of $In_{0.53}Ga_{0.47}As$ TFET shows that the leakage floor increases exponentially with temperature (SRH) (**Fig. 7**) whereas I_{on} (a) increases at low V_{GS} due to gap reduction (limited by tunnel barrier resistance) b) decreases with temperature at high V_{GS} due to phonon scattering (limited by channel resistance) (**Fig. 8**). Gated negative differential resistance (NDR) behavior in TFET output characteristics during drain-to-source forward bias operation confirm the inter-band tunneling process (**Fig. 9**).

Logic and SRAM Performance: **Fig. 10** shows 100nm $In_{0.53}Ga_{0.47}As$ TFET (this work) outperforming previously reported Si[2], $Si_{0.3}Ge_{0.7}$[2], unstrained[2] and strained[3] Ge TFETs (of comparable gate length) with the highest on current performance till date and projects its logic performance with EOT scaling and increasing indium content. Due to its inherent asymmetric source and drain design, bidirectional current conduction is not possible in TFETs as shown with $In_{0.53}Ga_{0.47}As$ and Si TFETs (**Fig. 11**). This makes TFET based pass transistor implementation impossible resulting in 6T TFET SRAM with degraded read or write margins (**Fig. 12**).7T and 8T TFET SRAM implementations with separate read and write port have been proposed compromising cell size. We implement a novel 6T TFET SRAM where inward M5 and outward M6 TFETs are used to write "1" and "0", respectively, at the same node Q (**Fig. 13**). During writing, the cell is weakened by disabling the inverter pair cross-coupling via virtual ground. Excellent read and write noise margins are achieved in this 6T TFET SRAM (**Fig.**14).

Conclusion: We have demonstrated 100nm L_G vertical $In_{0.53}Ga_{0.47}As$ TFET with 10^4 I_{on}-I_{off} ratio and 20μA/um on current. The TFET I-V characteristics are explained by nonlocal inter-band tunneling, SRH and TAT. A 6T SRAM cell is shown with excellent noise margin down to 0.3V supply voltage making narrow gap III-V TFET a promising device architecture for ultra low power digital applications.

References: [1]S. Mookerjea *et al*, Elec. Dev. Lett. Oct (2009) [2]F. Mayer et al IEDM Tech. Dig. 163 (2008) [3]T. Krishnomohan *et al*, IEDM Tech. Dig. 163 (2008) [4]D. Kim et al, Proc. ISLPED '09 Aug (2009)

Acknowledgement: We acknowledge financial support from NRI/SRC sponsored MIND center and Intel and helpful discussions with A. Seabaugh (U. Notre Dame), P. Majhi (Sematech) and SEM support from S. Rommell (RIT)

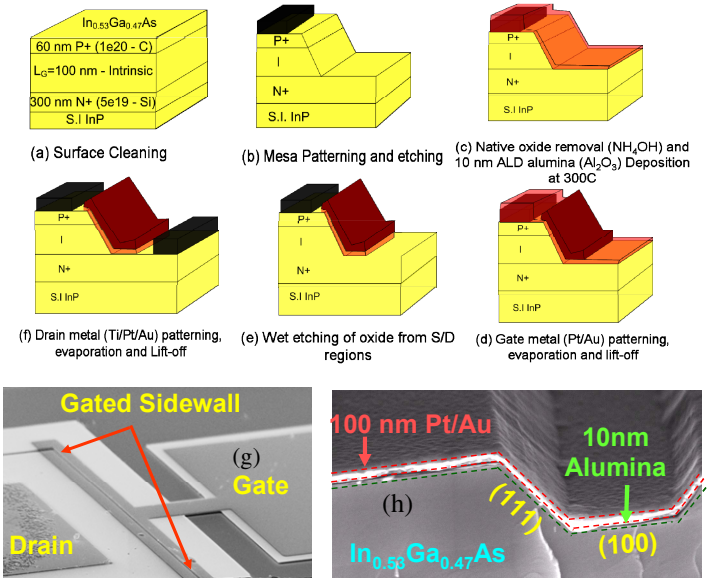


Fig 1. (a) MBE grown $In_{0.53}Ga_{0.47}As$ p+/i/n+ eptitaxial structure; Process Fabrication flow: (b) Source contact lithography, Ti/Pt/Au metallization and liftoff followed by sidewall mesa patterning using citric acid based wet etch chemistry; (c) Native oxide removal on the sidewall followed by ALD deposition of 10nm thick Al_2O_3 dielectric at 300°C (d) Gate patterning, Pt/Au metallization and liftoff; (e) S/D contact patterning, wet etch removal of Al_2O_3 ; (f) Ti/Pt/Au metallization and liftoff and a final mesa isolation etch; (g) Tilted view SEM picture of fabricated vertical TFET featuring a gate air-bridge process (h) Cross-section SEM picture of the etched sidewall with conformal gate stack.

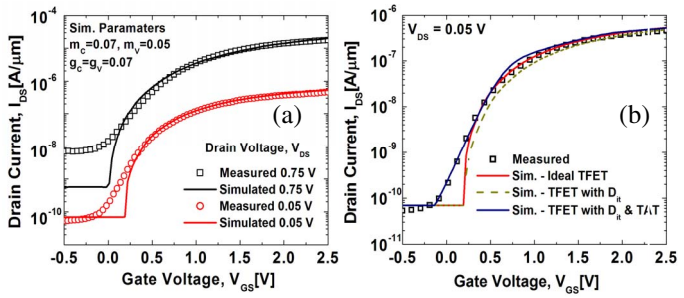


Fig 4. (a) Measured and simulated (ideal) $In_{0.53}Ga_{0.47}As$ TFET transfer characteristics and (b) simulated transfer characteristics using the measured Dit as well as trap assisted tunneling (TAT) + Dit.

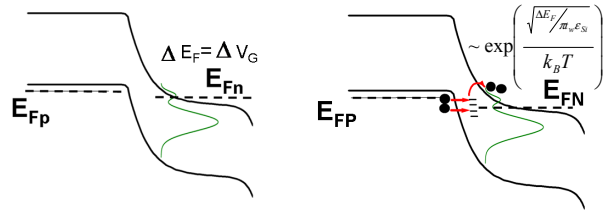


Fig 6. Energy band diagrams illustrating the impact of Dit on TFET sub-threshold slope; (a) Dit only effect is negligible and (b) D_{it} and TAT degrades sub-threshold slope since it involves tunneling into the interface traps and subsequent thermal emission from the traps giving rise to temperature dependence.

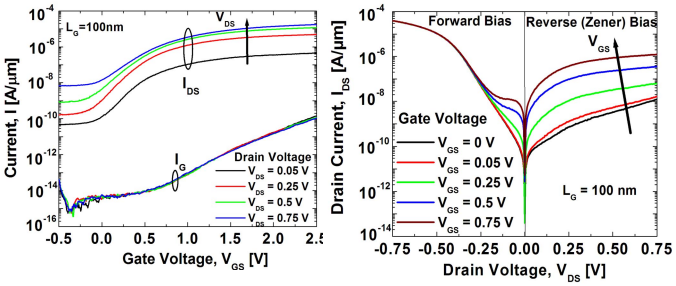
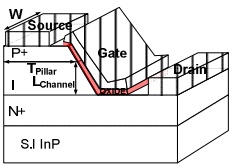


Fig 2. Measured (a) I_D-V_{GS}, I_G-V_{GS} and (b) I_D-V_{DS} characteristics for a 100nm channel length vertical $In_{0.53}Ga_{0.47}As$ TFET.



Parameter	Value
$L_{channel}$	100 nm
W	11 μm
EOT	4.5 nm
T_{pillar}	20 μm

Table I: $In_{0.53}Ga_{0.47}As$ TFET device parameters.

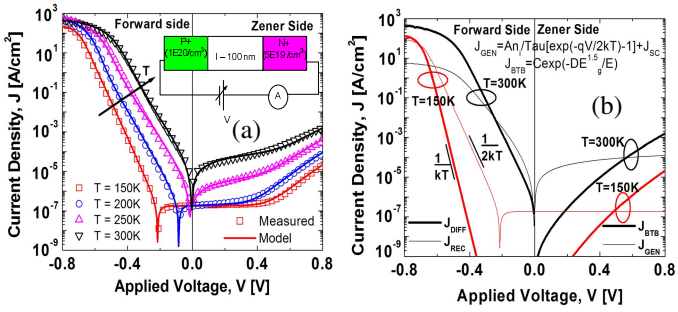


Fig 3. (a) Measured and modeled J-V characteristic and (b) various modeled components for $In_{0.53}Ga_{0.47}As$ p+/i/n+ diode at various temperature.

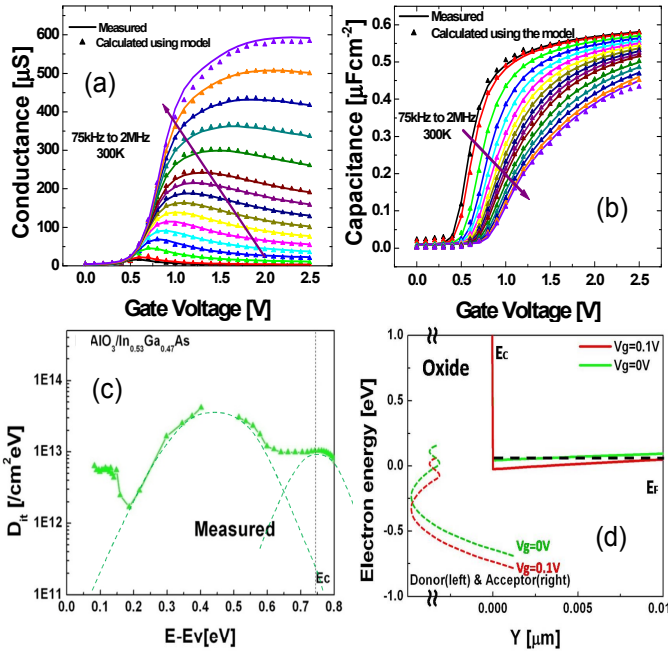


Fig 5. Measured (a) conductance, (b) capacitance, (c) interface state profile (Dit) for $In_{0.53}Ga_{0.47}As$ MOSFET and (d) simulated movement of Fermi level across Dit profile for $In_{0.53}Ga_{0.47}As$ TFET.

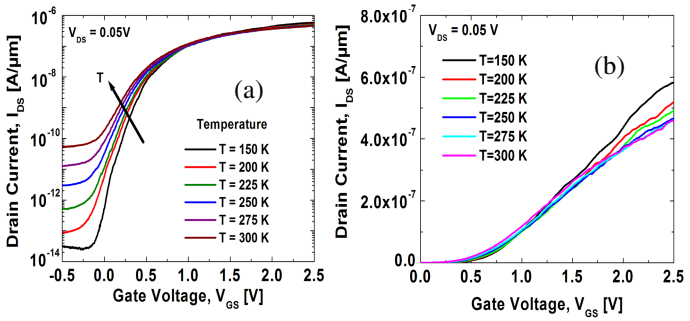


Fig 7. $In_{0.53}Ga_{0.47}As$ TFET transfer characteristics illustrating the temperature dependence of the leakage floor and the on-current. The leakage floor increases exponentially with increasing temperature consistent with SRH generation recombination mechanism.

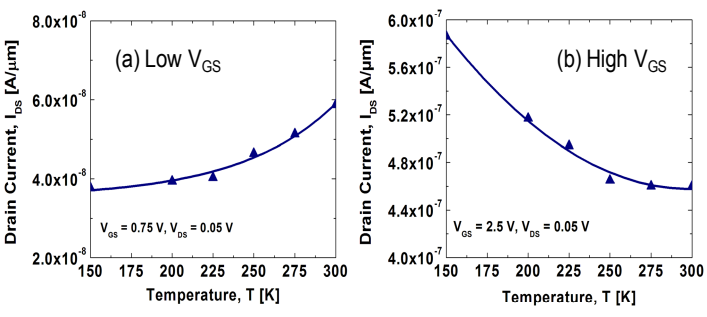


Fig 8. $In_{0.53}Ga_{0.47}As$ TFET on current (a) increases at low V_{GS} due to reducing tunnel gap (limited by tunnel barrier resistance) and (b) decreases with temperature at high V_{GS} (limited by phonon scattering limited channel resistance).

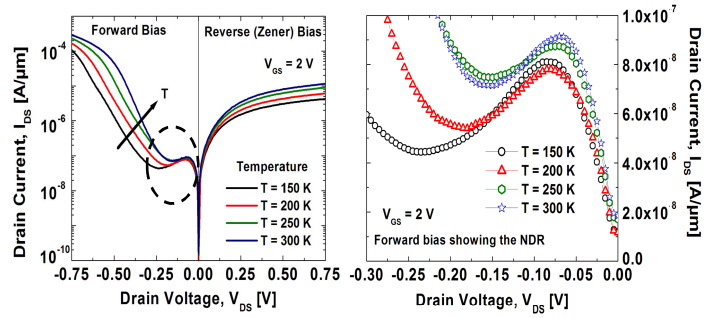


Fig 9. Gated negative differential resistance (NDR) characteristics as a function of temperature during forward bias between drain and source of $In_{0.53}Ga_{0.47}As$ TFET. A PVCR of 2 is observed at 150K.

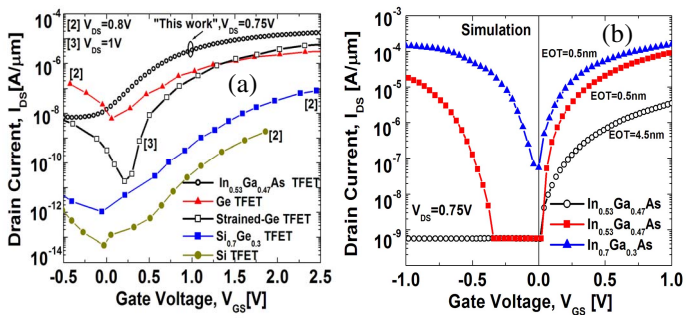


Fig 10. (a) Measured 100nm $In_{0.53}Ga_{0.47}As$ TFET transfer characteristics showing highest I_{on} benchmarked against Si, SiGe, Ge and strained Ge TFETs. (b) Projected performance of $In_{0.53}Ga_{0.47}As$ TFETs with EOT scaling and increasing indium content (70%) using calibrated TCAD model.

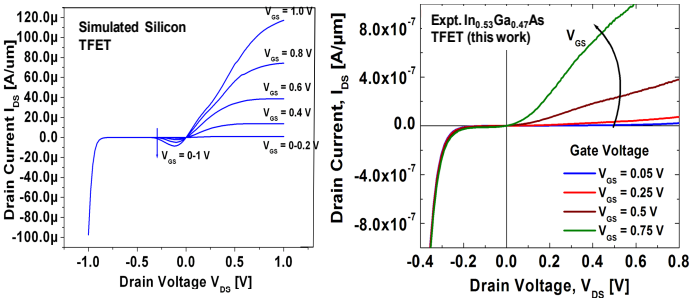


Fig 11. Asymmetric output characteristics in Si TFETs (simulated) and experimentally observed in $In_{0.53}Ga_{0.47}As$ TFETs due to the inherent diode between source and drain, highlighting the difficulty in pass transistor implementation.

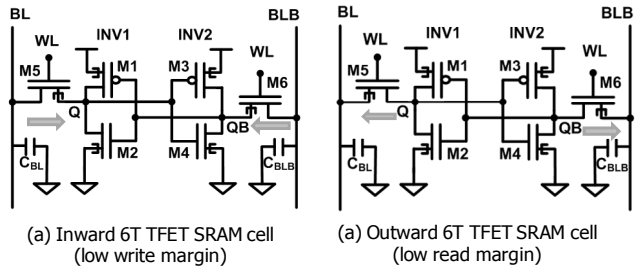


Fig 12. 6T TFET SRAM cell using TFET pass transistors pointing (a) inward and (b) outward. Inward 6T TFET SRAM has good read margin but poor write margin whereas the outward TFET SRAM exhibits excellent write margin but poor read margin.

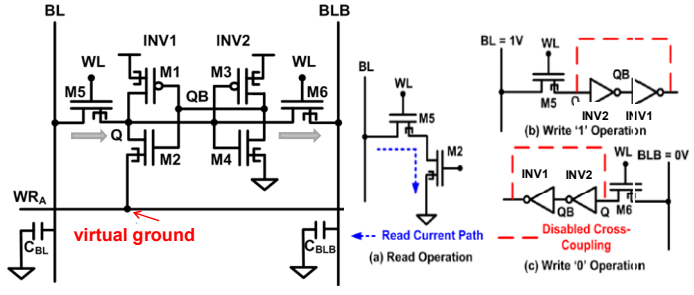


Fig 13. Novel 6T TFET SRAM is designed where M5 and M6 TFETs are used to write "1" and "0", respectively, at node Q. During write, the cell is weakened by disabling the inverter pair cross-coupling via virtual ground. Read operation is similar to inward 6T TFET SRAM.

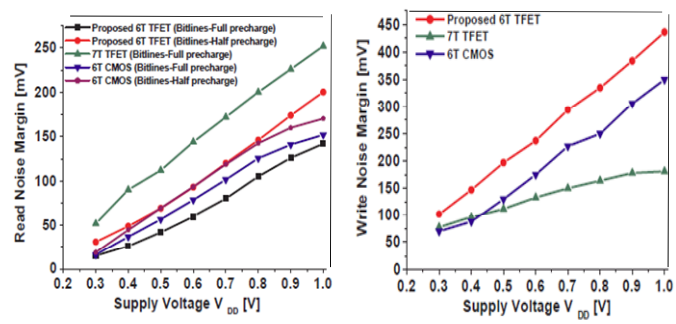


Fig 14. Excellent read and write noise margins achieved with the proposed 6T TFET SRAM cell with the SRAM cell exhibiting cell stability till 0.3V supply voltage.