

Interface State Response in HfO₂ Gated Strained InAs Quantum Well FETs

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Schottky gated high mobility quantum well FETs (QWFETs) such as In_{0.7}Ga_{0.3}As and InSb are potential candidates for high performance logic applications^{1, 2}. However, lack of good quality oxide interface poses challenges towards integrating high-k dielectric with the QWFETs for lower gate leakage. Recently, inversion mode surface channel In_{0.53}Ga_{0.47}As MOSFETs with ALD Al₂O₃, HfO₂ and MBD LaAlO₃ oxides have been demonstrated with high on-current but with degraded sub-threshold slope^{3, 4, 5}. Recently, a comprehensive small-signal model was reported to accurately extract the interface state profile, the trap constant and the inversion channel charge in inversion mode III-V devices⁶. Here we present, for the first time, two equivalent circuit models for high-k gated strained InAs quantum well FETs depending on the location of the interface states (oxide-barrier interface or barrier-channel interface). The device studied here consists of strained InAs layer inserted in an In_{0.53}Ga_{0.47}As channel layer on a semi-insulating InP substrate. A schematic cross-section of the epi-structure and fabricated device is illustrated in Figs. 1(a)-(b). The device has 10 nm thick HfO₂ dielectric, 200 nm thick TaN gate electrode and PdGe source-drain contacts contact directly contacting the QW along the mesa edge. Measured transfer characteristics of InAs QWFETs at various temperatures are shown in Fig. 1(c).

The measured C-V and G-V characteristics of the QWFET (Figs. 3(c)-(d)) show large frequency dispersion due to the presence of interface states. This frequency dispersion could arise from the interface states present at (a) the oxide and barrier interface (Fig. 2(a)), or (b) the In_{0.53}Ga_{0.47}As and the strained InAs channel interface due to relaxation of the strained InAs layer (Fig. 3(a)). The equivalent circuits representing the effects of interface states at the oxide-barrier interface and In_{0.53}Ga_{0.47}As - strained InAs channel are shown in Figs. 2(b) and 3(b), respectively. The equivalent circuits were solved self consistently using the approach in reference 6 to obtain the interface state density (D_{it}), trap response time (τ) and the quantum well accumulation capacitance. Extracted trap response time as a function Fermi energy using **equivalent circuit I** indicates presence of Fermi level near both valence and conduction bands of the InAlAs barrier as the gate voltage is swept from -1V to 0V (Fig. 2(c)). Since the InAlAs stays depleted over entire V_g sweep as indicated by energy band diagram in Fig. 2(d), this scenario was discarded. The C-V and G-V solution obtained from the **equivalent circuit II** of Figure 3(b) by attributing the interface state response to the In_{0.53}Ga_{0.47}As - strained InAs channel interface is shown in Figs 3(c)-(d). Figure 4(a) shows a continuous Λ - shaped response of τ vs Fermi energy with Fermi level sweeping across the InAs bandgap of 0.35eV. This is also consistent with our energy-band simulations (Fig. 2(d)). Finally, the true accumulation charge in the InAs quantum-well is extracted as a function of V_g based on the equivalent circuit II and the true field dependent mobility is extracted at 300K and 200K. The present 300K mobility of 1,590 cm²V⁻¹s⁻¹ could be further improved in the future by preventing the suspected InAs strain relaxation and interface state generation at the barrier-channel interface.

References:

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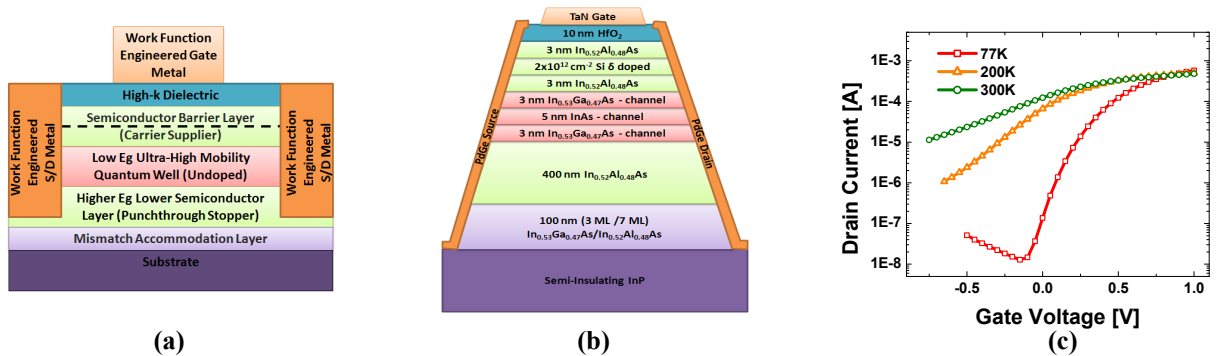


Figure 1. (a) Schematic of insulated gate quantum well FET (b) Multilayer epitaxial structure of the device (c) Experimental I_D - V_g characteristics vs temperature.

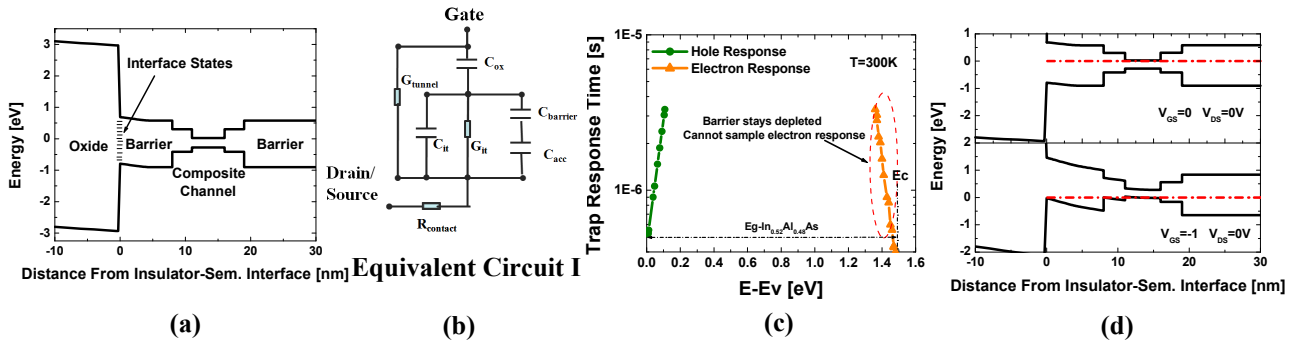


Figure 2. (a) Energy-band diagram showing interface states at the oxide-barrier interface (b) Equivalent small-signal model (c) Extracted trap response time showing the electron and hole response (d) Simulated energy-band profiles under the gate showing that the InAlAs barrier remains depleted as V_g is swept from 0V to -1V. (As the InAlAs barrier stays depleted, the electron response given by the model cannot be from the oxide-barrier interface)

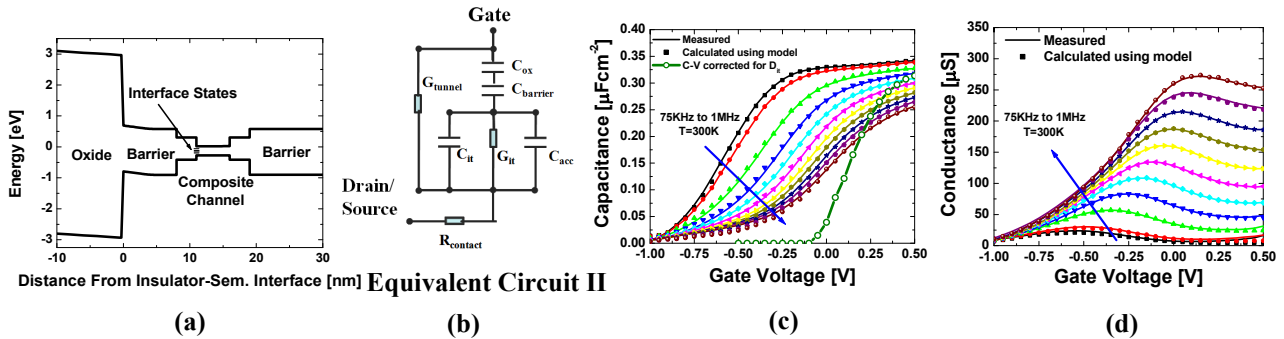


Figure 3. (a) Energy-band diagram showing interface states within composite channel due to strain relaxation (b) Equivalent small-signal model (c) Experimental C-V and (d) Experimental G-V data compared to the modeled data using the proposed equivalent circuit model. C-V data corrected for D_{it} is also shown in (c).

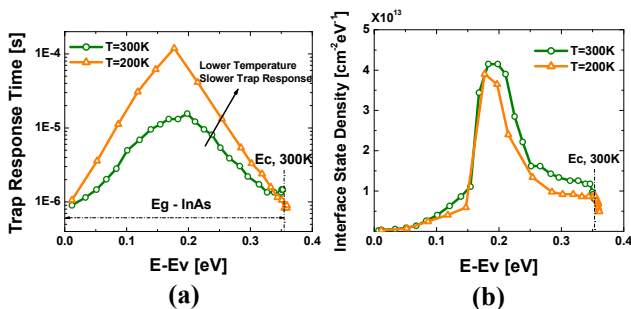


Figure 4. Extracted (a) Interface trap response time and (b) D_{it} .

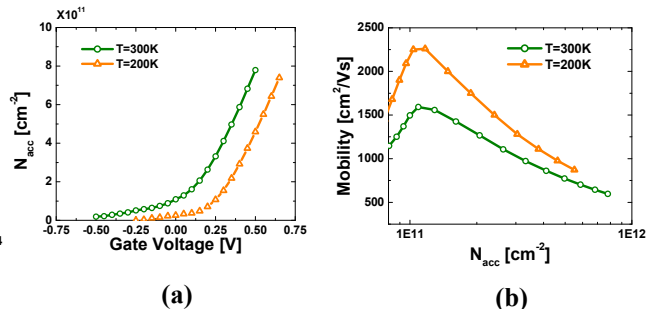


Figure 5. Extracted (a) Accumulation charge density and (b) Mobility.