Impact of Interface States on Sub-threshold Response of III-V MOSFETs, MOS HEMTs and Tunnel FETs

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Logic transistor scaling following Moore's Law over the last four decades has resulted in unprecedented increase in logic performance. However, rising transistor count has also led to increased energy consumption in modern VLSI. Thus, high mobility channel transistors (such as III-V) [1,2] and steep sub-threshold slope transistors [3] are needed in future to aggressively scale the supply voltage (Vcc) for logic transistors. High mobility quantum well FETs (QWFETs) (e.g. $In_{0.7}Ga_{0.3}As$ and InSb) have already been demonstrated at 0.5V Vcc with high performance [1,2], albeit with high gate leakage due to the Schottky gate. Efforts are underway to integrate a high quality high-k dielectric with III-V transistors. Recently, inversion mode $In_{0.53}Ga_{0.47}As$ MOSFETs with ALD Al_2O_3, HfO_2 and MBD $LaAlO_3$ oxides as well as insulated gate InGaAs MOS HEMT devices have been demonstrated[4,5]. Fig. 1 shows the benchmarking of the sub-threshold slope values in InGaAs based MOSFETs and MOS HEMTs with the former typically showing higher values than the latter [9]. In this work, we present a drift-diffusion based numerical simulation and analysis of the influence of interface states (D_{it}) present at the high-k dielectric and InGaAs interface on the sub-threshold response of 3 different types of transistor architecture: MOSFETs, MOS HEMTs and Tunnel FETs. Fig. 2(a) shows the experimentally measured D_{it} profile at the interface of an in-situ deposited $LaAlO_3$ high-k dielectric and $In_{0.53}Ga_{0.47}As$ interface. For simulation purpose, we approximate the D_{it} profile by a superposition of two exponential trap distributions (Fig. 2(b)) – the left distribution spanning across a large portion of the bandgap (left) and the right distribution extending into the conduction band. Figs. 3(a), (b) and (c) show the cross-section schematics of 3 different transistor architectures – an inversion mode surface channel $In_{0.53}Ga_{0.47}As$ MOSFET, an accumulation mode buried channel $In_{0.53}Ga_{0.47}As$ MOSHEMT with InAlAs barrier layer and an $In_{0.53}Ga_{0.47}As$-based interband tunnel FET. Figs. 4 (a)-(c) show the simulated transfer characteristics of the 3 devices along with their respective energy band diagrams and Fermi level movement as the devices turn on (Figs. 5 (a)-(c)). In MOSFETs, we identify 2 different regions for sub-threshold response: in the first region ($-1V < Vg < -0.54$ V), the Fermi level, E_F, sweeps the entire left distribution and causes severe degradation in sub-threshold slope (300mV/dec), while in the second region E_F spans one half of the right distribution up to its peak and the slope improves to 137mV/dec for a total $E_F$movement of 0.53V to turn the device on (Fig. 4(a)). It is to be noted that, since the second distribution extending into the conduction band has lower peak value, a high inversion charge and thereby a high on-current is expected in InGaAs MOSFETs, despite its poor sub-threshold slope. The donor and the acceptor character of the D_{it} also affects the threshold voltage, V_T, of the MOSFET with the latter causing a positive V_T shift. In MOS HEMTs, the sub-threshold slope is less affected by D_{it} than MOSFETs since the Fermi level moves by 0.4V through the first peak and does not even reach the second peak when the quantum well turns on (Fig. 5(b)). Finally, in the case of InGaAs TFETs, the Fermi level moves by a very little amount to turn the device on. Tunnel FETs turn on abruptly when the valence band edge in the p+ source region is raised above the conduction band edge in the channel which is already weakly inverted in the off-state, this gives rise to steep (<kT/q) sub-threshold slope. Fig, 5(c) shows that, even in the presence of interface states, the steep sub-threshold behavior is retained since the Fermi level sweeps the interface by only a small amount (~ 40mV) and primarily across the second D_{it} distribution which has lower peak density. In this work, we have shown how the same exact D_{it} distribution at the high-k/III-V interface can affect the sub-threshold response of different transistor architecture in dramatically different ways.

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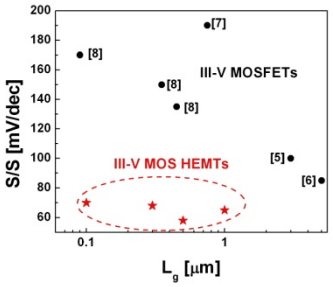


Figure 1. Benchmarking of sub-threshold slope in III-V MOSFET and MOS HEMT.

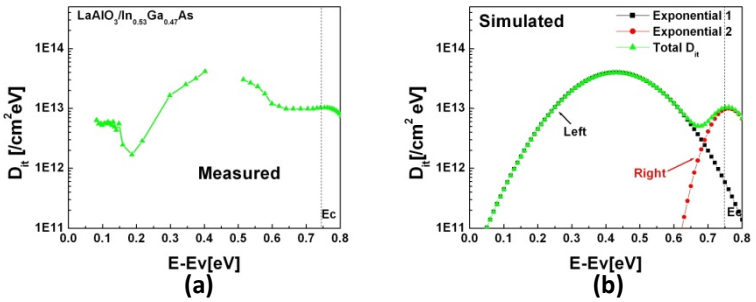
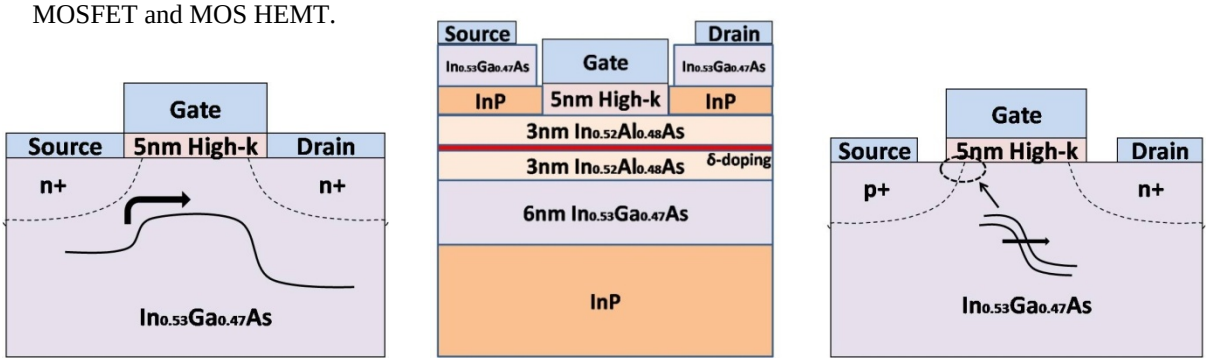
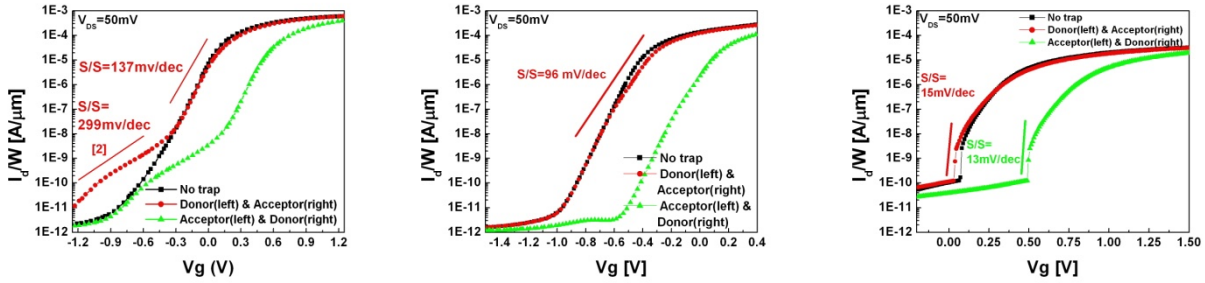


Figure 2. (a) Extracted D_{it} from experiential measurement. (b) D_{it} distributions used in simulations.



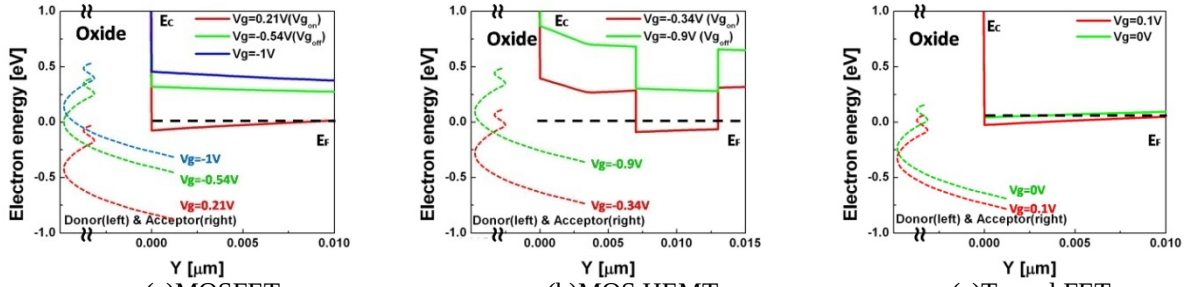
(a)MOSFET (b)MOS HEMT (c)Tunnel FET

Figure 3. Schematic of (a)$In_{0.53}Ga_{0.47}As$ MOSFET (b) $In_{0.53}Ga_{0.47}As$ MOS HEMT (c) $In_{0.53}Ga_{0.47}As$ Tunnel FET.



(a)MOSFET (b)MOS HEMT (c)Tunnel FET

Figure 4. I_d-V_g characteristics at low drain bias for the (a) $In_{0.53}Ga_{0.47}As$ MOSFET, (b) $In_{0.53}Ga_{0.47}As$ MOS HEMT and (c) $In_{0.53}Ga_{0.47}As$ Tunnel FET.



(a)MOSFET (b)MOS HEMT (c)Tunnel FET

Figure 5. Energy-band diagram with Dit distribution at the oxide-semiconductor interface (shift left for clarity) for (a) $In_{0.53}Ga_{0.47}As$ MOSFET, (b) $In_{0.53}Ga_{0.47}As$ MOS HEMT and (c) $In_{0.53}Ga_{0.47}As$ Tunnel FET at different gate voltage. Here V_{on} is V_g when E_F-E_C=3kT.