Band-gap Engineered Hot Carrier Tunnel Transistors

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Inter-band tunnel field effect transistors (TFETs) with a gate controlled zener tunnel junction at the source are of interest because of its ability to operate with sub-kT/q sub-threshold slope device operation over a specified gate bias range [1,2]. This allows TFETs to achieve, in principle, much higher I_{ON}-I_{OFF} ratio over a given gate voltage swing compared to conventional MOSFETs, making them attractive for ultra-low power operation. We present here a study on the strong non-equilibrium character of the tunnel injected carrier population in the channel of the TFETs through detailed energy balance (EB) simulations [3,4] and its implication on TFET device design. We specifically show the following: (i) A large and highly inhomogeneous electric field at the source side tunnel junction at high gate voltages results in a non-equilibrium distribution of injected carriers in the TFET channel (ii) A novel source side heterojunction design enhances and sharpens the source side electric field amplitude and shape resulting in greater carrier heating and band-to-band tunneling (BTBT) currents even at moderate gate voltages (iii) The energy relaxation process of the injected carriers on both sides of the tunnel barrier are studied as a function of bias conditions and is a strong function of the 2-dimensional electric field profile in the TFET channel.

The n-channel DG TFET/MOSFET (Fig. 1) used in this study have a gate length, L_G of 30 nm and 2.5 nm thick HfO_2 gate dielectrics. The typical body thickness (T_{body}) is kept at 7 nm. Gaussian doping profiles of peak density 1e20 cm^{-3} and gradients of 2nm/decade are used for the source (p^+) and drain (n^+) regions; channel doping is kept at 1e15 cm^{-3}. In MOSFETs the p^+ source is replaced with n^+ doping. Fig.2 compares the carrier energy distribution for Si TFET and MOSFET under high gate and drain bias (V_{GS}=V_{DS}=1V). An average value of 0.3 ps and 0.25 ps is used for the electron and hole energy relaxation rates in silicon. Fig 2(a) and (b) show that in a n-type Si MOSFET the carriers (electrons, unipolar device) are gradually heated in the channel via the drift field and finally relax on entering the drain. In contrast, TFET (Fig 2(c) and (d)) is a bipolar device with a large electric field at the source end resulting in a heated distribution of BTBT induced electrons in the channel conduction band and holes in the p+ source region valence band. Fig 3 compares the I_{DS}-V_{GS} (V_{DS}=1V) characteristics computed via drift diffusion (DD) and Energy Balance (EB) simulation. EB predicts a 1.36X higher ON current for MOSFET (fig 3(a)) and a 6X higher ON current for TFET (fig 3(b)) compared to DD. Fig 4(a) shows a lower band-gap source (p+ $Si_{0.7}Ge_{0.3}$) TFET design with p- Si channel and n+ drain having a 2 nm gate-source and drain overlap regions (the SiGe source (SGS) design). Fig 4(b) compares the I_{DS}-V_{GS} characteristics obtained via DD and EB simulation, in this case EB predicts a 3.3X higher ON current. The carrier heating effects for SGS design begins at V_{GS}=0.16 V. In order to further reduce the characteristic gate bias for carrier heating a novel heterojunction source design (Fig 5(a), Displaced SGS (DSGS)) is proposed, here the p+ doping is physically shifted from the heterojunction edge by 2 nm. Fig 5(b) shows that the EB predicts a 3.2X higher ON current (I_{ON} = 1.56 mA/um) compared to DD (I_{ON} = 487 μA/μm) with the characteristic gate bias for carrier heating at V_{GS}=0.08V. At V_{GS}=0.16 V, DSGS TFET design results in 10X improvement in ON current over SGS design due to enhanced carrier heating at lower gate biases. This is primarily due to the enhancement and sharpening of the electric field profile in the source side tunnel junction (fig. 6). Fig 7 shows the electric field profile and electron temperature along the entire length of the device for low and high gate bias. Under high gate bias (fig 7(a)) the tunneling carrier (hole like in source valence band and electron like in channel conduction band) is accelerated in the source electric field and appears as a hot carrier electron distribution on the channel side and then relaxes gradually along the channel (fig 7(b)). Under low gate bias (fig 7(c)) the electric field re-distributes itself resulting in large electric field at the source-channel and the drain-channel interface causing the carriers (electrons) to heat at both ends of the channel and, as a result, maintaining a hot carrier distribution all throughout the length of the channel and relaxation occurs only in the drain (fig 7(d)). This explains the higher ON current enhancements predicted by EB over DD at low gate voltages.

In conclusion, this letter clearly elucidates the importance of non-equilibrium hot carrier transport in tunnel transistors through EB simulations and shows that unlike DD, a large and highly inhomogeneous electric field at the source tunnel junction leads to considerable carrier heating and non-equilibrium carrier distribution which results in enhanced band to band tunneling current for both low and high gate voltages. It was shown that novel heterojunction source design like the DSGS TFET could be used to exploit this carrier heating effect and boost the ON-current of tunnel transistor. This work provides the incentive to study this hot carrier effect in greater detail and further explore novel device designs to realize the full potential of tunnel transistors.

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[3] T. Grasser et al., *Proc. of the IEEE*, **91**, 251, (2003).
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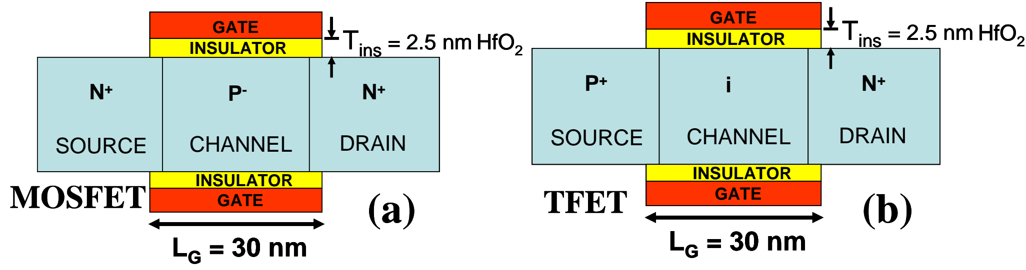

Fig 1. Simulated Device Schematic (a) MOSFET (b) TFET

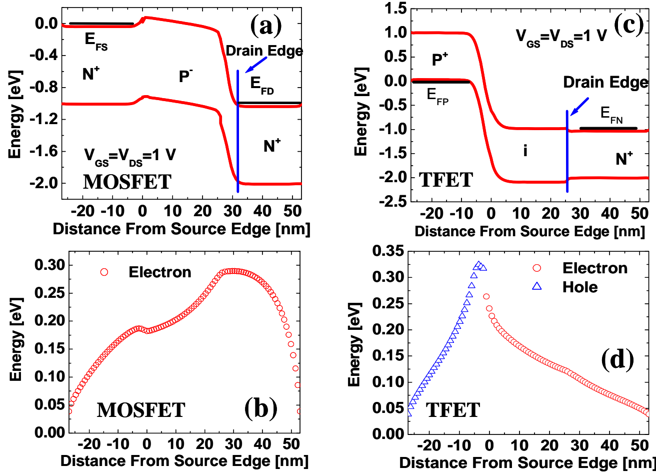

Fig 2. (a) Si MOSFET band diagram under high gate and drain bias (b) Electron energy along the length of the device (c) Si TFET band diagram under high gate and drain bias (d) Electron and Hole energy

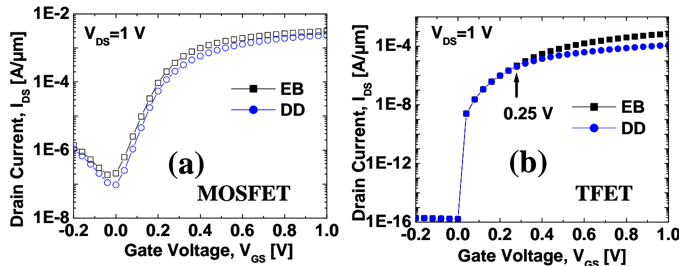

Fig 3. (a) Si MOSFET and (b) Si TFET I_{DS}-V_{GS} at V_{DS}=1V for Energy Balance (EB) and Drift Diffusion (DD) simulation

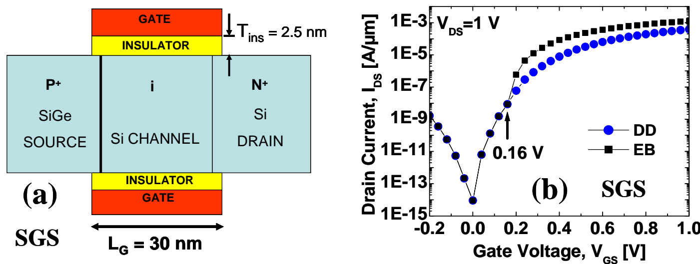

Fig 4. (a) $Si_{0.7}Ge_{0.3}$ source (SGS) device schematic (b) SGS I_{DS}-V_{GS} at V_{DS}=1V for Energy Balance (EB) and Drift Diffusion (DD) simulation

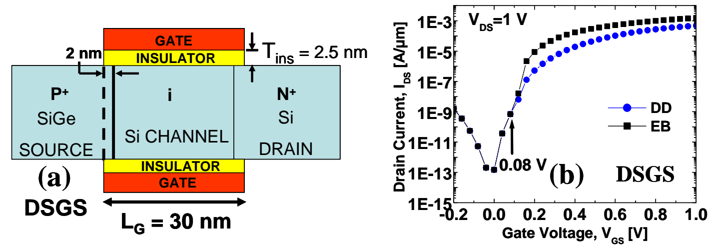

Fig 5. (a) Displaced Si0.7Ge0.3 Source (DSGS) schematic wherein the doping edge is moved away from the heterojunction edge by 2 nm (b) DSGS I_{DS}-V_{GS} at V_{DS}=1V for Energy Balance (EB) and Drift Diffusion (DD) simulation

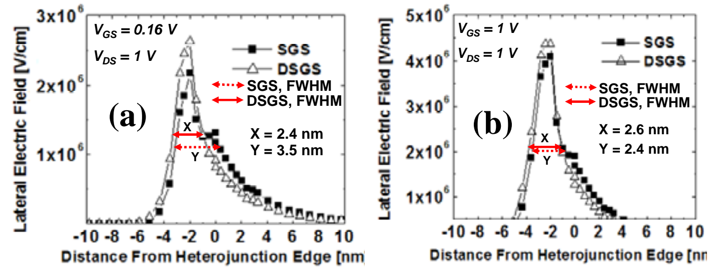

Fig 6. Lateral Electric Field at the source side tunnel junction for (a) Low gate bias (b) High gate bias. FWHM (Full width half maximum) signifies the rapid change of the electric field profile at the tunnel junction.

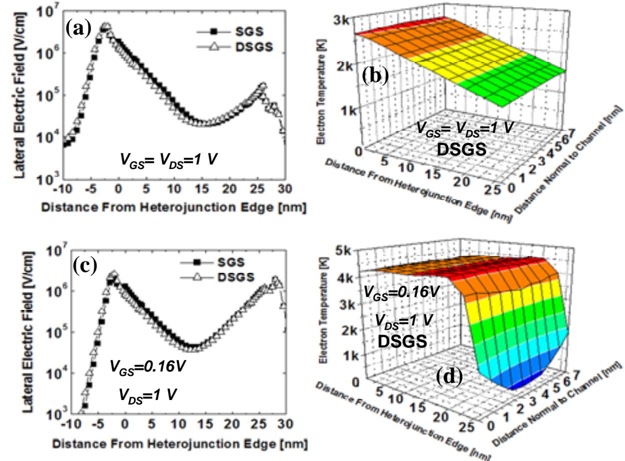

Fig 7. (a) Electric Field and (b) Electron temperature along the device under high gate bias. (c) Electric Field and (d) Electron Temperature along the device for low gate bias.