HfO_2 Gated, Self Aligned and Directly Contacted Indium Arsenide Quantum-well Transistors for Logic Applications – A Temperature and Bias Dependent Study

A. Ali[1], S. Mookerjea[1], E. Hwang[1], S. Koveshnikov[2,3], S. Oktyabrsky[2], V. Tokranov[2],
M. Yakimov[2], R. Kambhampati[2], W. Tsai[3] and S. Datta[1]
[1]The Pennsylvania State University, University Park, PA 16802, USA
[2]University at Albany – SUNY, Albany, NY 12203, USA; [3]Intel Corporation, Santa Clara, CA 95052, USA
Phone: (814) 777 3160, Fax: (814) 865 7065, E-mail: aua176@psu.edu

III-V compound semiconductors with extremely high mobilities have recently emerged as a potential technology of choice for future beyond-Si CMOS logic applications [1]. InAs PHEMT (on InP) containing an InAs strained layer inserted in an $In_{0.53}Ga_{0.47}As$ channel layer has been demonstrated with improved scalability and performance [2], albeit with Schottky gate and non self aligned source drain contacts. This is unsuitable for future VLSI logic applications. Here, we integrate, for the first time, an in-situ deposited high-k dielectric (HfO_2) and metal gate (TaN) stack with the InAs quantum-well device layers incorporating Pd/Ge source-drain contacts fully self-aligned with the gate edge and contacting the quantum-well directly. A bias and temperature dependent experimental study of the off-state leakage and the carrier transport identifies the various physical mechanisms limiting the device performance.

The process flow starts with the multi-layer epitaxial growth of InAs inserted $In_{0.53}Ga_{0.47}As$ quantum-well device layers on a semi-insulating InP substrate using Molecular Beam Epitaxy. A cross-section of the epi-structure is illustrated in Fig. 1. The epi-wafer was then transferred under ultra-high vacuum conditions into an oxide deposition chamber where 10 nm thick HfO_2 dielectric was deposited by electron beam evaporation of metallic hafnium (Hf) in an oxygen ambient at about 10^{-6} Torr. The epi-structure with the insulated dielectric in place was taken out of vacuum and annealed (in some cases). Hall measurements (Fig. 3) show the average room temperature mobility of the annealed samples in the range of 1,200-1,600 $cm^2V^{-1}s^{-1}$ with 2DEG concentrations of $2\text{-}3x10^{12}$ cm^{-2}. This is followed by 200 nm thick TaN gate metal deposition using magnetron sputtering followed by anneal at 600C for 5min. A single step optical photolithography is used to pattern ring-like FET gate patterns, followed by a chlorine-based dry reactive ion etch to form a trapezoidal shaped mesa structure (Fig. 2). Without removing the photoresist, PdGe source drain (S/D) contacts were evaporated and then lifted-off to contact the epi-structure along the mesa edge. A slight undercut etch of the TaN layer prior to that prevents source/drain to gate shorts. S/D PdGe contacts are finally annealed at 400C for 30sec to form fully self-aligned source drain ohmic contact to the quantum-well. It should be noted that two mono-layer thick $In_{0.53}Ga_{0.47}As$ was incorporated above the InAlAs barrier layer to reduce the Dit by at least 10x as compared to InAlAs/HfO_2 interface. Numerical simulation reveals the location of the 2DEG spread over the InAs quantum-well as well as the InGaAs cladding layers (Fig. 4).

We performed DC and AC characterization of the IG-QWFETs from room temperature down to 5K. Figs. 5, 6 show the transfer and the gate leakage characteristics of the IG-QWFETs as a function of temperature. Both off-state and gate leakage currents improve dramatically as temperature is reduced. An Arrhenius plot of the off-state leakage reveals a thermionic component with an activation energy barrier of 32 meV above 50K while it is limited by gate tunneling leakage below 50K (Fig. 7). The activation energy is much less than *Eg/2* (~170meV) and indicates the existence of defects within the epi-structure that pins the Fermi level close to InAs conduction band. Figs. 8(a) and (b) show the simulated and measured C-V characteristics of the devices as a function of temperature. The existence of a parasitic channel at low V_{GS} is evident from the room temperature experimental CV data. Further, at high V_{GS}, the C-V kink occurs due to neutralization of the donors and the appearance of carriers in the barrier layer close to the HfO_2 interface [3]. Fig. 9 shows the extracted carrier density (simulated and experimental) as a function of V_{GS} at 300K and 77K. The effective channel mobility in the InAs IG-QWFETs is extracted from the output characteristics (Fig. 10) under low drain bias in conjunction with the extracted carrier densities at different temperatures and at various gate biases. The increase in the on-state current with reducing temperature is evident from Fig. 11. The extracted mobility numbers are also corrected for the external resistances at each temperature step (Fig. 12). Fig. 13 reveals that the mobility increases monotonically with decreasing temperature as $T^{-1.5}$ in 150K<T<300K and as T^{-1} at 50K < T <150K limited by phonon scattering (from the soft optical phonons of the high-k dielectric). At low gate biases and low temperature (<50K) where carrier screening is the weakest, Coulombic scattering due to the defect states dominates.

In summary, we have demonstrated an insulated gate quantum-well transistor architecture using InGaAs/InAs quantum well with an HfO_2/TaN gate stack and self aligned ohmic contacts directly contacting the quantum-well. Temperature dependent measurements indicate a high mobility limited by phonon scattering is achievable under moderate to high gate field making it another promising device architecture for future VLSI logic applications.

[1] R. Chau et al., IEEE Trans. Nano., pp. 153-158 (2005). [2] D. H. Kim, J. del Alamo, IEDM Tech Dig., pp. 719 - 722 (2008).
[3] M. A. Aziz et al , Solid State Electr., pp. 891 – 900 (1999).

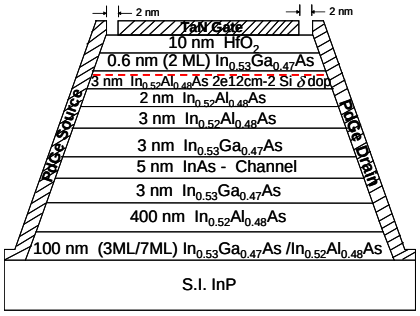

Fig 1. Cross-section of device schematic

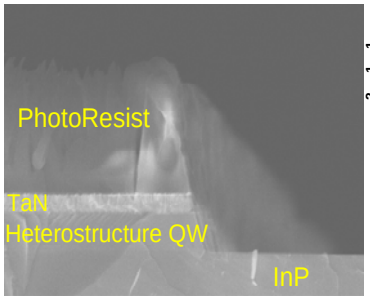

Fig 2. Cross-section SEM picture after mesa etch

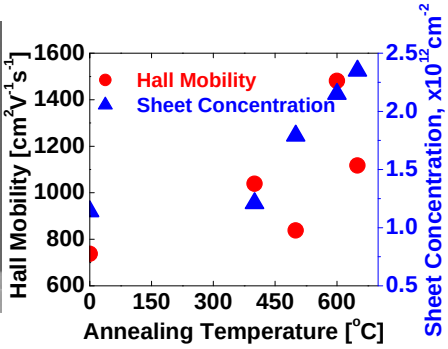

Fig 3. Room temperature Hall measurement data

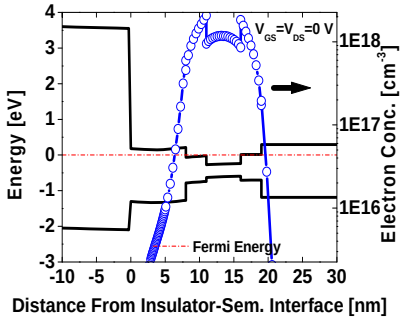

Fig 4. Energy band diagram and carrier density profile under the gate

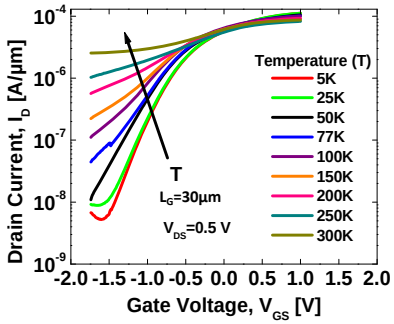

Fig 5. I_D-V_{GS} at V_{DS} = 0.5 V of InAs IG-QWFET at different temperatures

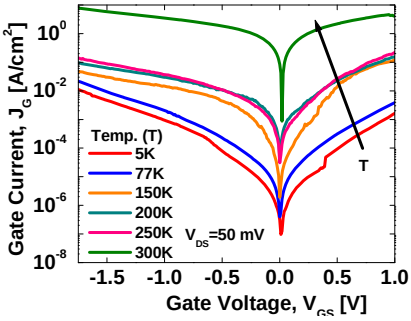

Fig 6. J_G-V_{GS} at V_{DS} = 0.05 V of InAs IG-QWFET at different temperatures

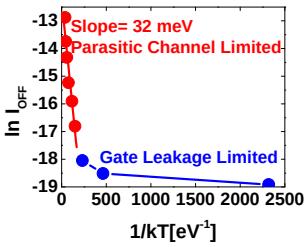

Fig 7. I_{OFF} vs temperature

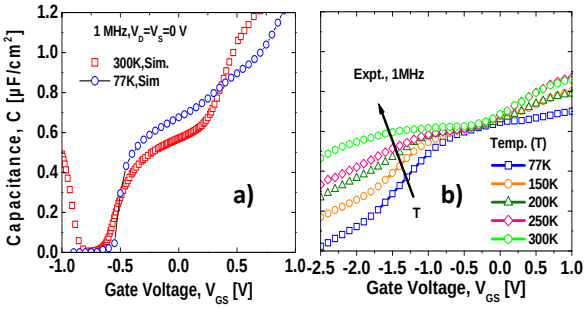

Fig 8. a) Simulated and b) experimental CV characteristics

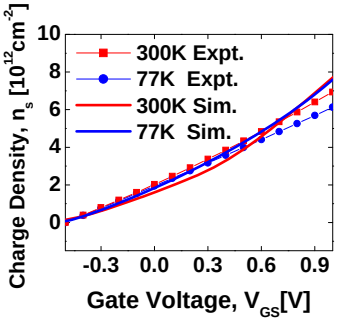

Fig 9. Carrier density vs V_{GS}

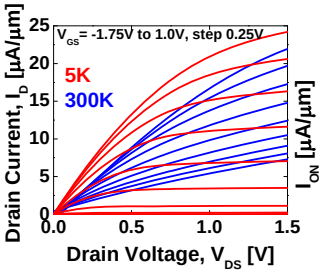

Fig 10. I_D vs V_{DS} at 5K and 300K (L_G = 20 μm)

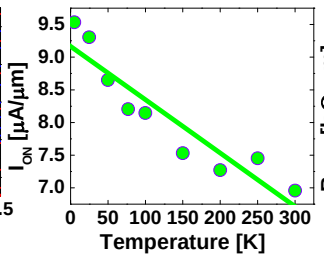

Fig 11. I_{ON} vs temperature (L_G = 30 μm)

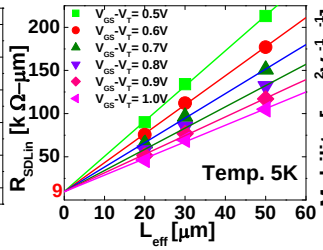

Fig 12. R_{SD} vs L_{eff} at 5K

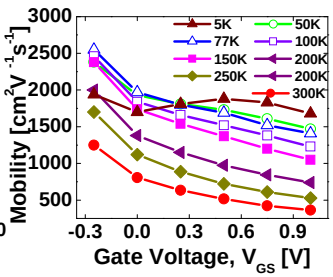

Fig 13. . Extracted mobility vs gate voltage, V_{GS}, for different temperatures