Inter-band Tunnel Transistor Architecture using Narrow Gap Semiconductors

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The inter-band tunnel transistor (TFET) architecture features a sub-kT/q sub-threshold slope operation and can potentially support high I_{ON}/I_{OFF} ratios over small gate voltages. Based on two-dimensional numerical simulations, we investigate TFET in various material systems ranging from silicon to indium arsenide. TFET performance can be enhanced when heterojunctions are employed at the source side to enhance tunneling, nonequilibrium carrier population is maintained in the channel and one dimensional tunneling junction are incorporated. Mixed mode circuit simulations using TFETs highlight the impact of feed forward gate-to-drain capacitance in these devices during transient switching operation and reveal important differences with MOSFETs. Narrow gap semiconductors with low density of states are projected as viable candidates to implement TFET architecture in sustaining an aggressive supply voltage scaling roadmap for future digital logic applications.

Introduction

Continued miniaturization of the silicon CMOS transistor technology, has resulted in an unprecedented increase in single-core and multi-core performance of modern-day microprocessors. However, the exponentially rising transistor count has also increased the overall power consumption, making performance per watt of energy consumption the key figure-of-merit for today's high-performance microprocessors. Today, energy efficiency serves as the central tenet of high performance microprocessor technology at the system architecture level as well as the transistor level ushering in the era of energy efficient nanoelectronics. Aggressive supply voltage scaling while maintaining the transistor performance is a direct approach towards reducing the energy consumption since it reduces the dynamic power quadratically and the leakage power linearly. To that effect, narrow gap compound semiconductor-based (e.g. indium antimonide, indium arsenide and $In_xGa_{1-x}As$) inter-band tunnel transistor (TFET) architecture could enable the next generation of logic transistors operating below 0.5 V supply voltage. In this invited paper, we present a comprehensive study of the basic TFET architecture, the optimum materials choice to improve TFET performance, the advanced TFET architectures and, finally, the transient response of the TFETs in a digital circuit configuration.

Inter-band Tunnel Transistor

Inter-band tunnel field effect transistors (TFETs) with a gate modulated zener tunnel junction at the source have recently attracted a great deal of interest, both theoretically and experimentally [1]-[7]. Figure 1 shows a schematic of an n-channel TFET architecture which incorporates a highly doped p+ source region, a near intrinsic channel

region and n+ drain region. The n-channel TFET operates on the principle of band to band tunneling of electrons across the source to channel tunnel junction under the influence of a gate electric field. The major advantage of the TFETs in comparison with the metal-oxide-semiconductor field-effect transistors (MOSFETs) is that the reverse biased tunnel junction in the former eliminates the high energy tail present in the Fermi-Dirac distribution of the valence band electrons in the p+ source region and allows sub-kT/q sub-threshold slope device operation over a certain gate bias range near the off-state. This allows TFETs to achieve, in principle, much higher I_{ON}-I_{OFF} ratio over a given gate voltage swing compared to the MOSFETs, making the TFET architecture an attractive vehicle to implement low supply voltage (V_{DD}) digital logic circuits.

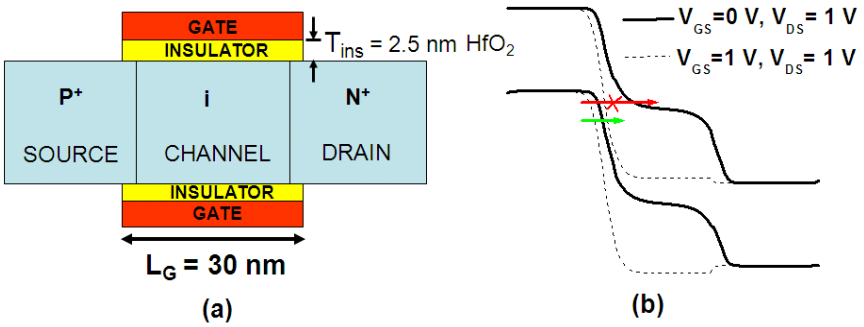

Figure 1. a) Schematic of a double gate inter-band tunnel transistor (TFET) architecture; (b) Energy band diagram illustrating the TFET ON and OFF state conditions

Figure 2 shows the transfer characteristics of a silicon (Si) double gate 30 nanometer gate length TFET benchmarked against a Si MOSFET of identical dimensions, both operating under 1V supply voltage. The very low off-state current of the TFET is set by the reverse bias saturation current of the p-i-n diode. Near the off-state, the TFET clearly exhibits < 60mV/decade which results in a vastly superior I_{ON}-I_{OFF} ratio compared to the MOSFETs. However, the on current in a TFET is significantly lower than its MOSFET counterpart being limited by the low transmission rate of electrons across the reverse biased tunnel junction between the source and the channel. The band to band tunneling transmission rate is a strong function of the height and width of the tunnel barrier. The height of the barrier is set by the semiconductor bandgap while the width of the barrier is set by the magnitude of the junction electric field as well as the bandgap (Figure 3a).

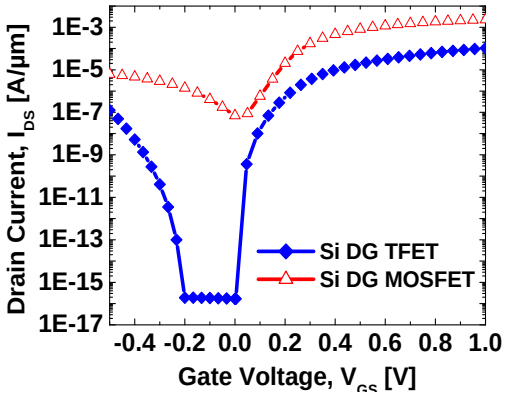

Figure 2. Transfer characteristics of 30nm gate length double gate silicon TFET compared against a silicon MOSFET operating under 1V supply voltage

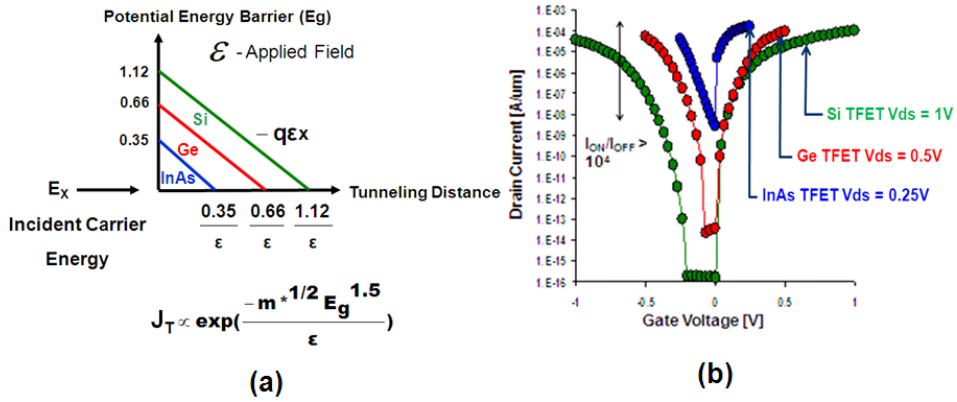

Figure 3. (a) Schematic of a tunnel barrier in various semiconductors (b) Transfer characteristics of double gate TFETs in Si, Ge and InAs semiconductors under various supply voltages

It is evident that narrow gap semiconductors such as Ge and InAs can significantly enhance the source side tunneling rate due to the combined effects of reduced barrier height and shorter tunneling distance in addition to the reduced tunneling mass. Figure 3(b) compares the transfer characteristics of Si, Ge and InAs TFETs under various supply voltages. The InAs TFET shows the highest on current (275 µA/µm) at the lowest supply voltage of 0.25V with an I_{ON}/I_{OFF} ratio exceeding $4x10^4$. However, the InAs TFETs also exhibit strong ambipolar characteristics due to the tunneling of carriers from the drain into the channel at negative gate voltages. This warrants the need for other advanced tunnel transistor architecture in addition to introducing the narrow bandgap semiconductors to enhance its overall performance and its energy efficiency.

Enhancing Tunnel Transistor Performance

Recent experimental and thermal equilibrium based drift-diffusion studies of silicon-based TFETs suggest that the on-state performance of TFETs will always be inferior to conventional MOSFETs due to the limitation in the band to band tunneling rate in large and indirect bandgap silicon [5-8]. Although narrow gap semiconductors enhance the TFET on-current by increasing the source side tunneling rate, the drain side tunneling is also enhanced leading to ambipolar current voltage characteristics. Here we explore three advanced TFET architecture concepts that can potentially enhance TFET on-current while retaining its energy efficiency.

Heterojunction Tunnel FET

The use of a heterojunction incorporating a narrower bandgap silicon germanium (SiGe) in the source region [9] or a thin delta doped region [10] between the source and channel has been shown to significantly enhance the tunneling rate and on-current. Figure 4(a) shows the tunnel current density as a function of the junction voltage for a homojunction lattice matched $In_{.53}Ga_{.47}As$ p+/n+ tunnel junction and a $In_{.53}Ga_{.47}As$/InAs p+/n+ tunnel heterojunction. The thin InAs insert near the source-channel junction reduces the effective tunnel barrier leading to a higher tunneling rate while the higher bandgap $In_{.53}Ga_{.47}As$ matrix reduces the drain side tunneling thereby suppressing the ambipolar behavior. The doping and thickness of the InAs insert need careful

optimization as illustrated in Figure 4(b) in order to preserve the steep sub-threshold slope behavior. While the n+ doped InAs insert increases the electric field at the junction and the emission thereby degrading the sub-threshold characteristics. On the other hand, a p doped InAs pocket of similar thickness stays fully depleted in the off-state and maintains low leakage current.

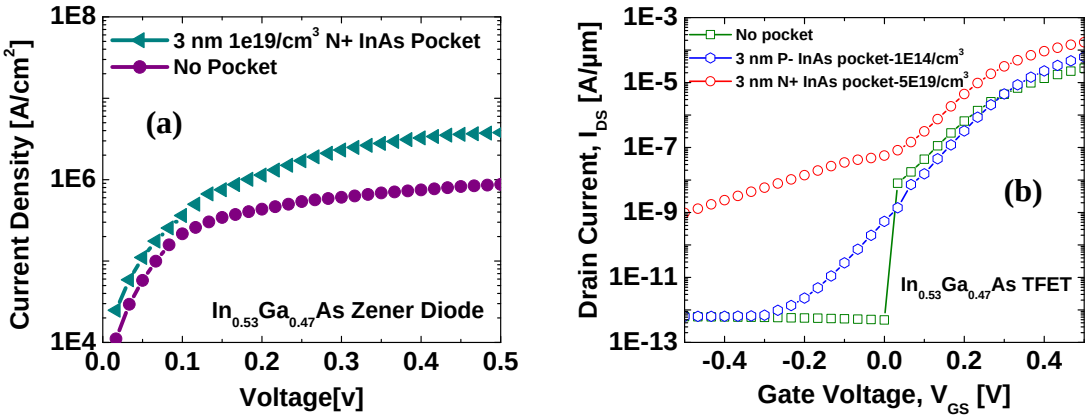

Figure 4. (a) Tunnel current density vs. voltage in homojunction and heterojunction $In_{.53}Ga_{.47}As$ tunnel junctions (b) Transfer characteristics of homojunction and heterojunction $In_{.53}Ga_{.47}As$ TFETs with n+ and p doped InAs inserts.

Nonequilibrium Carrier Transport

In the on-state (i.e. at high gate voltage) the electric field at the source side tunnel junction in TFETs often exceeds 1MV/cm leading to significant carrier heating and a nonequilibrium carrier distribution. We find that nonequilibrium carrier effects positively impacts the band to band tunneling rate in TFETs particularly with heterojunction tunnel source (Figure 5(a)). Through self consistent energy balance simulation we find that, the TFET transfer characteristics, particularly its on-current performance, is significantly improved over a large gate bias range by tailoring the shape of the tunnel barrier potential which enhances the junction electric field and the carrier heating effects (Figure 5(b)).

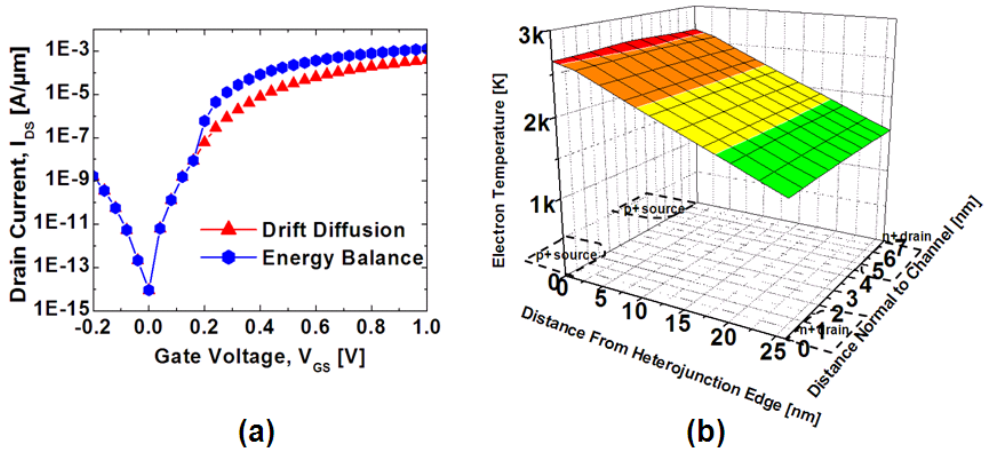

Figure 5. (a) Transfer characteristics of heterojunction TFET with (energy balance) and without carrier heating (drift-diffusion) (b) Electron temperature profile along the channel of a heterojunction TFET at $V_{GS} = V_{DS} = 1V$ showing significant carrier heating at the source side

One Dimensional Nanowire Tunnel FET

The transverse momentum and energy need to be conserved in the band to band tunneling process. This leads to an effective increase in the both the barrier height and the width in bulk tunnel junctions as shown in Figure 6(a) [11,12]. The incorporation of one dimensional nanowire geometry within the tunnel FET configuration provides another knob to modulate the tunneling efficiency and improve the tunneling rate. Axially doped nanowires are being investigated to realize high performance TFETs (Figure 6(b)).

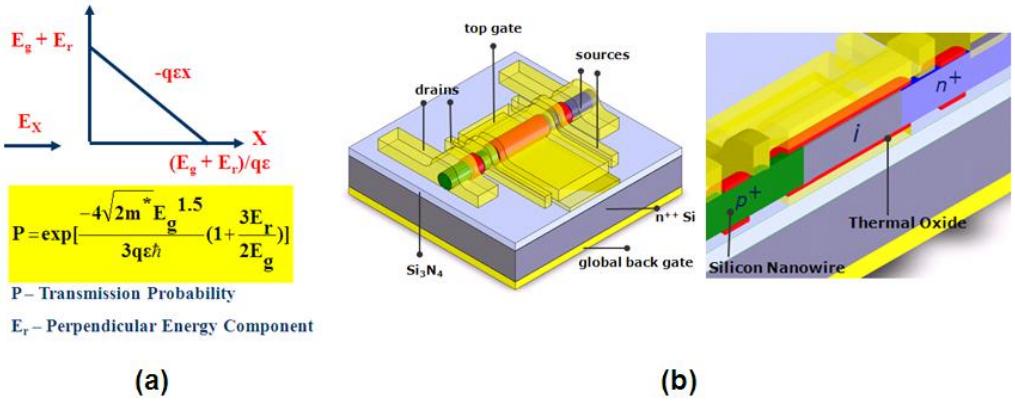

Figure 6. (a) Effective tunnel barrier profile when conservation of the transverse energy of the carriers is considered (b) Axially doped p+ i n+ nanowire tunnel FET

Transient Response of TFET

TFET based digital inverter circuit can be constructed using an n-channel and p-channel TFETs (Figure 7(a)). Figure 7(b) compares the transient response of silicon TFET with their MOSFET counterparts. Due to the presence of the source side tunneling

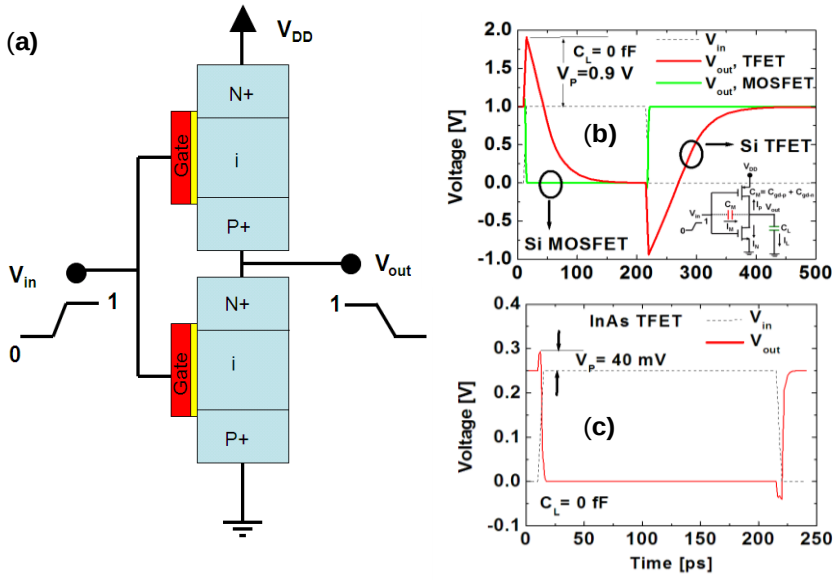

Figure 7. (a) Schematic of a TFET inverter (b) Transient response of a Si TFET inverter compared with a Si MOSFET inverter (c)Transient response of an InAs TFET inverter

barrier in silicon TFETs the gate capacitance is entirely reflected by the gate-to-drain capacitance which acts a feedforward element during switching and results in large voltage overshoot/undershoot in its switching characteristics. This adversely impacts the performance of TFETs for digital logic applications [13]. It is shown in Figure 7(c) that TFETs based on lower bandgap and lower density of states materials like InAs show significant improvement in switching behavior since the source side tunnel barrier is more transparent and both gate-to-source and gate-to-drain capacitances contribute to the gate capacitance. Furthermore, the gate capacitance is limited by the quantum capacitance of the InAs channel which results in much lower voltage overshoot/undershoot in the transient characteristics (Figure 7(c)). The higher ON current at reduced supply voltages result in sub-picosecond delay in InAs TFET based inverters making them viable for future energy efficient digital logic applications.

Acknowledgments

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