Ultra Low Power Signal Processing Architectures

Enabling Next-Generation BioSensing and Biomimetic Systems

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***Abstract*—An increasing integration of nanoscale sensors is being observed in BioSensing and Biomimetic systems. Power consumption is deemed a major limiter as the complexity of integration increases. Supply voltage based scaling using CMOS is also a challenge due to increasing leakage currents. This work presents alternative devices – Interband Tunnel Field Effect Transistors (TFETs) and Split-Gate Quantum Nanodots to achieve further scaling.**

Keywords-Interband Tunnel FETs, Split-Gate Quantum Nanodots, Single Electron Transistors (SETs), Reconfigurability.

I. INTRODUCTION

The ability for electronics to mimic and augment biological functions has been greatly enhanced by the integration of nanoscale sensors with signal processing circuitry on a single chip. For example, the integration of hundreds of nanoscale sensors on a single chip to mimic olfactory systems of mammals has several application domains including homeland security and the food and drug industry. Our prior work [1] that involved the design of a nanosensor array-based gas discrimination system demonstrated that nanoscale dimensions of the sensor provides better sensitivity to detect minuscule traces of target analytes and reduces power consumption. A key challenge to the design of more powerful smart sensors in future is the limitations on power consumption of the signal processing circuitry. Power consumption is a major limiter as it determines the life-time of battery (which is critical in implantable devices) and determines the heat dissipation (which determines viability of implanting the device in biological systems).

The difference between the supply voltage and the threshold voltage influences the drive current and, hence, the device performance. Due to the nonscalability of the threshold voltage limited by the device electrostatics and the nonscalability of the silicon dioxide gate dielectric due to tunneling induced leakage, supply voltage scaling is challenging with traditional CMOS transistor architecture.

Fig. 1 shows several generations of energy-efficient device architectures that have been developed by addressing these fundamental limitations to supply scaling in traditional CMOS structures. By introducing a new gate stack with high-K dielectrics and metal gate electrodes, constant inversion charge was achieved with lower supply voltage with same gate oxide-thickness. The improvement of device electrostatics through the introduction of multigate control structures enabled further lowering of supply voltage without sacrificing performance. Incorporation of ultra-high mobility compound (III-V) semiconductors along with corresponding changes in the device channel structure enables supply voltage reduction to below 500mV with excellent switching performance at reduced gate over drive. Our ongoing research focuses on further reducing the supply voltage to below 250mV supply voltage and below through abrupt turn-on (as opposed to a slower turn-on in traditional CMOS devices) exploiting the phenomena of inter-band tunneling in a novel vertical transistor (TFET) architecture. This device architecture also has a major influence on reducing the interconnect power consumption due to the smaller footprint resulting from its vertical orientation. We expect the TFETs to show better energy-delay performance than conventional CMOS circuits operated at sub-threshold voltage due to the abrupt turn-on characteristics. Section 2 of this paper provides an overview of this research.

Reducing the supply voltage further to 50mV and below requires a radically new approach towards device design and system architecture. The ultra-low voltage operation in the single or few electron regimes require a complete rethink of traditional circuit design to avoid high fan-out structures and contact related parasitic loss.

In this work, we propose a novel Binary Decision Diagram (BDD) based reconfigurable logic architecture that uses III-V compound semiconductor based split-gate controlled quantum nanodots which operate based on Coulomb blockade. Section 3 of this paper focuses on this architecture.

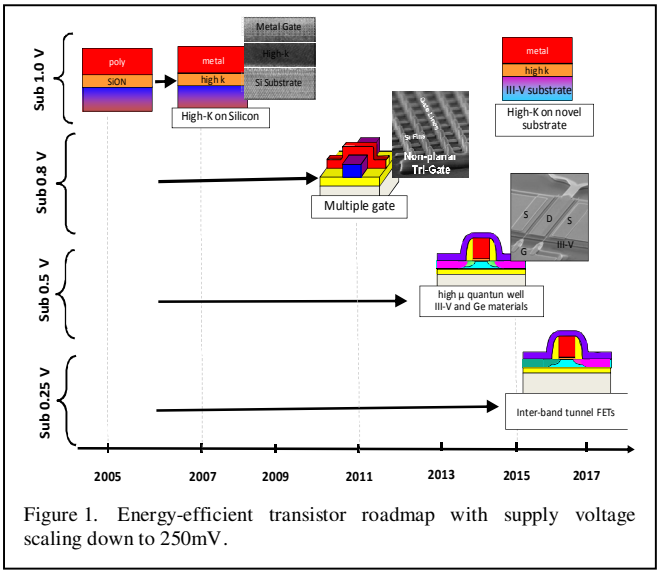

Figure 1. Energy-efficient transistor roadmap with supply voltage scaling down to 250mV.

II. INTER-BAND TUNNEL FETS

A. *Basic Device Structure*

With the continued miniaturization of MOSFETs, the OFF-state leakage current (I_{OFF}) is exponentially increasing due to the nonscalability of the threshold voltage imposed by the fundamental 60 mV/decade sub-threshold swing at room temperature. Sub-threshold swing refers to the change in

voltage required at the gate electrode of the transistor to change the source to drain current by one decade. Interband tunnel transistor [2] features sub-60mV/dec sub-threshold slope operation and can be used to circumvent the above fundamental limitation. Tunnel transistors operate via interband tunneling of electrons from the valence band into the conduction band across a reverse biased p+/n+ junction induced by a vertical gate field. Fig. 2a illustrates the TFET device architecture along with the electron current density profile. The tunnel current originates near the dielectric/channel interface at the source side due to the high electric field and rapidly spreads into the bulk. The band-to-band tunneling induced turn-on ensures steep room temperature sub-threshold slope for the TFETs compared to conventional MOSFETs but also results in low I_{ON} limited by the tunneling rate, particularly in indirect bandgap silicon (Fig. 2b). Narrow gap semiconductors such as germanium (Ge) and indium arsenide (InAs) enhance the tunneling rate considerably due to the lower barrier height as well as shorter tunneling distance (Fig. 2c) and allow for aggressive V_{CC} scaling as shown by the transfer characteristics. The InAs TFETs can exhibit I_{ON}-I_{OFF} ratio > 10^4 over a limited gate swing of only 0.25V making it a highly energy efficient logic transistor.

In fact, the InAs TFETs show the maximum benefit when their supply voltage V_{CC} is scaled aggressively down to 0.25V and this benefit primarily arises from a) efficient tunneling under low electric field and b) their higher source-side injection velocity compared to MOSFETs. Classical MOSFETs in this low V_{DD} range do not even meet the I_{ON}-I_{OFF} stipulation of 10^4, due to the limitation of > 60mV/decade sub-threshold slope, making the narrow gap semiconductor based tunnel FET device architecture promising for ultra-low voltage logic applications down to quarter volt V_{CC}. For below quarter volt and upto 50 mV supply voltage operation we propose the use of split-gate quantum nanodots which are described in the following section.

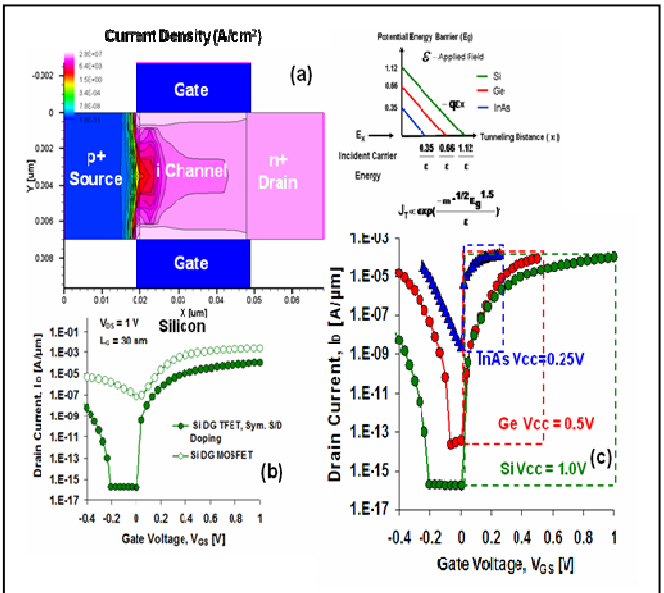

Figure 2. (a) Electron current density profile in tunnel FETs (TFETs) (b) Transfer characteristics of Si TFETs and MOSFETs (c) Transfer characteristics of Si, Ge and InAs TFETs - lower barrier and shorter tunneling distance for tunneling in InAs.

III. Reconfigurable BDD Logic Architectures

A. *Device Structure*

The basic structure of the split-gate quantum nanodots shown in Fig. 3a is built using an InP-based quantum-well heterostructure grown using solid-source Molecular Beam Epitaxy (MBE) technique. E-beam evaporation and lift-off technique is used to define a pair of wrap-around Schottky gates around the nanowire (Fig. 3b). This pair of Schottky gates called the split-gate induces depletion regions in the heterostructure through electrostatic action thus forming double tunnel barriers at the source and drain ends. The two induced depletion regions and the quantum well heterostructure isolate a quantum dot between the source and drain tunnel junctions. The height and width of the tunnel barriers as well as the dot size are controlled using the bias on the split-gate. The voltage bias on the split-gate also provides the reconfigurability feature to the quantum dot enabling it to operate in three different modes: active, open and short. Providing a very high and a very low split-gate bias allows the device to function as an open and as a short respectively (Fig. 4b and 4c).

The device is in active mode when the split-gate voltage is adjusted such that the well heterostructure acts as a quantum dot that is confined by two tunnel barriers (Fig 4a). A top control gate (Fig. 3c), which is separated from the quantum dot and the split-gates via a deposited high-K gate dielectric, can control the dot potential independently. The device now in the active mode acts as a Single Electron Transistor (SET) with the top control gate acting as the input control signal to allow or block electrons to tunnel through the island.

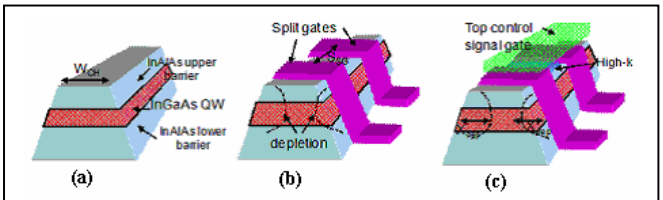

Figure 3. (a) III-V nanowire formation (b) wrap-around Schottky split gate formation (c) top control gate formation.

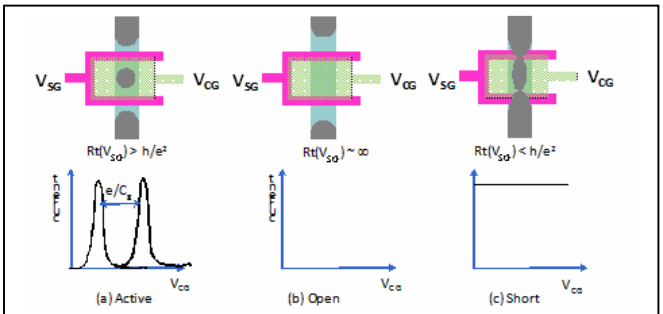

Figure 4. Various modes of operation of the Split-Gate nanodot device when it is being controlled by the wrap around Schottky Split-Gate.

B. *Logic Architecture*

In order to use the split-gate quantum nanodots to build logic devices a change in the implementation architecture of Boolean logic is required. This is in order to avoid contact and wire parasitic effects and the voltage gain associated with a

large fanout. In order to do this, we propose the use of BDD logic architectures using quantum gates which have been pioneered by the group at Hokkaido University [3] [4] [5] [6]. Further, nanoscale devices are also prone to faults and reconfigurability becomes a valuable feature that allows us to configure BDD logic devices to work around faults in the fabric. Our work proposes using the split-gate quantum nanodot device described previously to support a reconfigurable architecture based on the BDD fabric [10].

We now give a brief overview of BDD logic before discussing operational characteristics in the next section. Each row of the BDD fabric is controlled by a single variable. Depending on the input value of the control variable, messenger electrons are transferred to either the left or right exit branches (Fig 5a). The variables implementing the given function establish a path in this fabric from the root (output) node to either a one-terminal or a zero-terminal to realize desired functionality (Fig 5b). An input vector corresponds to a unique path from the root node of the BDD to an output terminal. A current detector at the root measures the current and depending on the operating mode (active high or active low) it is interpreted as a logic one or a zero.

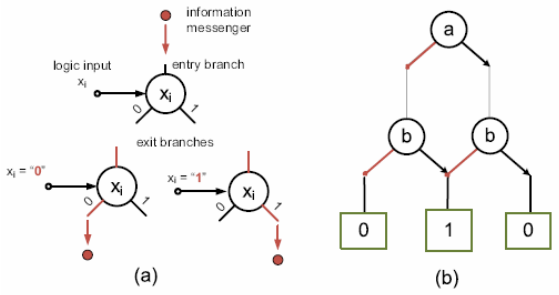

Figure 5. (a) A binary decision diagram (BDD) node device (b) Paths from the root node to an output terminal in a BDD.

C. *Operational Characteristics*

The split-gate controlled quantum nanodot in the active mode acts as a Single Electron Transistor (SET) with the top gate (Fig. 3c) controlling the Coulomb blockade and hence the tunneling of electrons across the barrier isolated quantum dot at is formed by the split-gate. The operation of SETs based on Coulomb blockade is a well understood phenomenon and a large amount of work is based on the orthodox theory of single charge phenomenon proposed by Devoret et al. [7]. We conducted a series of simulation experiments using SIMON, a Monte Carlo simulation tool for SETs [8] [9], in order to understand the operation of SET based BDD logic circuits. We assumed a quantum dot size of 10nm, a tunnel barrier width of 10 nm, a tunnel resistance of 100 KΩ and an operating temperature of 77K.

The current-voltage characteristics of a BDD circuit that is built using SETs can be understood by approximating its operation to that of a linear 1D array of SETs. For a given set of inputs to the BDD logic only one path in the BDD is active, effectively reducing the circuit to a 1D array of SETs through which current is driven by a certain amount of voltage bias applied across the array. When a 1D array of SETs is considered, the devices are turned On/Off based on the control gate voltages applied to individual SETs. The voltage bias applied across the array of SETs then defines the magnitude of current flow (Fig 6).

Fig. 6 also shows that for a given voltage bias, as the number of devices in the 1D array increases, the current flowing through the devices decreases. Thus, for a 1D array of SETs of certain length, in order to drive sufficient amount of current the voltage bias across the devices may need to be increased. However, this increase is limited as the Coulomb blockade, which is the operational principle behind these devices, breaks down as the voltage bias is increased (Fig 7). Thus, there is a limit to the length of the array of SETs and hence, on the depth of the BDD logic implementation. This occurs when there is a drop in the current levels due to an increase in the number of SETs and the current cannot be increased further by increasing the voltage bias because this would lead to a breakdown of the Coulomb blockade.

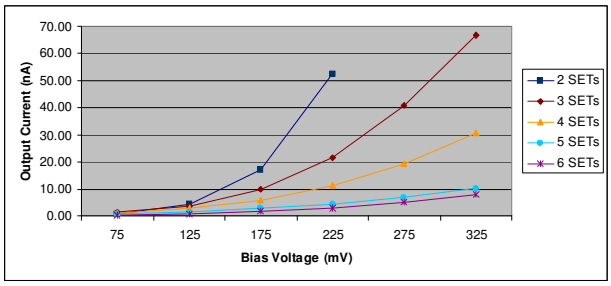

Figure 6. Increasing voltage bias across a 1D array of SETs increases the amount of observed current.

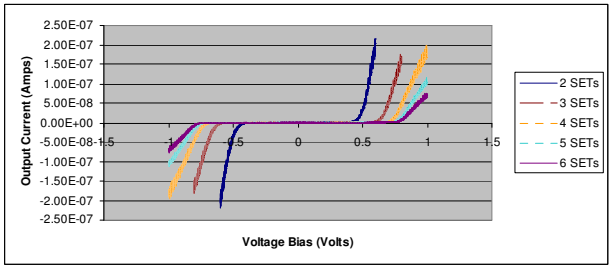

Figure 7. Increasing voltage bias across a 1D array of SETs leads to a breakdown of Coulomb Blockade (SETs are in Off State).

D. *Energy and Delay Characteristics*

The energy consumption in SETs is mainly caused by capacitive charge adjustments made by the bias and control gate voltage sources as electrons tunnel across various tunnel barriers in the circuit. Fig. 8 compares the switching energy of Tunnel FETs and Quantum nanodot SETs to that of Quantum Well Field Effect Transistors (QWFETs) and Silicon NMOS transistors. The figure suggests that at very low feature sizes Tunnel FETs and Quantum nanodot SETs may be able to beat CMOS devices as ultra low power devices.

Delay in SETs can be understood in terms of the tunneling rates of electrons across the tunnel barriers. When an electron tunnels across a barrier there is a change in the free energy of

the circuit associated with the particular tunneling event. The change in the free energy, ΔF, is computed as the change in the electrostatic energy of the system minus the work done by the voltage sources during the tunnel event. From the orthodox theory of SETs [7] the tunneling rate, Γ, is given by:

$$\Gamma(V) = (-\Delta F / e^2 R_T) \cdot (1 - \exp(\Delta F / K_B T))$$

where ΔF is the change in the free energy of the system, V is the voltage bias applied across the array of SETs, e is the charge of an electron, R_T is the Resistance of a Tunnel Barrier, K_B is the Boltzman constant and T is the operating temperature of the circuit.

The tunneling process across a tunnel barrier can be viewed as a Poisson process with the tunneling rate, Γ(V) as its parameter. Hence, when all the devices in a 1D array of SETs are turned 'On', the delay experienced before an output current is detected is a random variable whose mean value is the number of tunnel barriers multiplied by the expected tunneling delay (which is the inverse of the tunneling rate) for a single tunnel barrier. Typical tunneling rates for a tunnel barrier are of the order of 10^{12} when an SET is turned on. Fig. 9a shows the energy delay curves for 1D arrays of SETs of various lengths to give a picture of both the energy and the delay associated with SET based circuits. Fig. 9b compares the energy delay product of a single SET device (10 nm quantum dot at 77K) with the energy delay products of TFET, QWFET and high-K gate MOS devices (values used in the plot are representative of various technologies and do not represent a specific process technology).

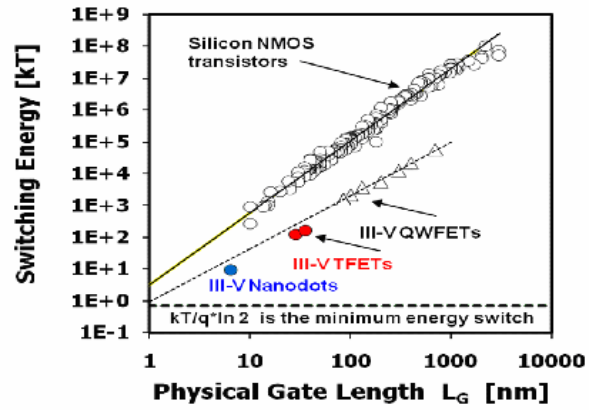

Figure 8. Comparison of switching energy vs device feature size for Silicon NMOS, QWFETs, TFETs and Quantum nanodots.

IV. Conclusion

This paper introduces two new device technologies which are promising candidates for realizing ultra-low power signal processing. The incorporation of these devices in novel signal processing architectures can enable the next generation of smart devices.

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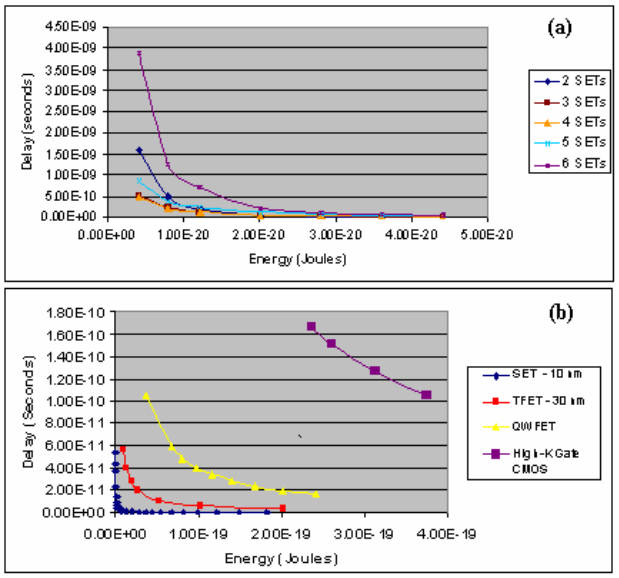

Figure 9. (a)Energy-Delay curves for 1D arrays of SETs (b) Energy-Delay curves for various technologies.

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