Integrated nanoelectronics for the future

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Integrated electronics has come a long way since the invention of the transistor in 1947 and the fabrication of the first integrated circuit in 1958. Given feature sizes as small as a few nanometres, what will the future hold for integrated electronics?

Gordon Moore's prediction made over 40 years ago, that the number of transistors in an integrated circuit would double roughly every 24 months, continues to be the guiding principle of the semiconductor and computing industries. As transistor count increases, each transistor becomes smaller, faster and cheaper, leading to an unprecedented increase in microprocessor performance[1].

Today, the so-called 65-nm technology node (related to half the metal pitch of a dynamic random access memory device) of the most advanced microprocessors in production[2] has transistor gate lengths of 35 nm and a SiO_2 gate oxide thickness of 1.2 nm. However, further miniaturization by traditional geometric scaling of conventional silicon devices faces many technical challenges. These include, amongst others, excessive leakage currents through the SiO_2 gate oxide, exponentially increasing leakage currents between transistor source and drain, increasing source–drain access resistance, carrier-mobility degradation in the transistor channel from increasing electric field, as well as increasing device-to-device variation[3].

The silicon community has been responding promptly and is overcoming many of these challenges with various research breakthroughs and innovations to improve present and future generations of the complementary metal–oxide–semiconductor (CMOS) transistor technology for gigascale digital systems. Examples of these innovations include mechanically strained silicon channels, where strain enhances electron and hole mobility, as well as gate stacks composed of dielectrics with high dielectric constant (high-*K* dielectrics) and metal electrodes for higher drive current and lower overall gate leakage. Furthermore, non-planar designs such as tri-gate transistors are being developed to mitigate problems arising, for example, from short-channel effects.

Combined, these innovations and strategies will enable continued logic CMOS transistor downscaling and improvements in performance trends until at least the middle of the next decade. Furthermore, intensive research is currently being carried out by both industry and academia on electronic materials other than silicon (for example, other semiconductor materials, semiconductor nanowires and carbon nanotubes) and their integration onto silicon wafers for future high-performance and energy-efficient very-large-scale integrated (VLSI) nanoelectronics applications beyond 2015.

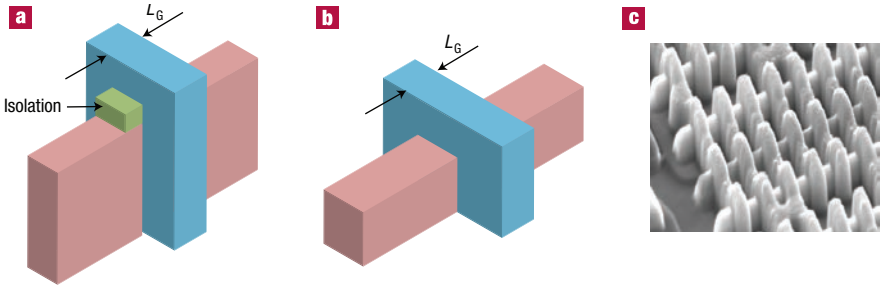

Figure 1 Non-planar transistors. **a**, Double-gate transistor. **b**, Schematic and **c**, scanning electron microscope (SEM) image of a tri-gate transistor. L_G is the physical gate length of the transistor. In the double-gate transistor, its top gate electrode (blue) is isolated from the silicon channel (brown). Hence the transistor has two gate electrodes, one on each side of the silicon channel. The tri-gate transistor has three gate electrodes surrounding the silicon channel.

TODAY'S CMOS TECHNOLOGY

Until earlier this decade, the scaling and performance trends of the logic transistor were mainly the result of SiO_2 gate oxide scaling as well as source–drain junction and well engineering. The physical gate-oxide thickness was scaled from about 20 nm 15 years ago to only 1.2 nm in the current 65-nm technology node. Along the way various innovative gate-oxide annealing

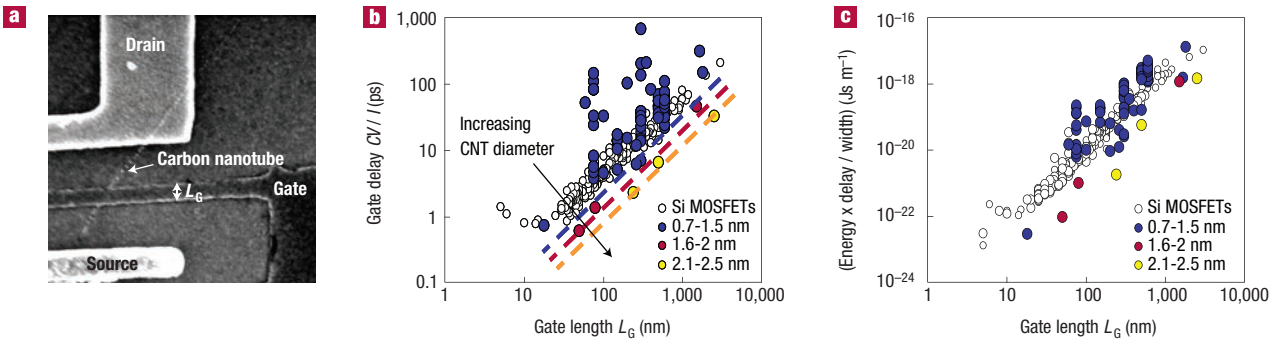

Figure 2 Carbon nanotube transistor characteristics compared with standard silicon p-channel MOSFETS. **a**, SEM image. **b**, Intrinsic gate delay of the transistor. **c**, Normalized energy-delay product, which represents the energy efficiency of the device. In general the electrical characteristics of the nanotube transistors are related to its tube diameter, which in turn is related to the bandgap of the nanotube. The larger the CNT diameter, the smaller the bandgap of the CNT, the higher the carrier mobility in the CNT[16].

and surface-cleaning technologies were introduced to improve reliability and reduce defect density. In particular, the SiO_2 oxide was treated by nitridation to enhance its scalability and improve transistor reliability.

In the 90-nm node, strained silicon technology was introduced to boost performance and improve the energy efficiency of the CMOS transistors. In the case of the p-channel transistor, silicon germanium is now used instead of silicon to form the source and drain regions and to induce uniaxial compressive strain in the silicon channel, thereby enhancing hole mobility as well as reducing parasitic source and drain resistances. In the case of the n-channel transistor, a tensile silicon nitride cap is deposited on top of the transistor to induce uniaxial tensile strain in the silicon channel and improve electron mobility.

A second generation of strained silicon technology has already been adopted in the 65-nm technology node and is currently in high-volume manufacturing. As the thickness of the SiO_2 gate oxide has reached 1.2 nm, which is less than five atomic layers thick, there is no room left for further scaling, and any more reduction in oxide thickness will make the gate leakage unmanageable. To solve this problem, an alternative high-*K* gate dielectric is needed. In addition, metal-gate electrodes with the correct work functions are required to achieve the correct n- and p-channel MOS transistor threshold voltages and high performance[4–6]. Intel has successfully implemented high-*K*/metal-gate stacks in its 45-nm technology node, leading to a significant improvement in transistor performance and reduction in gate leakage. A second-generation of high-*K*/metal-gate stacks is in development for the next technology node.

CMOS TECHNOLOGY FOR THE NEXT 15 YEARS

Although strained silicon and high-*K*/metal-gate technologies will continue to play significant roles in advancing present technology, the continuation of Moore's law over the next 15 years will require the transistor structure itself to evolve. For example, a transition for the present planar structure to non-planar, three-dimensional structures such as the double-gate transistor[7] and the tri-gate transistor[8], as shown in Fig. 1, will improve short-channel performance and enhance scalability. Furthermore, the integration of novel electronic materials with silicon is required to further improve speed and energy-efficiency of the transistors. Both the double-gate and tri-gate transistors are fully depleted so that the entire available silicon underneath the gate electrode is depleted of carriers before the threshold condition is reached. Such double-gate and tri-gate transistors have shown significantly improved electrostatics and hence better scalability than planar transistors. Furthermore, compared with the double-gate transistor structure the tri-gate transistor structure provides more raw drive current per device footprint, further improves short-channel performance and is more manufacturable.

Recently the combined benefits of the tri-gate CMOS transistor architecture with strained-silicon channels, high-*K* gate dielectric, metal-gate electrode, and dual epitaxially grown raised source–drains have been demonstrated, and the resulting CMOS transistors show excellent short-channel characteristics with high drive-current performance[9]. These results demonstrate that the benefits of all these different silicon innovations can be combined to extend and continue the CMOS scaling and performance trends.

Meanwhile, much interest has been generated and good progress has been made in the research of non-silicon electronic materials for future logic applications, and their integration onto the silicon platform. Among the most studied materials are Ge, III–V compound semiconductors such as InSb (ref. 10) and InGaAs (ref. 11), semiconductor nanowires[12] and carbon nanotubes (CNTs)[13]. These materials, in general, have significantly higher intrinsic (p or n) mobility than silicon, and they have the potential for enabling future high-speed applications at very low power-supply voltages[14]. For example, the p-channel single-walled CNT field-effect transistors (FETs) have some interesting and useful device characteristics, as shown in Fig. 2. However, like other 'bottom-up' chemically synthesized materials, CNTs are currently suffering from the fundamental placement problem as there is no practical way to precisely align and position them. This problem needs to be solved before CNTs find many practical applications in VLSI nanoelectronics.

On the other hand, III–V materials have been used in communication and optoelectronic products for a long time. They have, in general, much higher electron mobility and conductivity than silicon, which make them potentially useful for future high-speed and low-power applications, as shown in Fig. 3. Recently very-high-speed 85-nm InSb quantum-well transistors have been demonstrated at a low supply voltage of only 0.5 V. Compared with state-of-the-art silicon transistors, these III–V transistors show either a 1.5-fold improvement in intrinsic speed performance at the same power, or 10-fold reduction in power for the same speed performance[10]. As these III–V materials have low bandgaps, quantum-well device structures — where carriers are confined in

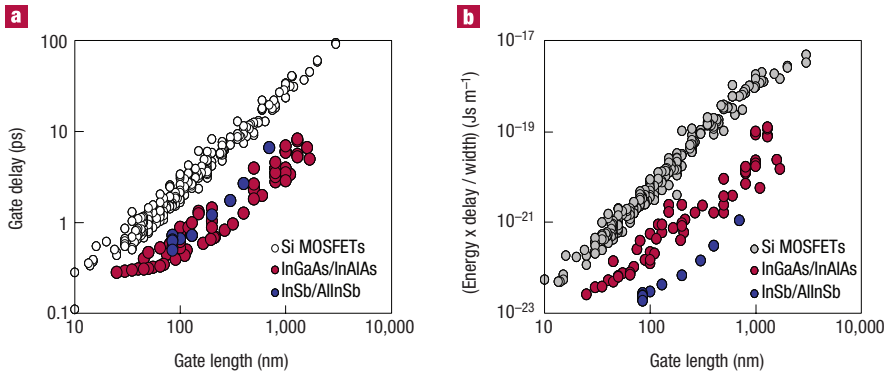

Figure 3 III–V quantum-well transistor characteristics compared with standard silicon MOSFETS[15]. **a**, Intrinsic gate delay. **b**, Normalized energy-delay product of n-channel InSb and InGaAs quantum-well transistors.

a low-bandgap material by adjacent barrier layers with a larger bandgap — are required to control the transistor parasitic junction leakage and off-state leakage.

Although III–V quantum-well FETs have some very attractive and tangible merits, many technical challenges need to be overcome before they will become practical for future high-speed and low-power applications[15]. For instance, because of the lack of a stable gate dielectric, currently all of these devices use a direct Schottky metal gate, which results in a large parasitic gate leakage. A gate dielectric stack that is compatible with III–V materials will be needed to solve this problem. However, the recent successful implementation of high-*K*/metal-gate in the 45-nm silicon technology node will have positive impact on the progress of high-*K* research for III–V. Another challenge is the low hole mobility in III–V materials and the lack of a p-channel device strategy for the CMOS configuration, which is required for low-power applications. Yet another challenge is the scalability of III–V devices. Like the silicon transistor, the III–V transistor may also need a non-planar, three-dimensional structure to improve its electrostatics with scaling.

MEMORY DEVICES

The benefits of dimensional scaling include increased transistor density, lower cost per transistor, and lower switching energy per transistor. Increase in transistor density in particular results in enhanced on-chip logic functionality as well as increased on-chip cache memory density. In the twenty-first century, the microprocessor is moving into the 'multi-core' era where multiple CPU engines or 'cores' are integrated into a single monolithic die. The processing power of such a tiny die will soon match a large computer system that at present is made up of many microprocessors.

This level of integration in processing power demands ever-increasing memory capacity and bandwidth to keep up with the CPU performance needs. Large and fast on-die memory has become increasingly important in today's microprocessors. The six-transistor (6T) static random access memory (SRAM)-based cache memory continues to be the workhorse serving the high-performance requirement of the CPUs. The 6T SRAM not only has the highest access speed, it also provides excellent synergy in terms of process integration with the high-performance logic transistor technology. Technology scaling has made it feasible to integrate over 10 MB of high-speed SRAM memory on a single die at today's 65-nm logic technology node. Transistor-level innovations such as the high-*K*/metal-gate stacks and the fully depleted tri-gate CMOS transistors will mitigate many of the key scaling challenges facing the 6T SRAM, including leakage power management and cell instability.

Dynamic RAM (DRAM) has also played a significant role in computing systems as the main off-chip memory. The relentless technology scaling has driven up DRAM density into the gigabit regime, which enables the use of DRAM as the large main memory to meet system bandwidth needs while lowering overall system cost. Innovations in both transistor architecture and new materials, for example non-planar low-leakage transistors and high-*K*-based storage capacitors, certainly will continue to drive the scaling of DRAM well beyond today's 65-nm dimension. Another form of silicon-based semiconductor memory is the non-volatile memory (NVM) where data can be maintained even after the power supply is removed. The primary NVMs today are built on a simple MOSFET transistor with a 'floating-gate' where charges can be stored to modulate the threshold voltage of the transistor. Continued transistor miniaturization has also enabled a dramatic density increase in NVMs. It is possible to have over a gigabit of storage elements integrated into one single die. The rapid density growth along with cost reduction in NVMs have enabled the explosive growth in consumer electronics such as cell phones and digital cameras. Once again, silicon technology innovations will help drive the growth and use of NVMs in more applications over the next decade. Furthermore, novel electronic materials, novel nanostructures, emerging nanotechnologies, biological systems and so on are being researched and explored for future memory applications.

LOOKING INTO THE FUTURE

The relentless forward march of science and technology in shrinking transistors and integrating more novel electronic materials on silicon to produce ever-higher-performance and more energy-efficient computational and memory devices will definitely continue for many years to come. The natural scaling process has already led us to the realm of nanotechnology and nanoelectronics where both difficult technical challenges and golden opportunities co-exist. To overcome the challenges, research on new nanodevice structures, different device usage models, novel electronic materials and their integration on silicon, bottom-up chemical synthesis and assembly techniques are required. Addressing such fundamental issues, research on nanotechnology and nanoelectronics for high-performance and energy-efficient VLSI applications is more exciting and rewarding than ever.

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