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III-V field-effect transistors for low power digital logic applications

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Abstract

Sustaining Moore's Law of doubling CMOS transistor density every twenty four months will require not only shrinking the transistor dimensions, but also introduction of new materials and new device architectures to achieve the highest performance per watt of power dissipation. Compound semiconductor-based quantum-well field effect transistors have recently emerged as a promising transistor option for future ultra low-power logic applications. This paper reviews the opportunities and challenges in this exciting field of research.

Keywords: Nanotechnology; III-V; high-κ dielectric; quantum-well; field effect transistors

1. Introduction

According to Moore's Law, the number of transistors per integrated circuit doubles every 24 months, and it has been the guiding principle for the silicon semiconductor industry for over 30 years. The sustaining of the Moore's Law, however, requires continued transistor scaling and performance improvement. The physical gate length L_G of the Si transistors used in the 65 nm logic generation node is ~ 35 nm. It is projected that transistor L_G may reach ~10 nm in 2011. Increasingly, there is an urgent need for these nanoscale transistors to be "energy efficient" which they should operate with the lowest switching power and the lowest off-state leakage power. There are multiple parallel approaches and combination of them from both materials innovation and transistor architecture standpoint that are being pursued today in the silicon nanoelectronics area that will continue to deliver transistors with ever shrinking physical dimensions and increased performance at same or reduced power consumption. These innovations include highly strained-Si channels [1, 2] for mobility enhancement, high-κ/metal-gate stacks [3, 4] for higher drive current and lower gate leakage, and the non-planar multiple gate CMOS transistor architecture such as Tri-gate transistors [5, 6]. Recently, a lot of interest has been generated in incorporating III-V nanoelectronics onto

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the silicon platform to benefit from the ultra-high electron mobility offered by the compound semiconductors.

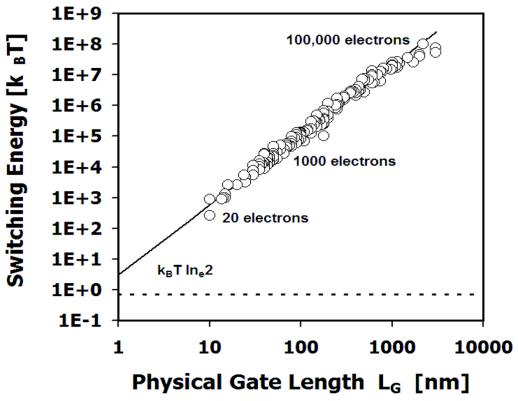

Fig. 1. Transistor switching energy plotted as a function of physical gate length. Also shown is the thermodynamic minimum energy for a hypothetical irreversible single particle binary logic gate [9, 10].

For example, good progress has been made in the development of III-V narrow band-gap compound semiconductor quantum-well field-effect transistors (QWFETs) [7, 8], which show promise for future high performance and low power logic applications. These III-V nanoelectronic devices hold promise as candidates for integration with the ubiquitous silicon platform in order to enhance circuit functionality while simultaneously enabling the extension of Moore's Law well into the middle of next decade.

2. Low energy switch

Fig. 1 shows the monotonic and exponential reduction in the switching energy of individual silicon NMOS transistors as we continue to scale physical gate length, gate width and supply voltage with every technology generation. It is also noted that, with device scaling there is a reduction in the total number of electrons that participate in the switching event. Interestingly, the trend-line approaches the Shannon-von Neumann-Landauer fundamental limit for the thermodynamical minimum of energy per binary switching event as given by the formula $k_B T \log_e 2$ [9]. However, with the reduction in the number of electrons with physical scaling, the device to device fluctuation continues to increase which degrade the robustness of complex ULSI circuits created using these nanoscale transistors.

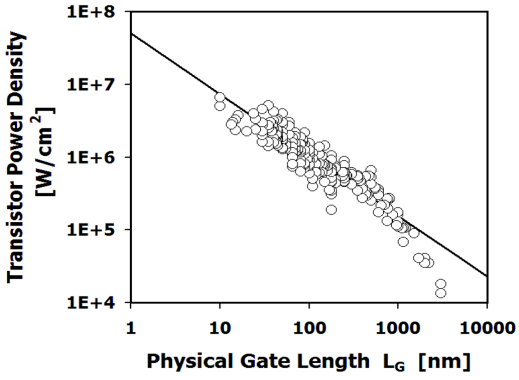

Fig. 2. Individual transistor switching power density plotted as a function of physical gate length. With physical dimensional scaling the device level power density continues to increase exponentially.

Additionally, the operating supply voltages of the transistors are not scaled proportionally as the device area scales due to performance degradation concerns, which, in turn, results in monotonic increase in device power density per unit area. This results in an increase in chip temperature depending on the overall on-chip transistor packing density and the transistor switching activity factor. Thus, there is a strong need to explore novel transistor options that could enable dramatic supply voltage reduction without sacrificing performance and density. We have recently demonstrated sub-micron gate length indium antimonide (InSb) based quantum well field effect transistors (QWFETs) operating at very low drain voltages [8]. Enhancement mode n-channel InSb quantum well transistors were demonstrated with unity gain cutoff frequency, f_T, exceeding 300 GHz at an operating voltage of only 0.5V V_{DS}. These InSb quantum well transistors demonstrate 50% higher intrinsic speed, f_T, than silicon NMOS transistors while consuming an order of magnitude less dynamic power [8].

3. III-V Field Effect Transistors

Indium antimonide (InSb) holds promise for ultra-fast, very low power digital logic applications as it has the highest electron mobility and saturation velocity of any known semiconductor.

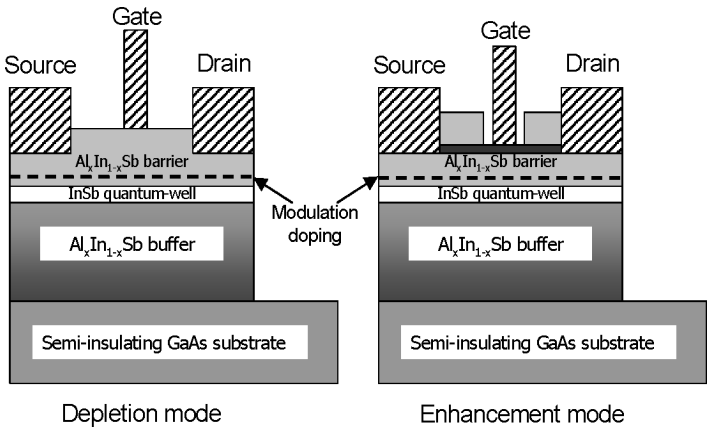

Fig. 3. Schematic of the depletion mode and enhancement mode indium antimonide (InSb) quantum well transistors.

This performance potential was demonstrated first in a 200nm gate length (L_G) depletion mode InSb quantum well transistor (QWFET) with 150GHz f_T at 0.5V V_{DS} and subsequently a 100nm L_G depletion mode device with 210GHz f_T [7]. In both cases, the transistors were fabricated on a semi-insulating GaAs substrate using a relaxed metamorphic buffer layer of $Al_yIn_{1-y}Sb$ to accommodate lattice mismatch, a compressively strained InSb quantum well confined between layers of $Al_xIn_{1-x}Sb$ and a Schottky barrier metal gate. The quantum well transistor architecture employs barrier layers with higher bandgap materials to mitigate the effect of the narrow bandgap InSb on device leakage and breakdown. For direct coupled FET logic (DCFL) applications, both enhancement (i.e. positive V_T) and depletion mode devices are required. At the IEDM 2005, we reported, for the first time, on the fabrication and characterization of 85nm gate length enhancement (e-mode) and depletion mode (d-mode) InSb QWFETs [8]. An enhancement mode InSb QWFET was demonstrated using a novel deep recess etch in the gate region, which shows a peak f_T of 305GHz at 0.5V V_{DS}. A depletion mode device was demonstrated at the same time utilizing a shallow recess gate with a peak f_T of 256GHz at 0.5V V_{DS}. Fig. 3 shows the cross-section schematic of the depletion mode and enhancement mode InSb QWFETs. The demonstration of both high performance depletion and enhancement mode InSb QWFETs makes the technology a promising candidate for future high-speed, low-power logic applications.

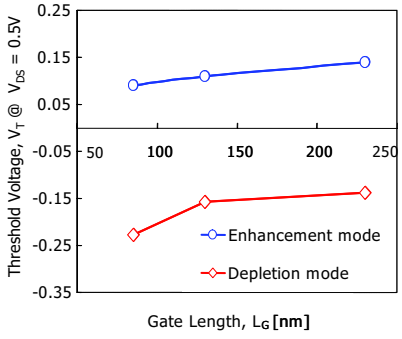

Fig. 4. Transfer characteristics of 85nm gate length enhancement mode InSb QWFET at V_{DS} = 0.5V and 0.05V.

Due to the small gate to channel separation, the deep recess gate 85nm L_G e-mode devices exhibit excellent sub-threshold slope of 105 mV/decade and DIBL of 95mV/V, with maximum I_{ON}-I_{OFF} ratio of 330 limited by the gate leakage current through the vertical metal-semiconductor Schottky junction, as illustrated in Fig. 4.

To further improve the I_{ON}-I_{OFF} ratio, a promising high-k dielectric/metal gate stack on the AlInSb/InSb device layers is identified which exhibits moderate hysteresis, low frequency dispersion and four orders of magnitude reduction in gate leakage. Fig. 5 shows the room temperature C-V frequency dispersion

characteristics of high-k/metal gate stack on AlInSb/InSb. The high-k dielectric, in this case, is Al_2O_3 (alumina) deposited using a low temperature atomic layer deposition (ALD) process. The frequency dispersion in the inversion region is a combination of a) minority carrier generation in low bandgap AlInSb/InSb material system and b) the generation/recombination from the surface traps. The room temperature C-V characteristics still exhibit a moderate level of hysteresis, as shown in the inset of Fig. 5, which is believed to be from elemental antimony acting as hole traps [11]. The high-k/metal gate stack results in four orders of magnitude reduction in the gate leakage current compared to the Schottky metal gate stack (Fig. 5). Fig. 6 shows the I_D-V_G characteristics of the InSb QWFETs with

(a)

(b)

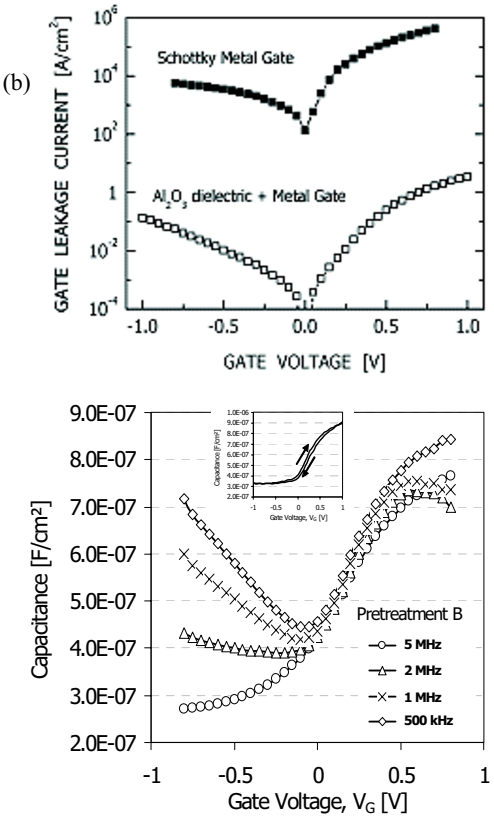

Fig. 5. Room temperature (a) gate to channel leakage characteristics for ALD Al_2O_3 high-k dielectric and Al metal gate stack on AlInSb/InSb device layers showing four orders of magnitude reduction in leakage compared to Schottky metal gate (b) gate to channel capacitance characteristics showing frequency dispersion.

Schottky metal gate and with insulated gate using ALD Al_2O_3 gate dielectric. The insulated gate FET shows reduction in gate leakage as expected, but the introduction of the dielectric induced a large shift in the threshold voltage of the transistor due to high interface state density.

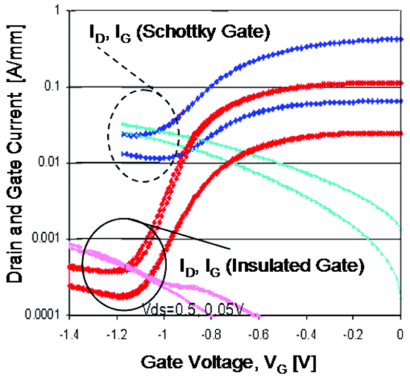

Fig. 6. Transfer characteristics of InSb QWFETs with Schottky metal gate and insulated metal gate with ALD Al_2O_3 dielectric.

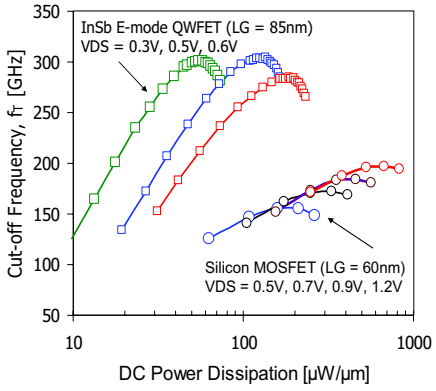

Fig. 7. Measured f_T vs DC power dissipation (normalized to the transistor width) for 85nm L_G InSb QWFETs and 60nm L_G silicon nMOS transistors.

To further improve the I_{ON}-I_{OFF} ratio, a promising high-k dielectric/metal gate stack on the AlInSb/InSb device layers is identified which exhibits moderate hysteresis, low frequency dispersion and four orders of magnitude reduction in gate leakage. Fig. 5 shows the room temperature C-V frequency dispersion characteristics of high-k/metal gate stack on AlInSb/InSb. The high-k dielectric, in this case, is Al_2O_3 (alumina) deposited using a low temperature

atomic layer deposition (ALD) process. The frequency dispersion in the inversion region is a combination of a) minority carrier generation in low bandgap AlInSb/InSb material system and b) the generation/recombination from the surface traps. The room temperature C-V characteristics still exhibit a moderate level of hysteresis, as shown in the inset of Fig. 5, which is believed to be from elemental antimony acting as hole traps [11]. The high-k/metal gate stack results in four orders of magnitude reduction in the gate leakage current compared to the Schottky metal gate stack (Fig. 5). Fig. 6 shows the I_D-V_G characteristics of the InSb QWFETs with Schottky metal gate and with insulated gate using ALD Al_2O_3 gate dielectric. The insulated gate FET shows reduction in gate leakage as expected, but the introduction of the dielectric induced a large shift in the threshold voltage of the transistor due to high interface state density.

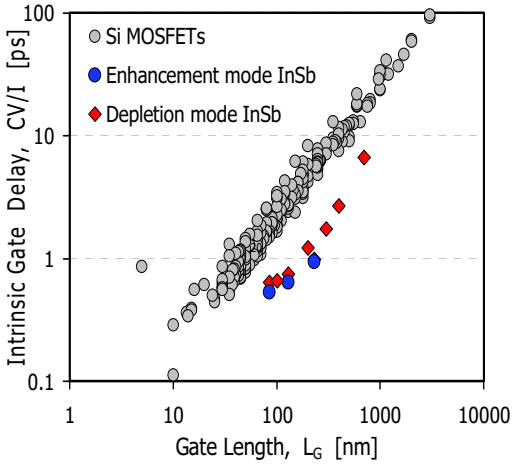

Fig. 8. Transistor gate delay (CV/I) versus gate length for InSb QWFETs at V_{DS} = 0.5 V benchmarked against state-of-the-art silicon nMOS transistors.

4. Conclusions

At this early stage of development, InSb QWFETs already show 50% higher intrinsic switching frequency and a simultaneous 10× reduction in dynamic power dissipation compared to the advanced Si MOSFETs (Fig. 7). Fig. 8 plots the intrinsic gate delay (CV/I) versus gate length of InSb QWFETs benchmarked against the historical and future Si nMOS transistor scaling trend. It is shown that, for a given physical gate length, the InSb devices offer 2.8× reduction in gate delay and 50× reduction in switching energy compared to the silicon transistors, [10] making them an attractive device option for future high-speed, ultra low-power logic applications.

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References

[1] S. Thompson, M. Armstrong, C. Auth, S. Cea, R. Chau, G. Glass, T. Hoffman, J. Klaus, Z. Ma, B. McIntyre, A. Murthy, B. Obradovic, L. Shifren, S. Sivakumar, S. Tyagi, T. Ghani, K. Mistry, M. Bohr, Y. El-Mansy, IEEE Electr. Dev. Lett. 25 (2004) 191.

[2] S. Datta, G. Dewey, M. Doczy, B. S. Doyle, B. Jin, J. Kavalieros, R. Kotlyar, M. Metz, N. Zelick, and R. Chau, IEDM Tech. Dig. 2003, 653–656.

[3] R. Chau, S. Datta, M. Doczy, J. Kavalieros, M. Metz, Extended Abstracts of International Workshop on Gate Insulator 2003, 124-126.

[4] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, M. Metz, IEEE Electr. Dev. Lett. 25 (2004) 408–409.

[5] R. Chau, B. Doyle, J. Kavalieros, D. Barlage, A. Murthy, M. Doczy, R. Arghavani, S. Datta, Extended Abstracts of International Conference on Solid State Devices and Materials, Nagoya, Japan (2002) 68-69.

[6] B. Doyle, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalieros, T. Linton, A. Murthy, R. Rios, R. Chau, IEEE Electron Dev. Lett. 24 (2003) 263-265.

[7] T. Ashley, A. Barnes, L. Buckle, S. Datta, A. Dean, M. Emeny, M. Fearn, D. Hayes, K. Hilton, R. Jefferies, T. Martin, K. Nash, T. Philips, W. Tang, P. Wilding, R. Chau, Proc. 7th Intern. Conf. on Solid-State and Integrated Circuits Technology (2004) 2253-2256.

[8] S. Datta, T. Ashley, J. Brask, L. Buckle, M. Doczy, M. Emeny, D. Hayes, K. Hilton, R. Jefferies, T. Martin, T. Philips, D. Wallis, P. Wilding, R. Chau, IEDM Tech. Dig. 2005, 34.1-34.4.

[9] R. W. Landauer, IBM J. Research and Development 5 (1961) 183-191.

[10] R. Chau, S. Datta, M. Doczy, B. Doyle, B. Jin, J. Kavalieros, A. Majumdar, M. Metz, M. Radosavljevic, IEEE Trans. on Nanotech. 4 (2005) 153-158.

[11] Z. Calahorra, J. Bregman, Y. Shapira, J. Vac. Sci. Techn. B 4 (1986) 1195-1202.