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Sub-*kT/q* Switching in Strong Inversion in $PbZr_{0.52}Ti_{0.48}O_3$ Gated Negative Capacitance FETs

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ABSTRACT Hysteretic switching with a sub-*kT/q* steep slope (13 mV/decade at room temperature) is experimentally demonstrated in MOSFETs with $PbZr_{0.52}$ $Ti_{0.48}O_3$ as a ferroelectric (FE) gate insulator, integrated on a silicon channel with a nonperovskite high-*k* dielectric (HfO_2) as a buffer interlayer. The steep switching is independent of drain bias. For the first time, sub-*kT/q* switching due to FE negative capacitance is observed not at low currents, but in strong inversion ($I_d \sim 100\ \mu A/\mu m$). Steep switching in strong inversion provides an important point of consistency with the predictions of the Landau–Devonshire theory and the Landau–Khalatnikov equation.

INDEX TERMS Ferroelectric (FE) field-effect transistor (FET), lead zirconate titanate, negative capacitance (NC), sub-*kT/q* switching.

I. INTRODUCTION

CMOS operating voltage and transistor power dissipation is fundamentally limited by Boltzmann statistics, according to which the application of a minimum voltage of 60 mV is necessary to change current by one order of magnitude. To circumvent this limit and enable low-voltage operation, it has been proposed that the conventional gate dielectric be replaced by an insulator that provides an effective negative capacitance (NC) [1]. NC causes the differential potential drop in the semiconductor and the insulator to have opposite polarity, enabling MOS current to increase at a rate higher than 60 mV per decade. Ferroelectric (FE) insulators had been predicted to have NC in accordance with the Landau mean-field-based theory. More recently, negative capacitance due to addition of a FE material to the insulator stack was demonstrated experimentally [2]–[4]. There have been few demonstrations of improved subthreshold swing due to a FE gate-stack at low currents [5]–[8]. However, a convincing correlation between the stand-alone FE switching properties and the resulting FE-gated NC transistor characteristics is absent in the existing literature. A clear understanding of the FE switching mechanism and the consequent enhancement of the transistor source to drain current is key to the progress of NC FerroFET toward becoming a viable technology. The Landau–Devonshire theory is a well-accepted phenomenological description of the physics of single-crystal FEs [9]–[15]. In the context of a manufacturable semiconductor technology, however, any FE material needs to be integrated directly within the gate-stack where the realization of single crystal FE may be difficult to achieve. For example, perovskite $SrTiO_3$ is an excellent substrate for the growth of popular FE such as $BaTiO_3$ with near perfect crystallinity [3]—but cannot be used as a part of the NC FET gate-stack because of negligible conduction band offset of $SrTiO_3$ with underlying semiconducting channels constructed using conventional semiconductors such as silicon, germanium, or gallium arsenide [16]. Thus, the experimental validation of a switching mechanism in nonideal polycrystalline FEs (resulting from deposition on the CMOS-compatible nonperovskite-based FE dielectric) directly integrated with a silicon FET represents a major step in the progress of the FE NC FET toward becoming a reality. In this paper, we report hysteretic switching with steep slope in long-channel FE field-effect transistors (FerroFETs)

with $PbZr_{0.52}Ti_{0.48}O_3$ (PZT) and hafnium dioxide (HfO_2) as the composite gate insulator. For the first time, sub-*kT/q* switching is observed in the strong inversion regime—providing a key point of agreement with the prediction of the Landau–Devonshire theory [9] for FEs and the Landau–Khalatnikov equation [17], [18]. The experimentally observed hysteresis window also closely matches with our FerroFET I_d–V_g calculations using the Landau theory. The two results represent a critical step in demonstrating NC FerroFETs whose characteristics quantitatively match the predictions of the Landau–Devonshire theory.

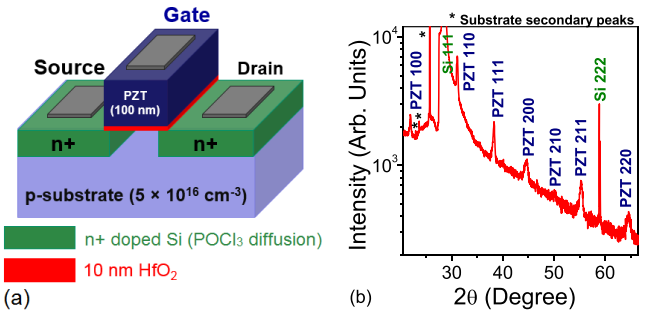

FIGURE 1. (a) Schematic of a FerroFET and (b) XRD data from PZT postprocessing. Pseudocubic perovskite PZT peaks are visible demonstrating the polycrystalline FE nature of PZT thin film on Si.

II. DEVICE FABRICATION

FerroFETs [Fig. 1(a)] were fabricated on (100) Si with a p-type doping of 5×10^{16} cm^{-3} [Fig. 1(a)]. Phosphoryl chloride ($POCl_3$) diffusion at 1000 °C with drive-in at 1050 °C was used for the n-type source/drain doping. To prevent reaction between the PZT and the Si channel, a 10-nm-thick HfO_2 was deposited underneath the PZT film as a part of the composite gate-stack using atomic layer deposition (ALD) at 250 °C. A 10:1 buffered oxide etch dip was used for native oxide removal prior to the ALD of HfO_2. Hundred nanometers of amorphous PZT was sputter deposited on HfO_2 (6 mtorr Ar pressure from a 5% excess Pb target). A 90-s rapid thermal annealing (RTA) in air at 620 °C was performed to crystallize the PZT. The polycrystalline nature of the PZT was confirmed through X-ray diffraction (XRD) data [Fig. 1(b)], which showed prominent perovskite PZT peaks corresponding to several different crystal orientations.

We shall show in the subsequent sections that from a design and capacitance matching perspective, it is advisable to have both PZT and HfO_2 films significantly thinner than in the fabricated devices. Thickness scaling of the HfO_2 will ultimately be limited by the tendency of Pb to diffuse through the HfO_2 and react with the underlying Si during the high-temperature (620 °C) RTA step. Similarly, PZT thinner than 100 nm typically shows higher coercive field and lower polarization, resulting in lower NC and poorer capacitance matching. Solving these material and fabrication issues is thus central to the realization of the full potential of the NC FerroFET.

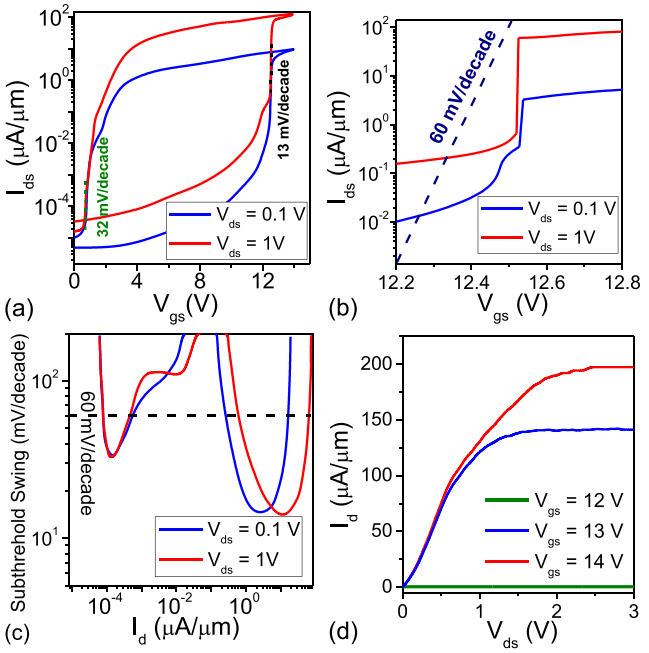

FIGURE 2. (a) Experimental I_d–V_g characteristics of a PZT gated FET with channel length $L_{ch} = 10$ μm for $V_{ds} = 0.1$ V and $V_{ds} = 1$ V. (b) Device shows *sub-kT/q* steep turn on with a slope of ∼13 mV/decade around $V_{gs} = 12.6$ V and steep turn off with a slope of ∼32 mV/decade. (c) Steep switching during turn on is observed in strong inversion. (d) I_d–V_{ds} characteristics show saturation.

III. FERROFET CHARACTERISTICS AND CONSISTENCY WITH THE LANDAU–DEVONSHIRE THEORY

Fig. 2(a) shows the measured I_d–V_g characteristics of the FerroFET with $L_{ch} = 10$ μm. The device shows sub-*kT/q* steep turn on with a slope of ∼13 mV/decade around $V_{gs} = 12.6$ V [Fig. 2(b)]. The steep switching is observed not at low I_d but in strong inversion [Fig. 2(c)]. Turn off is achieved with a hysteresis of ∼10 V. The steepest turn-off slope achieved is ∼32 mV/decade. The switching slope is independent of V_{ds} and is observed at both $V_{ds} = 0.1$ and 1 V. Saturation in the output characteristics is observed in the I_d–V_{ds} characteristics [Fig. 2(d)], which is important for a transistor's ability to drive an electrical load.

To understand the switching mechanism, the characteristics of the stand-alone FE capacitor and the baseline Si MOSFET (fabricated in a similar fashion as the FerroFET but without the FE PZT) are experimentally and independently studied. The stand-alone PZT is characterized using a PZT(100 nm)/HfO_2(10 nm)/silicon (p-doped 10^{20} cm^{-3}) stack. Since the 10 nm HfO_2 layer is a part of both the stand-alone FE capacitor and the baseline MOSFET, its effect has to be eliminated from the Q–V relationship of one of the two devices. For this purpose, it is important to understand the effect of high temperature processing of Pb containing

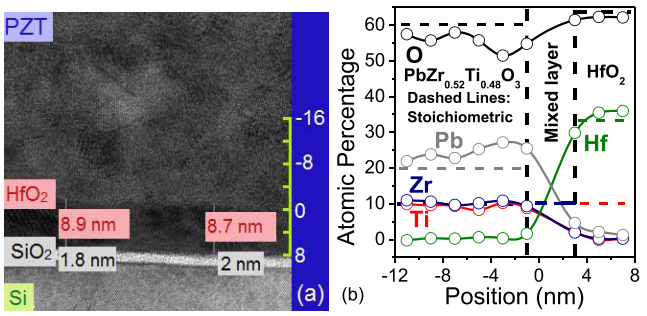

FIGURE 3. (a) Transmission Electron Micrograph (TEM) image and (b) EDX line profiles of different elements near the PZT/HfO^2 interface. Dotted lines represent the stoichiometric percentage. There is a clear pile up of Pb (gray) near the interface. There is a ~4 nm interfacial mixed layer with high percentage of both hafnium (Hf) and lead (Pb).

perovskite on HfO_2. Fig. 3 shows the composition of the interfacial layer between PZT and HfO_2 obtained through energy dispersive X-ray spectroscopy Energy-dispersive X-ray spectroscpy (EDX). An approximately 4-nm-thick interfacial mixed layer with high percentage of both Hf and Pb is observed. This layer results from Pb diffusing into HfO_2. Since the Pb-diffused HfO_2 and the mixed interfacial layer are present in both the stand-alone FE capacitor and the FerroFET, we eliminate the effect of the HfO_2 layer from the Q–V relationship of the baseline FET.

Fig. 4(a) and (b) shows the I_d–V_g and C_g–V_g characteristics, respectively, for the baseline FET. Extraction of

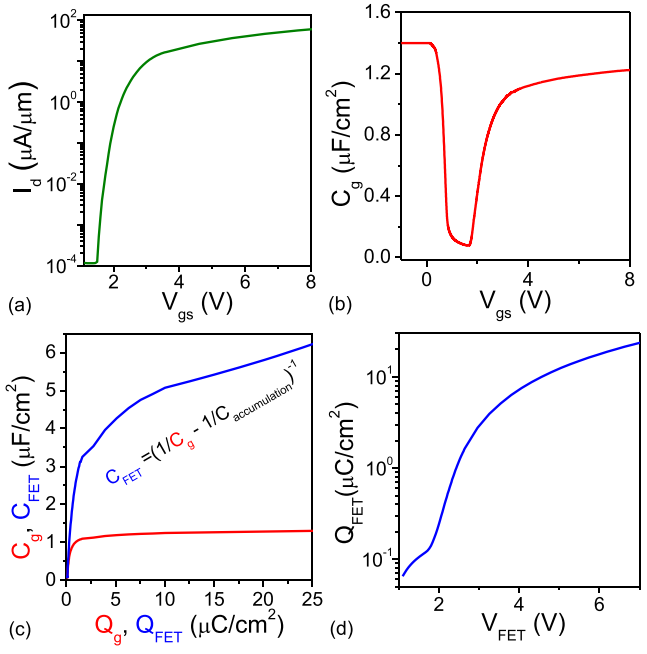

FIGURE 4. (a) Transfer and (b) *C*–*V* characteristics for the baseline FET. (c) Capacitance–charge (*C*–*Q*) characteristics with oxide (accumulation) capacitance removed. (d) *Q*–*V* relationship of the baseline device with oxide (accumulation) capacitance removed.

the charge–voltage (Q–V) relationship of the baseline FET is done by integrating the C_g–V_g characteristics. The C–V characteristics are measured by applying the voltage on FET gate, with source and drain grounded. To extract the charge versus voltage (Q–C) relationship with the contribution of the baseline FET gate oxide removed, the following procedure is adopted. First, the baseline FET Q–C (charge–capacitance) relationship is obtained by the integration of the C–V characteristics. From the total capacitance, the contribution of accumulation capacitance is subtracted, as shown in Fig. 4(c)

$$C_{\text{FET}} = (1/C_g - 1/C_{\text{accumulation}})^{-1}. \quad (1)$$

Finally, differentiating Q_{FET} with respect to C_{FET} yields the Q–V relationship of the baseline FET with the effect of oxide capacitance removed [Fig. 4(d)].

Thus, we partition the FerroFET into: 1) the stand-alone FE capacitor (containing PZT and HfO_2) and 2) the baseline FET without the HfO_2 gate dielectric (FET) [Fig. 5(a)].

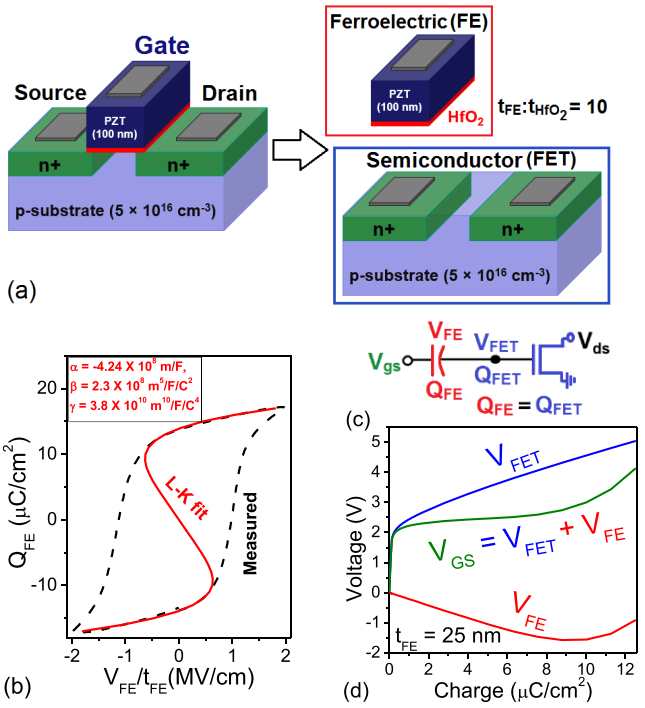

FIGURE 5. (a) Partitioning of the FerroFET into the stand-alone FE (containing PZT and HfO_2) and the baseline Si MOSFET (FET). (b) Experimental P-E (Q_{FE}–V_{FE}/t_{FE}) data and the corresponding fit to the Landau–Devonshire theory for a stand-alone 100-nm PZT on 10 nm HfO_2. (c) Schematic of the FerroFET. (d) Respective voltages, V_{FET}, V_{FE}, and $V_{gs} = V_{\text{FET}} + V_{\text{FE}}$, as a function of Q.

Extraction of the charge–voltage (Q–V) relationship of the baseline FET without the gate dielectric (as described in Fig. 4) and the stand-alone FE capacitor forms the basis for understanding the FerroFET switching mechanism. Fig. 5(b) shows the measured P-E loop data for the 100-nm PZT on a 10-nm HfO_2/Si MOS capacitor. The Landau–Devonshire FE model and Landau–Khalatnikov equation are applied to

the measured P-E data giving a Q–V relationship

$$V_{\mathrm{FE}}/t_{\mathrm{FE}} = 2\alpha P + 4\beta P^3 + 6\gamma P^5. \quad (2)$$

For the series combination of the FE and the FET [Fig. 5(c)]

$$V_{gs}(Q) = V_{\mathrm{FE}}(Q) + V_{\mathrm{MOS}}(Q). \quad (3)$$

The voltage enhancement in the FerroFET results from the FE voltage V_{FE} being of *opposite polarity* to the MOSFET voltage [Fig. 5(d)], V_{FET} for a given Q, thus causing the applied V_{gs} to be less than V_{FET} for a given charge (or I_{ds}). It can also be understood that closer the magnitude of the negative FE voltage V_{FE} is to the positive V_{FET}, the smaller is V_{gs} and the higher is the voltage gain for a given Q. The internal gain ($dV_{\mathrm{FET}}/dV_{gs}$) [Fig. 6(a)] is expectedly low in the subthreshold operation and increases in the inversion regime significantly past the threshold voltage V_{th} (2.2 V). At low I_{ds}, the FET is in depletion and depletion capacitance (C_{FET}) is low. The high degree of mismatch of the FET depletion capacitance with the FE NC ($-C_{\mathrm{FE}}$) and a positive C_{FET} produces a negligible voltage gain. As the device is biased into strong inversion, C_{FET} increases and a higher degree of match with $-C_{\mathrm{FE}}$ produces increased voltage gain, until $C_{\mathrm{FET}} > -C_{\mathrm{FE}}$ and the device enters into the regime of hysteretic operation. With increased thickness t_{FE}, the FE capacitance $|-C_{\mathrm{FE}}|$ decreases, increasing $|-V_{\mathrm{FE}}|$ and enhancing the voltage gain across the FET. The steepest slope in inversion thus provides a crucial point of agreement with the NC path predicted by the Landau–Devonshire theory. The hysteretic behavior of FerroFET is understood by comparing the charge–capacitance (Q–C) relationship of the FET and the stand-alone FE for varying t_{FE}. The FE to linear dielectric thickness ratio, t_{FE}:$t_{\mathrm{HfO_2}} = 10$, is assumed for all cases (such that the Q–C relationship of the FE on high-k dielectric stack can be assumed to scale with thickness). As stated earlier, the hysteresis condition is met when $|C_{\mathrm{FET}}| > |-C_{\mathrm{FE}}|$ for a range of Q [A–B in Fig. 6(b)]. The corresponding I_d–V_g characteristics are shown in Fig. 6(c). Fig. 6(d) shows the calculated hysteresis window for varying t_{FE} (0–150 nm). At $t_{\mathrm{FE}} = 100$ nm (thickness used in the fabricated devices), a hysteresis of 9.1 V is predicted. The experimentally observed hysteresis (∼10 V) is close to the calculated value, producing another critical point of agreement with the Landau–Devonshire theory.

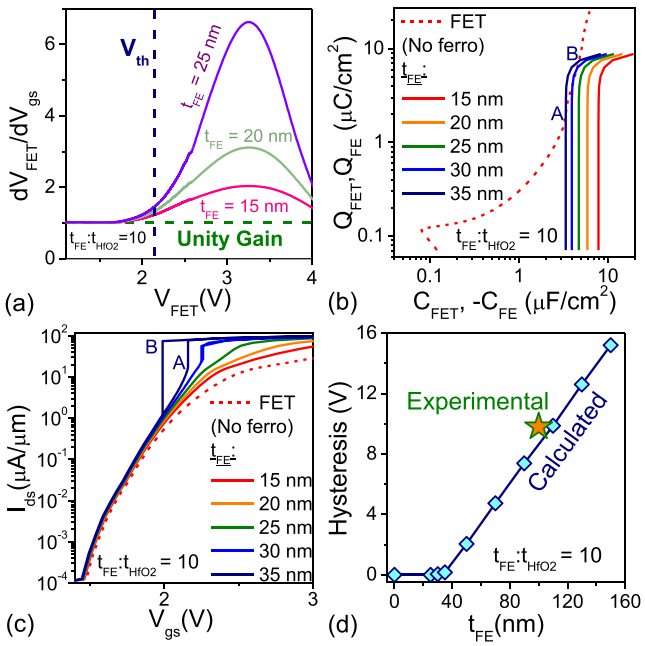

FIGURE 6. Internal voltage gain for the series combination of a stand-alone 100 nm PZT and a baseline FET. t_{FE}: $t_{\mathrm{HfO_2}} = 10$ is assumed for all thicknesses of the stand-alone FE. The highest voltage gain is observed in strong inversion. (b) Charge–capacitance (Q–C) relationship of the FET and the stand-alone FE for varying t_{FE}. (c) Corresponding I_d–V_g characteristics. (d) Calculated hysteresis window for varying t_{FE}. The experimentally observed hysteresis is very close to the value calculated in accordance with the Landau–Devonshire theory.

IV. PROJECTION TO HIGHLY SCALED STRUCURES

Apart from the experimental demonstration of NC FerroFETs with characteristics approaching the predictions of the Landau–Devonshire theory, the above results have another important consequence related to the characteristics of PZT deposited on a nonperovskite substrate. Fig. 5(b) shows the fit of the Landau-Devonshire theory to the measured polarization charge versus electric field characteristics. The fit is used to extract the Landau coefficient, α. A value of $\alpha = -4.24 \times 10^8$ m/F extracted for the PZT deposited on HfO_2. This is a significantly higher negative value than what is expected from PZT grown on substrates with low nucleation energies such as platinum or strontium titanate ($\alpha \sim -10^7$ m/F) electrodes. The Landau coefficient α represents the inverse of the negative permittivity of the FE (ε_r) near zero polarization. Thus, a high value of α implies a proportionally low value of $|-C_{\mathrm{FE}}|$ for a given t_{FE}. This can also be understood in terms of the very high (∼1 MV/cm) coercive field [Fig. 4(b)] of the PZT deposited on HfO_2, compared with 30–100 kV/cm on the conformal substrates. Thus, capacitance matching is obtained for a much smaller t_{FE} for the PZT on HfO_2 than for the PZT on a compatible substrate. A consistent point of concern for FerroFET designs using conventional FEs with high values of $-C_{\mathrm{FE}}$ has been the requirement of a t_{FE} that is impractically high for modern ultrascaled nonplanar transistor architectures with dense spacing [19]. If we consider the example in Fig. 6(b), the largest reduction in operating voltage with nonhysteretic behavior is achieved around $t_{\mathrm{FE}} \sim 30$ nm, with PZT having $\alpha = -4.24 \times 10^8$ m/F. On a substrate with low nucleation energy, with $\alpha = -10^7$ m/F, the same improvement in operating voltage would have been achieved at a very high $t_{\mathrm{FE}} \sim 1.272$ μm.

To better illustrate the point, we show the design considerations for the NC FET using a state-of-the-art Si tri-gate transistor [20] as the baseline device (Fig. 7). Sentaurus 3-D

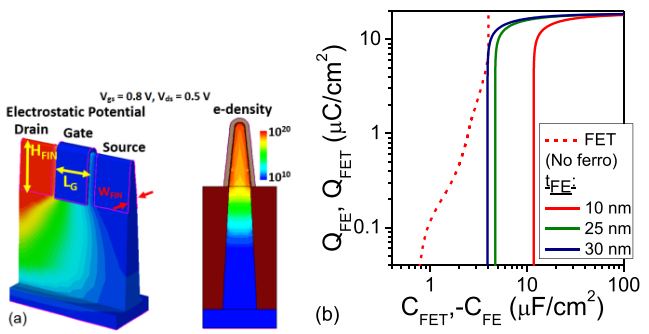

FIGURE 7. (a) Schematic of a Si bulk tri-gate transistor. (b) Charge–capacitance (*Q*–*C*) relationship of the tri-gate FET and the stand-alone FE for varying t_{FE}.

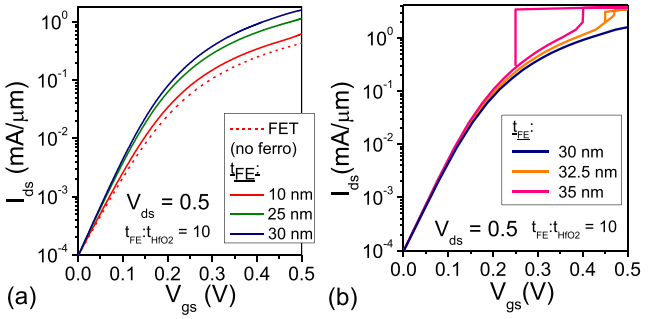

FIGURE 8. (a) Simulated I_d–V_g characteristics for t_{FE} = 10–30 nm on the tri-gate baseline FET TCAD model [10] show nonhysteretic reduction in operating voltage. (b) Further improvement in I_d is possible at the expense of ∼150 mV hysteresis.

Technology computer-aided design (TCAD) simulations are used to extract the Q–V relationship. The simulation model calibrated to a measured device has a gate length $L_G = 26$ nm, effective oxide thickness $E_{OT} = 0.9$ nm with 0.5 nm of SiO_2 sandwiched between HfO_2 and the fin, channel doping $N_{ch} = 10^{16}$ cm^{-3}, and an S/D doping N_{sd} of 10^{20} cm^{-3}. The width at the middle part of the tapered tri-gate is 8 nm with a tapering angle of 84° [20]. Using the I_d–V_g and Q–V relationships of the simulated tri-gate transistor and the measured stand-alone FE capacitor [Fig. 5(b)], the I_d–V_g characteristics are calculated as shown in Fig. 8 for different t_{FE}. The projected scaled FerroFETs incorporating the 10-nm-thick PZT dielectric exhibits an ON-current of 622 μA/μm with an OFF-current of 100 nA/μm at $V_{ds} = V_{gs} = 0.5$ V, which is 50% higher than the corresponding 22-nm technology node FinFET operating at the same bias condition. Further improvement in I_d is achieved at the expense of ∼150 mV hysteresis as the thickness of the FE t_{FE} is increased to 35 nm. However, such a thick dielectric wrapping the fins is not practically feasible due to continued fin pitch scaling. We should note that the lower polarization charge of the sputtered polycrystalline PZT film aids in capacitance matching with the FinFET inversion capacitance. With PZT deposited on compliant substrates, such an improvement would have required $t_{FE} > 1$ μm (for reasons mentioned in the last paragraph), which is clearly impractical at such extremely scaled complex architectures, necessary for achieving good electrostatic control. Thus, it appears that the polycrystalline insulator, essential for compatibility with a manufacturable device technology, plays the serendipitous role of enabling the low-negative ε_r FE that is critically important for the NC FerroFET to succeed at highly scaled dimensions.

Although the low-negative dielectric constant ε_r is necessary from a design perspective, the effort to realize this using a nonperovskite substrate for PZT comes with added technological challenges. The assumption that the basic FE properties stay unchanged with varying t_{FE} is not true at the dimensions of interest ($t_{FE} \sim$ 10–30 nm) for PZT. There are fewer convincing demonstrations of ferroelectricity at such a small t_{FE}. In addition, it is not clear how the properties of PZT (or another FE insulator) would actually change with the thickness of the silicon-compatible nonperovskite dielectric. For the fabricated devices, scaling the HfO_2 barrier was limited by the volatility of Pb [21], [22] and its tendency to diffuse into the underlying channel. The highly defective nonideal interface between the HfO_2 and PZT and the interfacial mixed layer is also probably the reason for the fabricated devices not having characteristics exactly matching the predictions of the Landau–Devonshire theory (such as higher turn-on voltage in experiments).

While PZT poses a number of challenges as a candidate for capacitance-matching-based NC FETs, most semiconductor-technology-compatible FEs have similar issues. Doped HfO_2–ZrO_2 alloys, which show stabilization of FE phase after high-temperature treatment and strain quenching, have generated much interest recently due to the compatibility of HfO_2 with manufacturable device technologies [22]–[25]. However, the published values of remnant polarization charge density and coercive field are in the ∼20 μC/cm^2 and ∼2 MV/cm ranges, respectively. Thus, reaching a $-C_{FE}$ value of 2–3 μF/cm^2 (to achieve optimal capacitance matching with state of the art FET C_{gg}) would require 33–50-nm-thick films, thereby providing no significant advantage over the PZT in terms of scalability. Perovskite FE such as $BaTiO_3$ or $Sr_{0.8}Bi_{2.2}Ta_2O_9$ also exhibits very high $-C_{FE}$ at sub-10-nm thicknesses, which is detrimental for efficient capacitance matching. In addition, most perovskite FEs conventionally require a compatible substrate such as $SrTiO_3$ for good crystalline quality growth at small thicknesses, introducing extra process complexity.

V. CONCLUSION

The demonstration of steep switching slope (13 mV/dec) over two orders of magnitude change in drain current in strong inversion is an important step in realizing FerroFETs with characteristics consistent with a physically palusible NC theory. Our results provide strong motivation for further exploration of scaled FE thin films with robust electrical properties desired for transistor gate-stacks. A thin-film FE with more uniform crystallinity and less defects is expected

to produce FerroFETs with improved agreement with theoretical models as well as improved yield and reliability.

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