III–V Tunnel FET Model With Closed-Form Analytical Solution

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***Abstract*— Using an idealized semianalytical model of charge transport for InAs-based tunneling FET, it is shown that the output and transfer characteristics can be accurately reproduced and could be used to develop compact models. The use of a mathematical approximation for the analytical solution of the surface potential is vital here to minimize the computation time. The 20-nm gate homojunction and 40-nm gate heterojunction transistors have been simulated and compared with the calibrated numerical simulation results. The results are in good agreement.**

***Index Terms*— Band-to-band tunneling (BTBT), heterojunction, homojunction, lookup table, tunneling FET.**

I. Introduction

TUNNELING FETs have been prime candidates for low power electronic circuits because of their demonstrated faster switching compared with advanced MOSFETs [1]–[4]. Fundamentally, the switching speed of a typical MOSFET is limited by its operating temperature, whereas in a tunnel FET (TFET), operation at a lower supply voltage with larger tunneling current is achievable [5]. Computer simulations of TFET-based circuits are usually carried out using a lookup table-based approach, which is computationally demanding for simulation and testing of large device count circuits. If a compact mathematical model could accurately predict the performance of TFETs in a shorter time compared with lookup table-based or numerical models, it would be highly useful for efficient circuit simulation of TFET-based systems [6]. In this paper, a semianalytical model is presented to predict the current/voltage and charge control characteristics of homojunction and heterojunction TFET devices. The main purpose of this model is to test the potential of technology for implementation in low-power analog and digital circuits. This has been achieved using simplified physical mechanisms to facilitate a shorter simulation time compared with a lookup table-based model. The basis used here has been derived from the compact model for double-gate silicon tunneling FETs [7], but modified to III–V material-based homojunction and heterojunction vertical TFET [8]. A mathematical approximation that has an analytical solution for the surface potential of a double-gate structure is used to determine the dc characteristics of the TFETs. This model can also predict the capacitance effect of homojunction TFET by first determining the charge at each terminal and then taking a derivative of this charge with respect to the applied voltage.

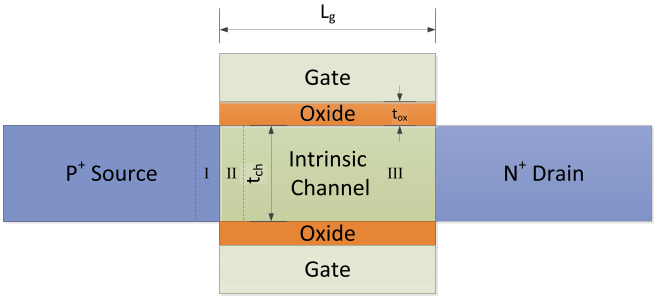

Fig. 1. Schematic cross section of the tunneling FET under study. The equation for electrical current is derived by solving Poisson's equations in Regions I–III and matching the boundary conditions across the interfaces [2]. Regions I and II: gated tunneling diode regions. Region III: DG-MOSFET region.

II. Modeling Procedure

A cross section of the modeled III–V-based vertical TFET is shown in Fig. 1. The double-gate homojunction InAs-based TFET consists of a p+ doped source region, an intrinsic channel region under the vertical double-gate structure followed by an n+ doped drain region. In the case of heterojunction TFETs, the source is made up of p+ doped GaSb. The device is reverse biased for normal operation with the source terminal connected with ground and the drain terminal connected with a positive voltage, creating depletion regions on either side of the source–channel junction. This reverse voltage bends the band structure, which brings the valence band edge of the source region closer to the conduction band edge of the channel region. When a positive voltage bias is applied at the gate terminal, empty electron states are created in the channel region and band-to-band tunneling (BTBT) of electrons from valence band in the source to the conduction band in the channel takes place. These electrons then get transported to drain due to the applied positive bias at the drain terminal.

In the original model [7], the device is analyzed as a series combination of a gated tunnel diode and a

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TABLE I
PHYSICAL PARAMETERS USED IN THE MODEL

SYMBOL	PARAMETER	VALUE	
		Homojunction	Heterojunction
L_g	Gate Length	20 nm	40nm
W_g	Gate Width	1 μm	1 μm
t_{ch}	Channel Thickness	5 nm	5nm
t_{ox}	Oxide Thickness	5 nm	2.5nm
N_s	Source Doping	$4x10^{19}$ cm^{-3}	$4x10^{19}$ cm^{-3}
N_d	Drain Doping	$6x10^{17}$ cm^{-3}	$6x10^{19}$ cm^{-3}
ε_{ch}	Dielectric Constant (Channel)	15.1	15.1
ε_{ox}	Dielectric Constant (Oxide)	21	21
m^*	Effective Tunneling Mass	$0.06m_0$	$0.06\ m_0$
E_g	Effective Tunneling Bandgap	0.383 eV	0.243eV

double-gate MOSFET (DG-MOSFET). This allows Poisson's equations to be solved in the three regions of the device: 1) Region I—the depletion region on the source side; 2) Region II—the depletion region in the intrinsic channel; and 3) Region III—the equivalent of a channel region of a DG-MOSFET. The boundary conditions are then matched, and the depletion lengths for the source junction are obtained. Using these values of the depletion length, the minimum tunneling distance from the valence band edge in the source-to-conduction band edge in the channel can be defined and calculated [9]. The parallel gate geometry and device parameters used in the model have been obtained from technology computer aided design (TCAD) simulations calibrated with the experimental results [10]. The tunneling probability is related to the minimum tunneling distance ($W_{t,\min}$) by the following relationship according to Kane's model [11] of BTBT:

$$W_{t,\min} = L_1 + L_2 - \lambda \cdot \cosh^{-1}\left(\frac{V_{gs} - V_{fbs} - \varphi_I}{V_{gs} - V_{fbb} - \varphi_{dg}}\right) - \sqrt{\frac{2\varepsilon_{ch}}{q N_{seff}}\left(\varphi_I - \frac{E_g}{q}\right)}. \quad (1)$$

In addition to the physical parameters given in Table I, q is the magnitude of electronic charge, λ is the natural length of DG-MOSFET $[(t_{ch} \cdot \varepsilon_{ch}/2 \cdot C_{ox})^{1/2}]$, where C_{ox} is oxide capacitance per-unit t_{ox}. V_{fbb} is the channel flat band voltage given by the work function difference between the gate and the channel, and V_{fbs} is the flat band voltage for source given by work function difference between the gate and the source. N_{seff} is the source doping concentration, and φ_I is the reference potential. L_1 and L_2 are diffusion lengths for the source and channel regions, respectively, which can be obtained using the following equations [7]:

$$L_1 = \sqrt{\frac{2\varepsilon_{ch}\varphi_s(0)}{q N_{seff}}} \quad (2)$$

$$L_2 = \lambda \cdot \cosh^{-1}\left(\frac{V_{gs} - V_{fbs} - \varphi_s(0)}{V_{gs} - V_{fbb} - \varphi_{dg}}\right). \quad (3)$$

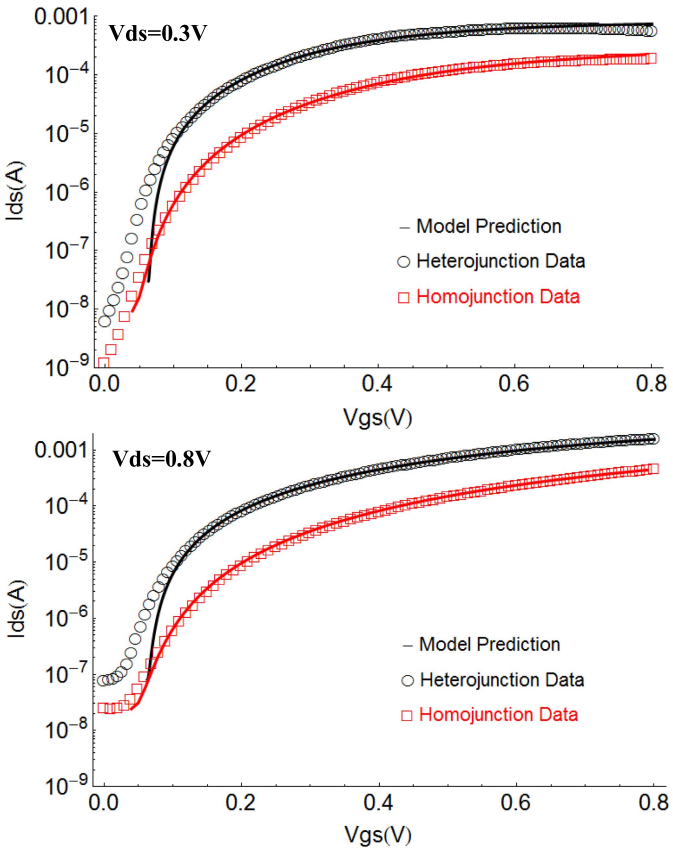

Fig. 2. Model prediction (line) for homojunction and heterojunction TFET devices at $V_{ds} = 0.3$ V (top) and $V_{ds} = 0.8$ V (bottom). The same model can predict drain current for both the cases with better agreement for the case of homojunction device. Solid lines: presented compact model prediction. Discrete symbols: experimental-based TCAD data [12], obtained by calibrating TCAD results with the experimental data.

With $\varphi_s(0)$ being the surface potential at the source junction and φ_{dg} being the surface potential of DG-MOSFET. Using this BTBT model, the total drain current (I_{ds}) equation can be obtained by relating the electron tunneling probability ($G_{t,\max}$) with the minimum tunneling distance [11]

$$G_{t,\max} = A \cdot E_g^{\frac{3}{2}} \cdot \frac{1}{W_{t,\min^2}} \exp\left[-\frac{q W_{t,\min}}{B \cdot E_g^{\frac{1}{2}}}\right] \quad (4)$$

$$I_{ds} = 2 \cdot B \cdot E_g^{\frac{1}{2}} \cdot G_{t,\max} \cdot W_g \cdot t_{ch} \cdot f_{fermi}. \quad (5)$$

In (4) and (5), A and B are Kane's tunneling coefficients, which are a function of the effective tunneling mass and the effective tunneling energy gap. The values of effective tunneling bandgap and effective tunneling mass are the same values used in the TCAD simulations and have been obtained from atomistic simulations of band structure. f_{fermi} is a correction term introduced to ensure zero drain current at $V_{ds} = 0$ V in the output characteristics.

III. TRANSFER CHARACTERISTICS

A comparison of transfer characteristic results between the homojunction and the heterojunction devices is shown in Fig. 2 for two different values of V_{ds} for simplicity. The discrete symbols represent the results calculated using

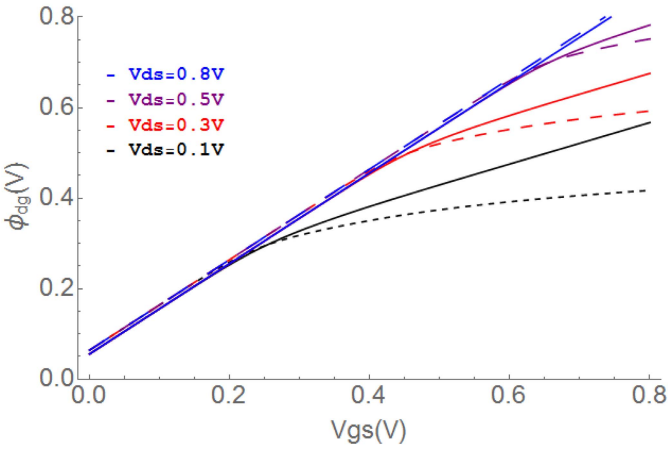

Fig. 3. Comparison between the iteratively calculated value of surface potential (dashed lines) and the mathematical approximation of surface potential (solid lines) in homojunction TFET at different drain bias voltages. The APE for this comparison is listed in Table II.

device calibrated TCAD simulations, and the solid lines represent the predictions of semianalytical model. The TCAD simulations also use idealized double-gate geometry and use Fermi statistics while accounting for carrier degeneracy. The correlation between the TCAD results and the model data shows that the model can accurately predict the variations in current as a function of V_{gs} over a wide range of V_{ds} values. By considering the different dielectric constants and work function of different materials on each side of the tunneling junction in the case of heterojunction TFET, new values of L_1 and L_2 can be obtained to model the drain current. The homojunction agrees very well and the heterojunction under predicts the current in the subthreshold region.

One possible cause for this could be that the model assumes that the electric field profiles are uniform across the source–channel junction. In a heterojunction, the field originates and terminates in different materials. While the TCAD takes this into account, this effect has not been considered in the model and could contribute to the under prediction of drain current. Recent reports have also indicated that material effects in mixed As/Sb staggered gap could contribute to this [12], [13].

Our main contribution in obtaining this model was to use a mathematical approximation for surface potential in a double-gate structure. The surface potential in a double-gate structure has a form of Lambert's W function which does not have a closed-form analytical solution and requires an iterative process (Fig. 3). We used a simple mathematical approximation for this function which has a relatively small absolute percentage error (APE) for the surface potential of the device (Table II) [14]. This mathematical approximation has the form of the following equation:

$$W(z) = \ln\frac{12\cdot z}{5\cdot \ln\left(1+\frac{12\cdot z}{5}\right)} \tag{6}$$

$$\varphi_{dg} = V_{gs} - V_{fbs} - 2W(z)/\beta \tag{7}$$

where $\beta = q/kT$. The equations and coefficients used to determine the parameter z have been obtained from an earlier work on surface potential of DG-MOSFETs [15]. In this case,

TABLE II
APE FOR SURFACE POTENTIAL

VGS(V)	VDS(V)	ABSOLUTE % ERROR
0.1V	0.1	5.188
	0.3	5.220
	0.5	5.220
	0.8	5.220
0.8V	0.1	35.975
	0.3	14.060
	0.5	4.086
	0.8	0.986

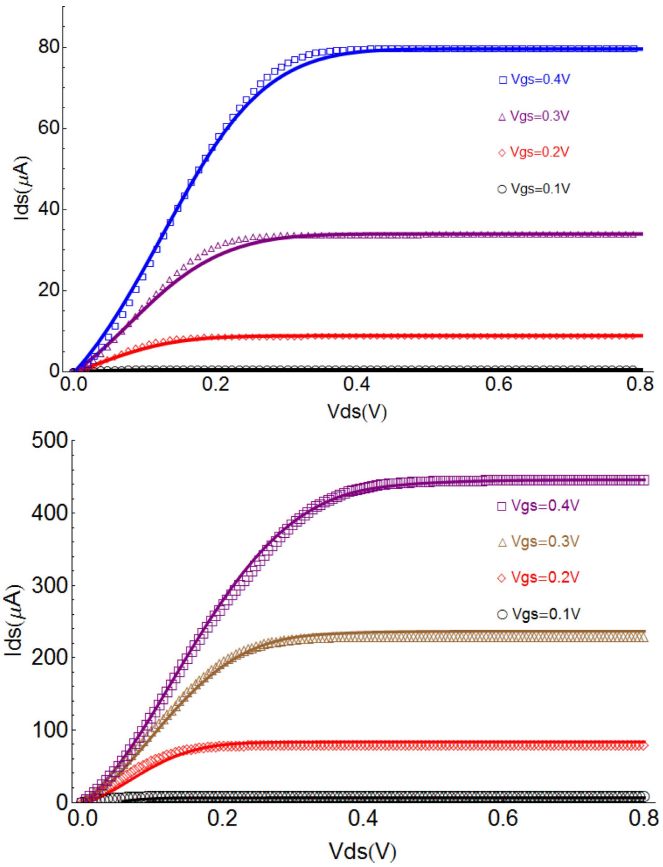

Fig. 4. Output characteristics of homojunction (top) and heterojunction (bottom) TFETs. The model results show good agreement for both the homojunction and the heterojunction devices.

z is a function of material parameters n_i and ε_s and applied voltages V_{gs} and V_{ds}. There have been reports of analytical solutions of DG MOSFETs using similar or different approaches [16]–[19]. However, none of these approaches utilize a mathematical approximation to obtain the surface potential solution. The reasoning behind the use of this particular approximation over others will be discussed in Section VII.

IV. OUTPUT CHARACTERISTICS

The output characteristics predicted by the model for both the cases are shown in Fig. 4 with homojunction (top)

TABLE III
INVERTER SIMULATION COMPARISON

	EFFECTIVE CURRENT	SWITCHING RESISTANCE
INVERTER MODEL	95μA	1.3KΩ
THIS WORK	97 μA	1.3KΩ

and heterojunction (bottom) TFETs. As evident from the figures, the model can accurately predict the drain current values over a wide range of drain bias voltages. The same analytical procedure from homojunction device model has been used to obtain the heterojunction device characteristics, demonstrating that this approach can be used to accurately predict device performance for use in circuit simulations.

V. INVERTER SIMULATION

For self-consistency, results derived from this model have been tested by applying to the inverter model presented in [20]. Using the output characteristic data from this study, the effective switching current and switching resistance has been extracted for a TFET inverter. The comparison between the results from [20] and our model is shown in Table III.

Although the device dimensions used to derive and calibrate our model were different from [20], both the effective current and the switching resistance can still be predicted accurately.

VI. CAPACITANCE MODELING

For capacitance modeling, (8)–(10) are used to obtain the charge at the drain, source, and gate terminal, respectively [21]

$$Q_d = -2W_g(L_g - L_2)C_{\rm ox}(V_{\rm gs} - V_{\rm fbs} - V_{\rm bi} - \emptyset_{\rm dg}) + W_g t_{\rm ch}\varepsilon_s E_m \quad (8)$$

$$Q_s = qN_{\rm seff}L_1 t_{\rm ch} \quad (9)$$

$$Q_g = -(Q_d + Q_s) \quad (10)$$

where E_m is the maximum electric field at the drain junction which is given by $[(V_{\rm ds} - V_{\rm bid} - \varphi_{\rm dg})/\lambda]$, where $V_{\rm bid}$ is the built-in potential of the drain junction. By differentiating the charge at each terminal with respect to applied terminal voltages and then substituting the values of the gate and drain voltages, the terminal capacitances can be found

$$C_{\rm gs} = -\frac{dQ_s}{dV_{\rm gs}} \text{ and } C_{\rm gd} = -\frac{dQ_g}{dV_{\rm ds}}. \quad (11)$$

Fig. 5 shows a comparison between the model prediction and the TCAD simulation results for a 20-nm InAs homojunction TFET. These results show the variations in gate-to-source and gate-to-drain capacitance values as a function of both $V_{\rm gs}$ and $V_{\rm ds}$. Using this approach, the presented model can predict the general behavior of charge control accurately; however, there are minor variations in the characteristics of $C_{\rm gd}$. The fact that the model can predict the essential inflection points on the capacitance curves with relatively small error points to the validity of the approach for implementation in a compact model.

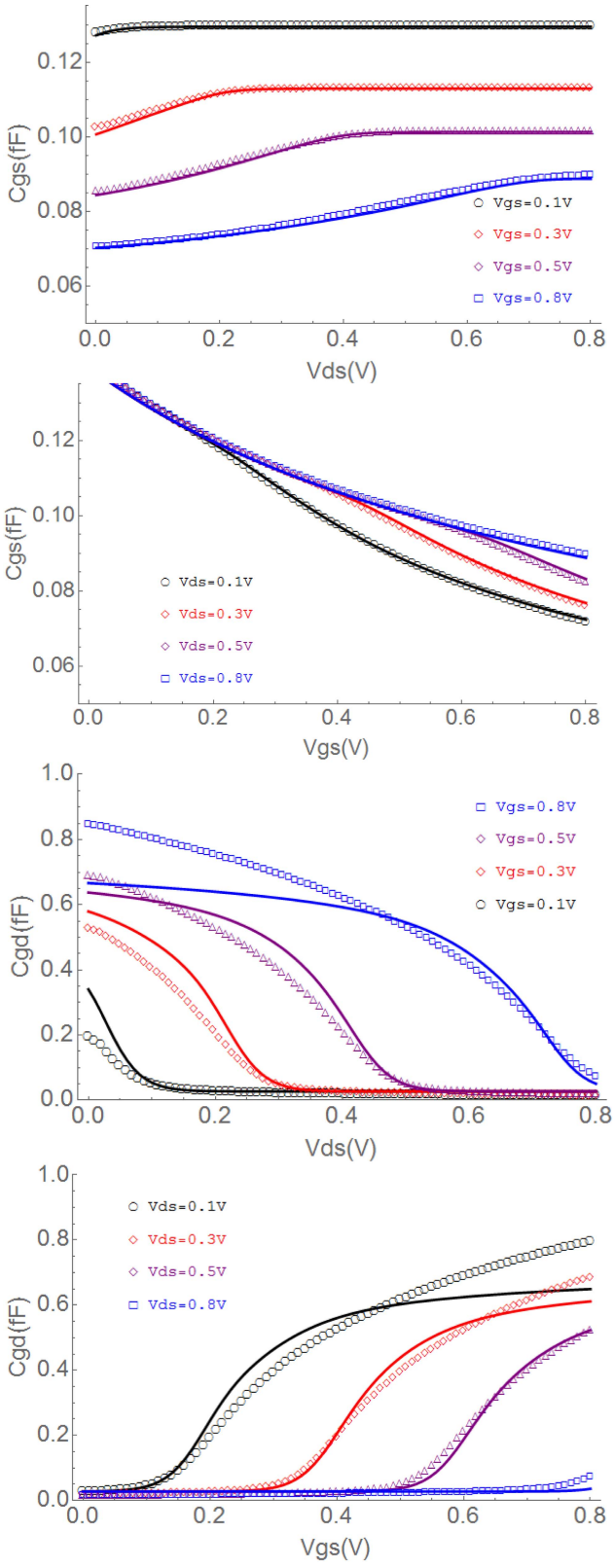

Fig. 5. Capacitance–voltage characteristics for a 20-nm InAs homojunction TFET. Solid lines: model prediction. Discrete symbols: TCAD data.

VII. DISCUSSION

In the transfer and output characteristics, the only region where the model prediction deviates from the TCAD results is in the subthreshold regime of the transfer characteristics for heterojunction TFET, where the model under-predicts

the current. One possible reason for this has already been explained in Section III. In addition, a fringe electric field exists at the source terminal due to gate electrode which affects the electron distribution in the valence band at the source/channel interface [3], [10]. The modeled structure does not consider these effects and these factors individually or in combination could cause the current prediction from the model to deviate from the TCAD results.

In the cases of C_{gd}, the change in terminal charge with respect to gate and drain bias voltages is more abrupt than what it should be. As a result, the derivative of surface potential rises and saturates quickly. This causes the model to over predict the capacitance before the inflection points and under predict the capacitance after the inflection. Finally, some aspects of device geometry can also have an effect on parasitic capacitance of the structure and the bias voltage dependence of capacitance. Since these effects were not considered in this simplified model, the deviations could be attributed to them.

Other analytical approximations for Lambert's W function were also tested to obtain the lowest APE, such as Pade approximant and Taylor series expansion. Even though these closed-form analytical solutions produced a much lower APE, they could not predict the capacitance characteristics accurately, with the derivatives going to infinity near the origin. The presented model has a distinct advantage over lookup table-based models which can predict device characteristics only at discrete operating points. The next step would be to set up these model equations in a commercial circuit simulator to test the validity of the model at the circuit level for analog and/or digital systems. Since the operation of TFET is highly dependent on the physical geometry of the device structure, these differences in geometry translate into variations in physical mechanisms that govern device operation, making it difficult to obtain a universal compact model for TFETs. A better approach would be to develop compact analytical models specific to the device structures and geometries rather than a universal compact model for generic TFET devices. These models can then be used to test the performance of TFET-based circuits and systems.

VIII. Conclusion

Results from a semianalytical model of charge transport in the homojunction and heterojunction III–V-based TFETs have been calculated. The model equations do not require any iterative procedure to obtain device characteristics, proving it useful for high speed simulations compared with the lookup table-based models. By implementing this model in a circuit simulator, the potential of technology can be tested at the circuit level. The results have demonstrated that this model can accurately predict the dc current characteristics of both the homojunction and the heterojunction devices and capacitance characteristics of homojunction TFET devices with marginal error.

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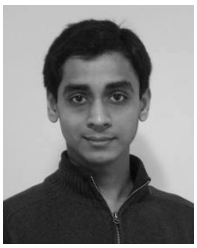

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