0.5 V Supply Voltage Operation of $In_{0.65}Ga_{0.35}As/GaAs_{0.4}Sb_{0.6}$ Tunnel FET

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***Abstract*— In this letter, we demonstrate using fast current–voltage measurements, low switching slope of 64 mV/decade over a drain current range between 10^{-3} and 2×10^{-2} μA/μm in staggered-gap $In_{0.65}Ga_{0.35}As/GaAs_{0.4}Sb_{0.6}$ tunneling field-effect transistors (TFETs) at $V_{DS} = 0.5$ V. This is achieved through a combination of low damage mesa sidewall etch and improvement in electrical quality of the high-κ gate-stack. Benchmarking our results against experimentally demonstrated TFETs, we conclude that, the staggered-gap TFETs are capable of achieving simultaneously high drive current and low switching slope.**

***Index Terms*— III-V, tunnel FET, steep switching slope.**

I. Introduction

Tunneling field effect transistors (TFETs) based on band-to-band tunneling of carriers have been identified as a promising candidate to replace conventional CMOS for low power logic applications [1], [2]. Though many material systems have been studied, TFET within the III-V compound semiconductor material system has recently gained interest due to the direct bandgap, lower effective mass of tunneling carriers, tunability of the effective barrier height (E_{Beff}) for tunneling by implementing mixed-arsenide-antimonide hetero-junctions [3], [4], all of which improves the efficiency of the band-to-band tunneling process. Many experimental III-V TFETs have been reported. However, the demonstrated TFETs either achieve steep switching slope or high drive currents, but not simultaneously [5]–[10]. It has been established that in order to outperform MOSFET at low supply voltages, TFET is required to achieve low switching slope as well as high on-state drive currents [11]. A hetero-junction TFET which simultaneously achieves high drive current (I_{ON}) as well as steep switching slope (SS) requires (a) high quality of the hetero-structure material to minimize the bulk OFF state leakage current [12] and (b) high quality gate stack to minimize trap assisted tunneling [13].

Manuscript received October 18, 2014; accepted November 1, 2014. Date of publication November 6, 2014; date of current version December 22, 2014. This work was supported by the National Science Foundation Nanosystems Engineering Research Center through the Advanced Self-Powered Systems of Integrated Sensors and Technology under Award EEC-1160483. The review of this letter was arranged by Editor S. J. Koester.

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Digital Object Identifier 10.1109/LED.2014.2368147

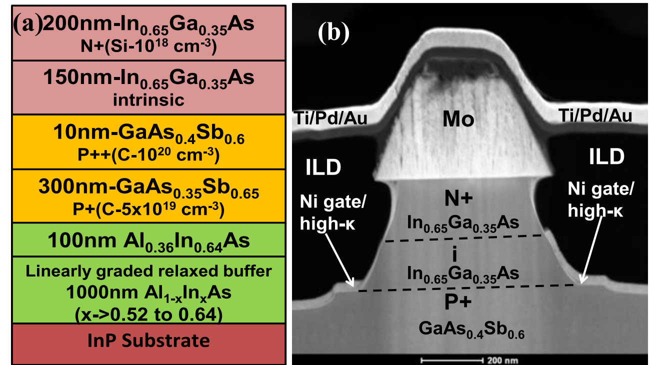

Fig. 1. (a) Cross-section schematic of the staggered-gap TFET layer structure. (b) Cross-section TEM image of the fabricated staggered-gap TFET.

In this work, we demonstrate staggered-gap $In_{0.65}Ga_{0.35}As/GaAs_{0.4}Sb_{0.6}$ TFET with a minimum SS of 64mV/decade at $V_{DS} = 0.5V$, $T = 300K$. Controlled epitaxial growth of hetero-structure (details in section II) and low damage mesa sidewall etch ensured low OFF state current (I_{OFF}). An *in-situ* plasma treatment is carried out to improve the gate stack quality. Further, thermally evaporated nickel (Ni) metal is used as gate electrode. The advantage of thermal evaporation of gate metals has already been reported through MOS capacitor based experiments [14] on planar $In_{0.53}Ga_{0.47}As$ surfaces. In this work, for the first time, we experimentally demonstrate that thermal gate metal evaporation significantly improves vertical TFET characteristics compared to electron beam evaporation process. I-V measurement is carried out to further improve the TFET characteristic by minimizing the residual interface states response.

Section II describes the layer structure and device fabrication details; section III discusses the electrical results and benchmarks I_{ON}, SS and I_{ON}/I_{OFF}; section IV concludes this letter.

II. Layer Structures and Device Fabrication

Figure 1(a) shows the layer structure of the $In_{0.65}Ga_{0.35}As/GaAs_{0.4}Sb_{0.6}$ n-channel TFET (nTFET) grown using solid source molecular beam epitaxy on semi-insulating InP substrate. The channel material consists of 150nm of intrinsically doped $In_{0.65}Ga_{0.35}As$ and the source material consists of heavily p-type doped $GaAs_{0.4}Sb_{0.6}$. To ensure high quality of the epi-layer, InAs like surface termination was implemented while switching from $GaAs_{0.4}Sb_{0.6}$ to $In_{0.65}Ga_{0.35}As$ as reported in our previous works [12], [15]. The tunnel barrier height, E_{Beff}, for this material system is approximately

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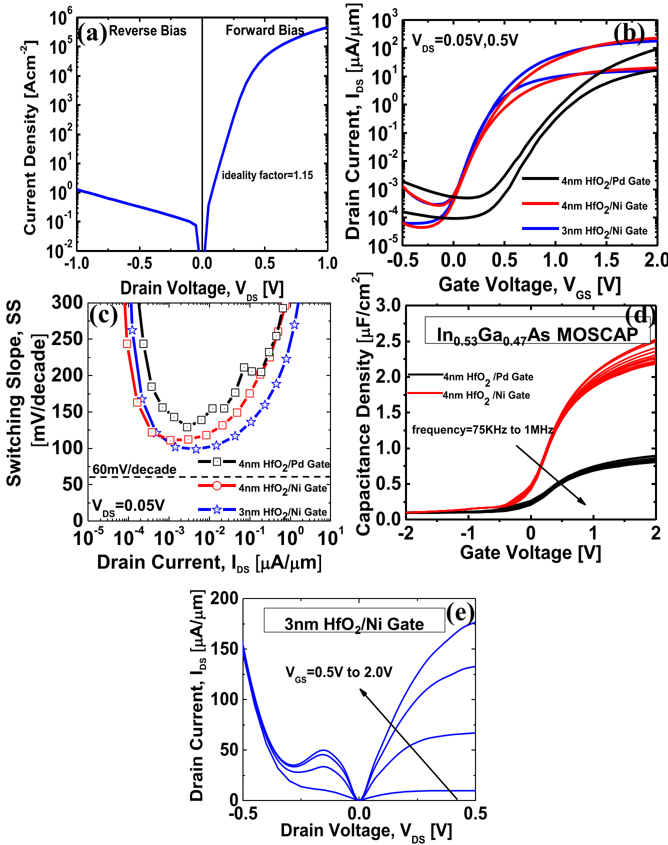

Fig. 2. (a) Floating gate p-i-n diode characteristics at $T = 300K$. (b) Transfer characteristics of TFET with different gate stacks at $T = 300K$ and for $V_{DS} = 0.05V, 0.5V$. (c) SS as a function of drain current showing improvement with thermal gate metal evaporation and EOT scaling. (d) C-V characteristics of MOSCAPs with gate stacks (1) and (2). (e) Output characteristics showing good saturation and NDR characteristics.

0.31eV [12] and, thus represents a staggered-gap hetero-junction. Figure 1(b) shows the cross-section transmission electron microscopy (TEM) micrograph image of the fabricated staggered-gap nTFET. A self-aligned gate nano-pillar process flow was used to fabricate the vertical TFET [16] with dual side gates. The mesa sidewall etch was performed in BCl_3 based plasma followed by a citric acid based wet etch. Prior to the deposition of HfO_2 high-κ dielectric by atomic layer deposition (ALD) process, in-situ nitrogen plasma treatment was carried out to reduce the interface states density and scale the electrical oxide thickness (EOT) [17]. The gate metal composed of 20nm of either Palladium (Pd) deposited using electron-beam evaporation process or Ni deposited using thermal evaporation process.

III. Results and Discussions

Figure 2(a) shows the floating gate p-i-n diode characteristics of the fabricated TFET measured at room temperature. An ideality factor of 1.15 is extracted, averaged over diode current in the range of $1A.cm^{-2}$ to $10^3A.cm^{-2}$. Further, low level of reverse leakage current is also achieved ($0.3Acm^{-2}$ at $V_{DS} = -0.5V$). This indicates a high quality of the hetero-junction which is critical in realization of the steep slope in a TFET [12]. TFETs were fabricated with three types of gate stack: (1) 4nm HfO_2/Pd gate (2) 4nm HfO_2/Ni gate and (3) 3nm HfO_2/Ni gate. Figure 2(b) shows the transfer characteristics ($I_{DS}-V_{GS}$) of the fabricated TFETs with the three gate stacks, measured at $T = 300K$ and $V_{DS} = 0.05V, 0.5V$. In TFET with gate stack (1), for $I_{OFF} = 1nA/\mu m$, at $V_{DS} = 0.5V$ and $V_{GS}-V_{OFF} = 1.5V$, I_{ON} of $84\mu A/\mu m$ is achieved. This corresponds to an I_{ON}/I_{OFF} ratio of 8.4×10^4. However, at $V_{GS}-V_{OFF} = 0.5V$, I_{ON} and I_{ON}/I_{OFF} drops to $0.43\mu A/\mu m$ and 430 respectively. Further, drain induced barrier thinning (DIBT) of 0.15V is measured at $I_{OFF} = 1na/\mu m$, indicative of poor device electrostatics. In TFETs with gate stack (2) and (3), I_{ON} of $130\mu A/\mu m$ is achieved at $V_{GS}-V_{OFF} = 1.5V$ and $V_{DS} = 0.5V$. This corresponds to a 42 % increase in comparison to the TFET with gate stack (1). Correspondingly, I_{ON}/I_{OFF} ratio increased to 1.3×10^5 at $V_{DS} = 0.5V$. Further, the DIBT is also negligible. Figure 2(c) shows the SS as a function of drain current (I_{DS}) at $V_{DS} = 0.05V$. SS improved from 130mV/decade in TFET with gate stack (1) to 105 mV/decade in gate stack (2), by reducing the gate metallization induced damage. By scaling EOT, a minimum SS (SS_{MIN}) of 97mV/decade is achieved in TFET with gate stack (3) at $V_{DS} = 0.05V$. Thus, at $V_{GS}-V_{OFF} = 0.5V$, I_{ON} of $4.3\mu A/\mu m$ and I_{ON}/I_{OFF} of 4.3×10^3 are achieved. Figure 2(d) shows the capacitance-voltage (C-V) characteristics of MOS capacitors (MOSCAPs) fabricated with gate stacks (1) and (2). MOSCAP with gate stack (1) exhibits lower accumulation capacitance and higher dispersion in the mid-gap region. It is known that electron-beam evaporation can significantly damage the oxide/semiconductor interface, most likely due to the x-rays generated in the process [14], [18]. It is also possible that an unintentional oxide layer be formed during the electron-beam evaporation of Pd [19]. Therefore, thermally evaporated Ni gate electrode improves TFET characteristics by improving EOT as well as reducing mid-gap D_{it}. The output characteristic of TFET with gate stack (3) shows excellent saturation and negative differential resistance (NDR) characteristics indicating efficient band-to-band tunneling process (figure 2(e)).

To further improve the SS by minimizing the trap response, fast I-V measurement was carried out on TFET with gate stack (3). The rise time of the gate voltage pulse was $1\mu s$ and a two stage amplifier with a gain of 2×10^4 was used to accurately sense low current in the sub-threshold regime. Significant steepening in the $I_{DS}-V_{GS}$ characteristic is observed with fast IV measurements and SS_{MIN} of 64mV/decade is achieved over an order of magnitude range in drain current level (figures 3(a-b)). At $I_{OFF} = 1nA/\mu m$, for $V_{GS}-V_{OFF} = 0.5V$ and $V_{DS} = 0.5V$, I_{ON} improved to $8.4\mu A/\mu m$.

Figures 4(a-b) show the SS vs I_{DS} and I_{ON} vs SS_{MIN} characteristics, respectively, for the best experimentally reported nTFETs till date, at high V_{DS}. The staggered-gap TFET simultaneously achieves high drive current and low SS. Figure 4(c) compares the $I_{DS}-V_{GS}$ characteristic of the staggered-gap TFET with Si Fin-FET at channel length of 150nm and $V_{DS} = 0.5V$. Sentaurus TCAD based numerical simulation was carried out to predict the $I_{DS}-V_{GS}$ characteristics of Silicon Fin-FET at similar channel length

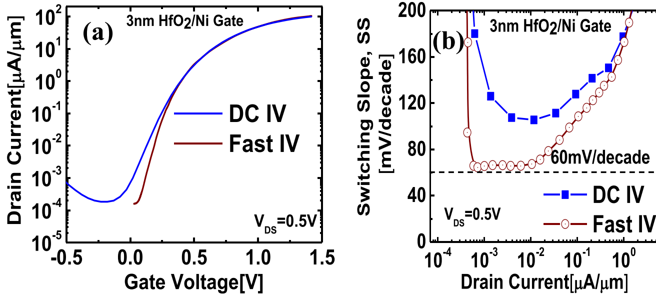

Fig. 3. (a-b) Transfer characteristics and SS improve with fast I-V measurement. Minimum SS of 64mV/decade is achieved at $V_{DS} = 0.5V$.

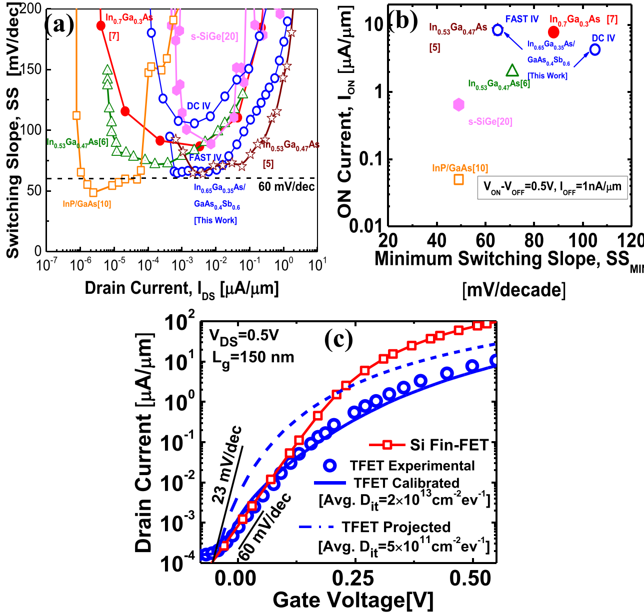

Fig. 4. (a) SS vs I_{DS} characteristics and (b) benchmarking I_{ON} vs SS_{MIN} against the best reported nTFETs till date at high V_{DS}. (c) Comparison of the staggered-gap TFET with Si Fin-FET at channel length of 150nm, $V_{DS} = 0.5V$.

of 150nm [21]. Silicon Fin-FET model was calibrated to the experimental data of 26nm gate length commercial Fin-FETs [22]. Further, TFET numerical simulation models were calibrated with the measured staggered-gap TFET characteristics using an average D_{it} value of $2 \times 10^{13} cm^{-2} eV^{-1}$.

With a projected reduction in average D_{it} to $5 \times 10^{11} cm^{-2} eV^{-1}$, SS_{MIN} of 23mV/decade is achieved and thus TFET outperforms Si Fin-FET at lower $V_{GS} - V_{OFF}$ of 0.25V. However, to outperform Si Fin-FET at scaled L_g, scaling of body thickness and EOT of TFET are required [11].

IV. Conclusion

To summarize, $In_{0.65}Ga_{0.35}As/GaAs_{0.4}Sb_{0.6}$ staggered-gap TFET is fabricated and characterized. High quality of the epitaxial hetero-structure is confirmed through p-i-n diode measurements. Thermal gate metallization coupled with improved high-k dielectric/III-V interface resulted in a 42% improvement in the ON state current at $V_{GS} - V_{OFF} = 1.5V$, $V_{DS} = 0.5V$. A minimum SS of 97mV/decade is achieved at $V_{DS} = 0.05V$ with negligible DIBT for a channel length of 150nm. With fast IV measurement, SS is further reduced to 64mV/decade and I_{ON} of 8.4μA/μm is achieved at $V_{GS} - V_{OFF} = 0.5V$, $V_{DS} = 0.5V$ which is among the highest reported in the category of III-V TFETs.

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