Impact of Sidewall Passivation and Channel Composition on $In_xGa_{1-x}As$ FinFET Performance

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***Abstract*— We experimentally demonstrate $In_xGa_{1-x}As$ FinFET devices with varying indium composition and quantum confinement effect. While increasing indium content enhances drive current by increasing the injection velocity, increasing quantum confinement enhances the drive currents by significantly improving the short-channel effects. Further, improved sidewall passivation using an *in situ* plasma nitride passivation process provides additional improved subthreshold behavior. Competitive drive currents are obtained with FinFETs realized through a scaled fin pitch process allowing 10-fins/μm layout width at a fin width of 20 nm. We report field effect mobility from multifin split-capacitance-voltage (split-CV) measurements having peak mobility of 3480 $cm^2/V\cdot s$ for a 10-nm QW FinFET with 70% indium. Peak transconductance (g_{mmax}) of 1.62 mS/μm, normalized to circumference, is demonstrated for devices with $L_G = 120$ nm.**

***Index Terms*— III-V, InGaAs, MOSFET, FinFET, sidewall, plasma nitride.**

I. INTRODUCTION

III-V MATERIALS are promising for n-channel field effect transistors (FETs) for low power applications due to their excellent low voltage transport properties, especially high electron injection velocity [1]. In this context $In_xGa_{1-x}As$ channels have received a lot of attention [2] due to the ability to suitably vary the percentage of Indium composition (x) in $In_xGa_{1-x}As$ and span a wide range of bandgap and effective mass. Additionally, the ability to design ultrathin channels confined between buffer layers with optimized band offsets can further enhance their transport properties by tuning the quantum confinement. Scalability to the 7nm or 5nm technology node, which is the likely point of introduction for III-V channels, demands excellent electrostatic integrity which, in turn, necessitates incorporation of III-Vs into multigate device architectures [3], [4].

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In this letter, we systematically explore performance in bulk and quantum well (QW) channel FinFET devices with novel plasma nitride passivated high-k gate stacks. Three different channel architectures are investigated [5], viz. the thick $In_{0.53}Ga_{0.47}As$ channel with body thickness $T_{Body} = 40$nm, the $In_{0.53}Ga_{0.47}As$ QW channel with $T_{Body} = 10$nm and the $In_{0.7}Ga_{0.3}As$ QW channel with $T_{Body} = 10$nm. The above three channel architectures are henceforth referred to as structures A, B and C respectively. All three channels are realized on $In_{0.52}Al_{0.48}As$ buffers on InP substrates. The channels with 53% Indium composition are lattice matched to the buffer and substrate, while the 70% Indium QW channel is compressively strained with respect to the $In_{0.52}Al_{0.48}As$ buffer layer. The structures also incorporate a heavily doped cap layer with a higher Indium percentage sub-cap to facilitate formation of ohmic contacts with low contact resistivity.

II. EXPERIMENT

Epitaxial structures for the device fabrication were grown by IQE Inc. using molecular beam epitaxy (MBE) on 3-in semi-insulating InP substrates. Devices are fabricated by first performing a citric acid/H_2O_2 solution based recess etch of the cap layer to define the gate recess. A well-controlled over etch is included to remove the 2nm InP etch stop layer to allow formation of gate stack directly on the $In_xGa_{1-x}As$ channel. This is followed by the formation of fins within the recessed region. The fin patterns are defined using ZEP electron beam resist. The pattern is first transferred onto an atomic layer deposited (ALD) Al_2O_3 hard mask through a dry etch step. Subsequently, the fin etch is performed using a Cl_2/N_2 plasma based dry etch. Nickel is then directly deposited on the heavily doped cap regions using a lift-off process to form the source/drain ohmic contacts. Subsequently the gate stack is formed by first growing an ultrathin passivation layer using alternating cycles of nitrogen plasma exposure with tri-methyl aluminum (TMA) pre-pulsing [6] followed by thermal ALD growth of 1nm Al_2O_3 and 2.5nm HfO_2 at 250°C. This is followed by thermal evaporation of Nickel and lift-off to form the gate electrode and a forming gas anneal at 350°C for 15 minutes.

All three structures are patterned into FinFET devices with raised source/drain architecture as seen in Fig. 1(a). As shown

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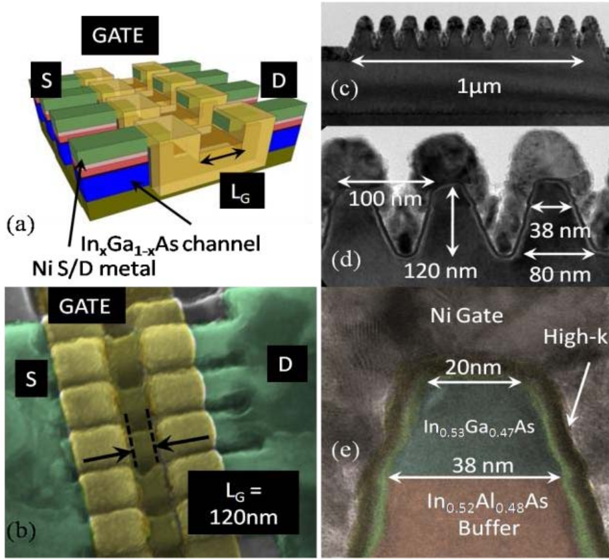

Fig. 1. (a) Schematic of FinFET device. As shown the gate metal forms a slight overlap region with the source/drain metal contacts. (b) False color SEM of the device with 120nm L_G (c) and (d) cross-section TEM of fin structures. (e) Cross-section TEM of single fin from the thick $In_{0.53}Ga_{0.47}As$ channel FinFET device.

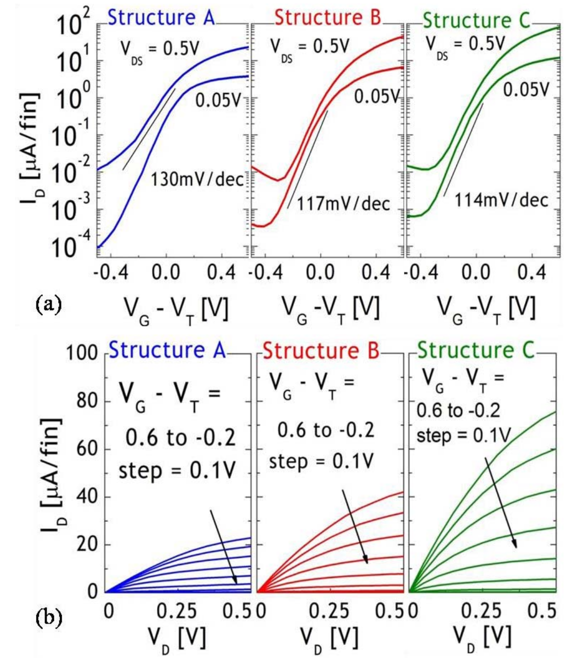

Fig. 2. (a) Transfer characteristics indicating SS_{lin}; (b) output characteristics of short channel FinFETs with $L_G = 120$nm and $W_{fin} = 20$nm.

in Fig. 1(c) and (d), we realize a fin pitch of 100nm allowing 10 fins per μm of layout width. Fig. 1(e) highlights the gate stack comprised of the bi-layer high-κ dielectric and nickel gate metal as well as the active fin region and buffer layers. Fin width of 20nm is realized with a sidewall taper angle of 71°, designed to allow gate metal deposition on the FinFET sidewalls.

III. Result and Discussion

Figs. 2(a) and (b) show the measured transfer and output characteristics respectively for the three short channel FinFET devices with $L_G = 120$nm. The plots shown in blue, red and green correspond to FinFET structure A (thick $In_{0.53}Ga_{0.47}As$), B ($In_{0.53}Ga_{0.47}As$ QW) and C ($In_{0.7}Ga_{0.3}As$ QW) respectively. All three devices show well behaved transfer characteristics with $I_{ON}/I_{OFF} > 10^3$ at $V_{DS} = 0.5$V. Threshold voltage of 0.24V, 0.23V and 0.31V and R_{EXT} of 314 Ω-μm, 276Ω-μm and 283 Ω-μm was measured for FinFET structures A, B and C respectively. An average subthreshold slope of 105mV/dec was obtained for long channel devices (not shown) for both linear (SS_{lin}) and saturation (SS_{Sat}) regions of operation, whereas the average SS_{Sat}, varies between 114-130mV/dec for short channel devices. We measure raw drive current (I_{ON}) of 250, 400 and 760μA for 10-fin devices which translates to 25, 40 and 76 μA/fin for FinFET structures A, B and C respectively, at $V_G - V_T = 0.6$V and $V_{DS} = 0.5$V. DIBL for the QW channels is comparable at 103 mV/V whereas the bulk FinFET shows a DIBL of 200mV/V. This is attributed to conduction through the bottom of the tapered fin which is not electrostatically well controlled.

Field effect mobility is measured from long channel ($L_G = 10\mu$m) FinFET devices as shown in the SEM of Fig. 3(a). The devices comprise of 100 fins in order to

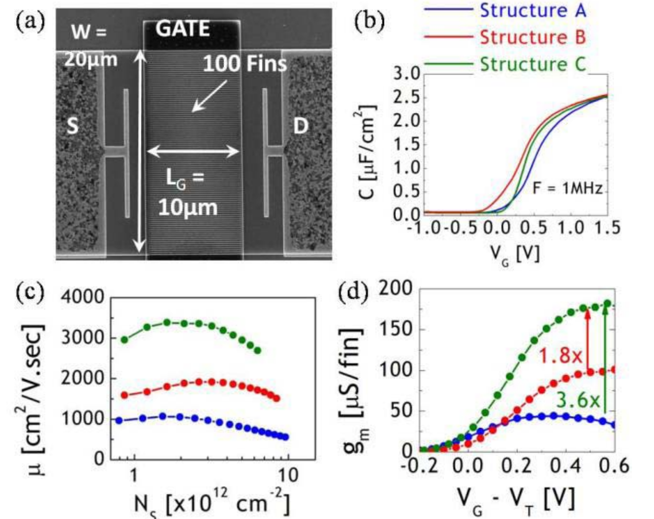

Fig. 3. (a) SEM of long channel FinFET; (b) measured multi-fin split-CV; (c) extracted long channel field effect mobility; (d) transconductance of short channel FinFET devices.

facilitate split-CV measurement of the capacitance. Both capacitance (C) and conductance (G) are measured over a frequency range of 75KHz to 1MHz. We achieve a capacitance equivalent thickness (CET) of 1.1nm for planar MOS capacitors (not shown) and obtain a CET close to 1.4nm for all the FinFET structures. This increase in CET is attributed to a thicker interfacial oxide on the sidewalls of the FinFETs. Fig 3(b) shows the measured capacitance normalized to total circumference, at a frequency of 1MHz for the three substrates. Experimentally extracted field effect mobility is shown in Fig. 3(c). The peak mobility is estimated at 1040, 2085 and 3480 cm^2/Vs for FinFET structures A, B and C respectively. At higher carrier concentration n_s of $5e12cm^{-2}$ the structures

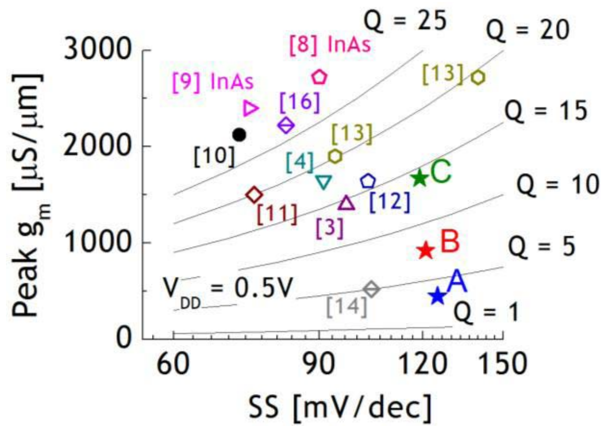

Fig. 4. Benchmarking of devices with published results on III-V planar and multi-gate devices. Q-factor close to 15 is obtained for the $In_{0.7}Ga_{0.3}As$ QW FinFET (structure C) with transconductance of 1.62mS/μm, normalized to circumference of the Fin.

show mobility of 732, 1780 and 3015 cm^2/Vs, respectively. This behavior is commensurate with the increased sidewall roughness scattering at higher gate overdrive where the charge centroid is pulled closer to the sidewall surface. These trends show clearly the relative improvements in mobility for a quantum well channel over the thicker bulk channel. Finally we summarize the transconductance (g_m) for short channel FinFET devices as shown in Fig. 3(d), where the left axis shows the g_m per fin (μS/fin). Normalizing the measured g_m to the gated circumference of the fin ($2H_{Fin} + W_{Fin}$), we report peak g_m of 0.445, 0.92 and 1.62 mS/μm for FinFET structures A, B and C respectively. From the TEM of Fig. 1(e) $W_{Fin} = 20$nm and $H_{Fin} = 45$nm, which is the extent of the gated surface region on the sidewall, resulting in an effective perimeter of 110nm per fin, for all three structures.

Benchmarking the results of this letter using the Q-factor metric as defined by Doornbos et. al. [7], we see that the QW $In_{0.7}Ga_{0.3}As$ FinFETs show among the highest g_m reported for III-V multi-gate (tri-gate, gate all around) devices along with a Q-factor close to 15 as shown in Fig. 4. It is observed however, that planar III-V MOSFETs with higher g_m [8], [9] have been demonstrated for InAs channels with shorter gate lengths. Further improvement in g_{mmax} may be expected for present devices with scaling of L_G indicating significant room for improvement at $V_{DD} = 0.5$V.

Comparison between the three structures shows the enhancement in I_{ON} with increasing indium percentage consistent with lowering the effective mass which significantly enhances transport properties. Additionally, I_{ON} further improves with quantum confinement in the channel as compared to the bulk structure. It has been shown in prior work [15] that compared to planar structures a significant degradation in mobility maybe expected in FinFETs due increased exposure to sidewall roughness scattering. However, by incorporating quantum confined channels, transport maybe improved significantly due to the enhanced volume inversion and simultaneously reduced side wall exposure. Trends observed in this letter are consistent with this observation thereby providing guidance for III-V FinFET channel design towards increasing indium percentage together with quantum confinement.

IV. Conclusion

Experimental benchmarking of three different channel architectures for $In_xGa_{1-x}As$ FinFETs with advanced plasma nitride passivated high-k gate stack and high peak transconductance is demonstrated. Significantly enhanced transport properties are observed for a thin QW $In_{0.7}Ga_{0.3}As$ channel device compared to a thick $In_{0.53}Ga_{0.47}As$ channel architecture. High field effect mobility in excess of 3000 cm^2/V-sec is measured from long channel multi-fin split-CV measurements. We obtain $g_{mmax} = 1.62$mS/μm for QW $In_{0.7}Ga_{0.3}As$ FinFETs at $L_G = 120$nm, which is among the highest g_{mmax} reported for multigate $In_xGa_{1-x}As$ devices.

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