Impact of Varying Indium(x) Concentration and Quantum Confinement on PBTI Reliability in $In_xGa_{1-x}As$ FinFET

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***Abstract*— In this letter, we present a comparative study of positive bias temperature instability (PBTI) reliability in $In_xGa_{1-x}As$ FinFET with varying Indium (x = 0.53, 0.70) percentage and quantization [bulk, quantum well (QW)]. Due to lower effective transport mass and higher injection velocity, $In_{0.7}Ga_{0.3}As$ QW FinFET provides better performance than $In_{0.53}Ga_{0.47}As$ bulk FinFET. However, stronger quantization lowers the effective barrier height between the carriers and defect density in the oxide causing degraded PBTI reliability in the former. Our preliminary PBTI stress study shows that $In_{0.7}Ga_{0.3}As$ QW FinFETs may need to operate at a gate overdrive of 0.1 V (i.e., near threshold operation) to meet 10 years of reliability specifications at 85 °C.**

***Index Terms*— III-V FinFET, positive bias temperature instability (PBTI), quantum well, time to failure (TTF).**

I. Introduction

As CMOS technology explores transistor options for the sub-10nm technology node, III-V materials are considered to be promising alternatives for transistor channel, particularly for nFET applications. Further, at the 22nm technology node and beyond, to achieve good electrostatic integrity, FinFET architectures have already been introduced [1]. Recently, it has been demonstrated that QW FinFET architecture with higher indium (In) mole fraction (x) $In_{0.7}Ga_{0.3}As$ can achieve better performance due to higher injection velocity [2], [3]. With ultra-thin high-κ gate stack on III-V nFETs, Positive Bias Temperature Instability (PBTI) becomes the limiting reliability issue. n-MOSFETs with InGaAs channel and Al_2O_3 gate has been reported to show high PBTI [4], [5]. Furthermore, the impact of quantization due to lower effective mass on PBTI reliability becomes important. In [6], the authors show that, with thinner quantum wells $In_{0.53}Ga_{0.47}As$ MOS-HEMT with Al_2O_3 as gate dielectric shows better electrostatic control but higher PBTI due to quantization effects.

In this letter, we systematically explore the PBTI reliability of three different FinFET architectures with varying Indium (In) percentage and quantization. Fig. 1 shows the three architectures considered namely, (a) $In_{0.53}Ga_{0.47}As$ Bulk FinFET with body thickness, T_{Body}, of 40nm, (b) $In_{0.53}Ga_{0.47}As$ QW FinFET with T_{Body} of 10nm, and (c) $In_{0.7}Ga_{0.3}As$ QW FinFET with T_{Body} of 10nm are as described in [3]. The devices are fabricated integrating a gate stack comprising of 1nm Al_2O_3/ 2.5nm HfO_2 with CET of 1.3nm. Fig. 2 shows the transfer characteristics of these devices at fixed linear threshold voltage, V_{TLin} and gate length, L_G of 1μm. Because of the reduced surface scattering due to volume inversion in QW architecture and increased injection velocity due to higher In percentage, $In_{0.7}Ga_{0.3}As$ QW FinFET show highest performance with 4.3x higher ON current, I_{ON}, at an overdrive of 0.3V and V_{DS} = 0.5V than $In_{0.53}Ga_{0.47}As$ Bulk FinFET.

In this letter, we present a study of PBTI in the three transistor architectures considered. The motivation behind the PBTI investigation in these device architectures is discussed in section II. Further, the characterization details along with the

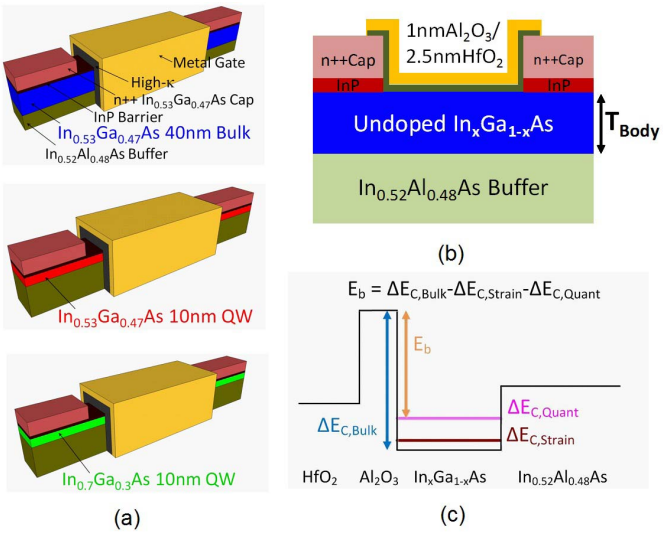

Fig. 1. (a) $In_{0.53}Ga_{0.47}As$ Bulk FinFET with body thickness, T_{Body} = 40nm, $In_{0.53}Ga_{0.47}As$ QW FinFET with T_{Body} = 10nm, and $In_{0.7}Ga_{0.3}As$ QW FinFET T_{Body} = 10nm [3]. (b) Fin cross-section along the source-channel-drain showing n++ cap as S/D, undoped $In_xGa_{1-x}As$ channel and Al_2O_3/HfO_2 gate stack. (c) Effective barrier height (E_b) seen by quantum confined electrons depends both on strain (higher Indium percentage) and on the extent of quantization (assuming first and second sub-band occupation). Reduction in E_b leads to higher rate of electron injection from quantum well into the high-κ gate dielectric and hence lower reliability.

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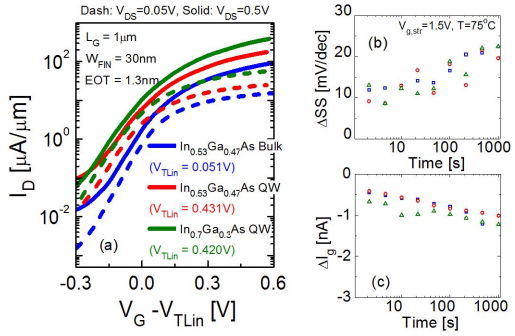

Fig. 2. (a) Transfer characteristics of the three FinFET architectures at gate length, L_G, of 1μm considered in this letter. (b) and (c) shows degradation of SS and gate current, I_g, respectively for $V_{g,str}$ = 1.5V and T = 75 °C for the three architectures.

TABLE I

QUANTIFICATION OF CONDUCTION BAND OFFSETS WITH Al_2O_3 IN THE THREE DEVICE ARCHITECTURES BECAUSE OF BULK, STRAIN AND QUANTIZATION. ALSO, THE EFFECTIVE BARRIER HEIGHTS (E_b) FOR THE THREE CASES ARE MENTIONED

Device	$\Delta E_{C,Bulk}$ [eV]	$\Delta E_{C,Strain}$ [eV]	$\Delta E_{C,Quant}$ [eV]	E_b [eV]
$In_{0.53}Ga_{0.47}As$ Bulk FinFET	3.5	0	0.020	3.48
$In_{0.53}Ga_{0.47}As$ QW FinFET	3.5	0	0.255	3.25
$In_{0.7}Ga_{0.3}As$ QW FinFET	3.675	0.102	0.274	3.29

threshold voltage degradation, ΔV_{Th}, results are presented in this section. In section III, we analyze the PBTI degradation results and extract the voltage and temperature acceleration factors to get the time to failure (TTF) of these devices. Section IV summarizes our key conclusions.

II. PBTI EXPERIMENTAL SETUP

Due to the sub-band formation from quantum confinement, the bulk conduction band height ($\Delta E_{C,bulk}$) decreases by $\Delta E_{C,Quant}$, assuming the conduction band is occupied by carriers till the second sub-band in the $In_{0.7}Ga_{0.3}As$ FinFETs, particularly at high stress voltages and temperatures. Moreover, lattice mismatch between the $In_{0.52}Al_{0.48}As$ buffer layer (lattice constant, a_{subs} = 5.869Å) and the $In_{0.7}Ga_{0.3}As$ QW (lattice constant, a_{QW} = 5.937Å) creates 1% compressive strain (ϵ_{ll}) in the QW channel [7]. This strain causes an increase in the band gap, E_g by $\Delta E_{C,Strain}$. Both these effects reduce the effective barrier height at the high-κ/channel interface (E_b) in these devices (fig. 1(c)). Table I summarizes these conduction band offset components for all the three architectures. This reduction in E_b will impact reliability of the devices.

To study the effect of higher indium (In) percentage and quantization on PBTI reliability, we stress the devices at higher gate voltages and temperatures and periodically halt to measure the DC IV characteristics to record the parametric shift using 300ms of measurement time in Keithley's Model 4200-SCS. Peak transconductance method is used to extract

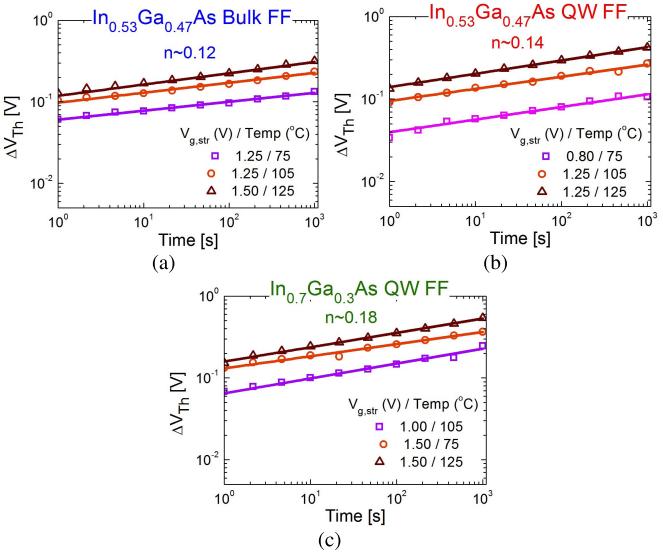

Fig. 3. Time evolution of ΔV_{Th} under PBTI stress of different stress voltage, $V_{g,str}$ and temperature, T for (a) $In_{0.53}Ga_{0.47}As$ Bulk, (b) $In_{0.53}Ga_{0.47}As$ QW, and (c) $In_{0.7}Ga_{0.3}As$ QW FinFET devices, respectively. Using power law fitting based on eq.(1), the time exponent (n) of each curve is extracted. The value of n for $In_{0.53}Ga_{0.47}As$ Bulk architecture is the lowest.

the threshold voltage, V_{Th}, of the devices. Fig. 3 plots the time evolution of the threshold voltage shift, ΔV_{Th}, under PBTI stress for different stress voltages, $V_{g,str}$, and temperatures, T, for the three FinFET architectures. Eq. (1) below shows the ΔV_{Th} dependence on stress time, t, stress voltage, $V_{g,str}$ and temperature, T where A, n, Γ and E_A are the prefactor, the time exponent, the voltage acceleration factor, and the activation energy, respectively.

$$\Delta V_{Th} = A * t^n * V_{g,str}^{\Gamma} * exp(-\frac{E_A}{kT}) \quad (1)$$

Lines in fig. 3 are mathematical fits with power law dependence giving the prefactor, A, and time exponent, n, at a particular $V_{g,str}$ and T. The values of A are 0.118, 0.134, 0.159 and n are 0.12, 0.14, 0.18 for $In_{0.53}Ga_{0.47}As$ Bulk, $In_{0.53}Ga_{0.47}As$ QW, and $In_{0.7}Ga_{0.3}As$ QW at $V_{g,str}$ of 1.5V and T = 125 °C, respectively. Highest prefactor, A, and time exponent, n, of $In_{0.7}Ga_{0.3}As$ QW FinFET among the three devices indicates lower PBTI reliability lifetime. In the next section, we discuss the PBTI results and compare the extracted acceleration factors for the three architectures.

III. RESULTS AND DISCUSSION

Fig. 4 plots the normalized transconductance degradation, $\Delta g_m/g_{m0}$ vs ΔV_{Th} for $V_{g,str}$ = 1.0V and T = 125 °C where g_{m0} is the peak g_m without any stress applied. We observe g_m shifts with PBTI stress in $In_{0.7}Ga_{0.3}As$ devices in conjunction with V_{Th} shifts which is contrary to high-κ/metal gate Si MOSFETs where PBTI stress has negligible or no impact on Δg_m [8]. This observed effect of transconductance change in $In_{0.7}Ga_{0.3}As$ devices needs further exploration in the future.

Fig. 5 (a) and (b) plot the voltage acceleration, Γ and the temperature activation, E_A dependence of ΔV_{Th} on $V_{g,str}$ and T respectively using power law fitting and exponential fitting for the three architectures.

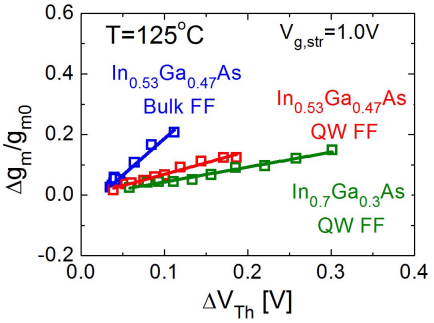

Fig. 4. Plot of $\Delta g_m/g_{m0}$ with respect to ΔV_{Th} for $V_{g,str} = 1.0V$ at 125 °C.

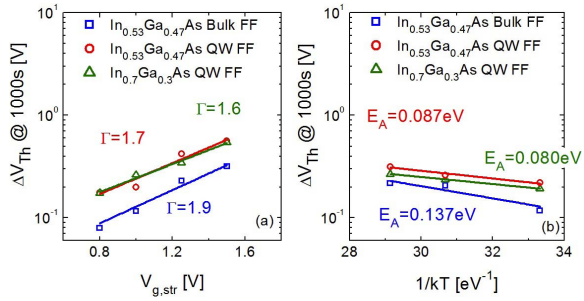

Fig. 5. (a) Plot of ΔV_{Th} with respect to $\Delta V_{g,str}$ to extract the voltage acceleration factor (Γ) for the three architectures. (b) Plot of temperature activation of ΔV_{Th} for the three architectures. The exponential fit gives us the activation energy, E_A values which are in accordance with the barrier height lowering due to quantization (fig. 1(c)).

Threshold voltage degradation, ΔV_{Th}, in fig. 5 is extracted after 1000s of stress time. While the absolute values of extracted n, Γ and E_A may depend on the exact recovery behavior due to the slow measurements used in this letter, but their relative difference among the three device architectures and the conclusions derived are likely to be independent of the same.

Lower activation energy, E_A, of QW devices correlates well with the effective barrier height, E_b, reduction (fig. 1(c)). Moreover, it is shown in [6] that the defect density distribution in Al_2O_3 is centered slightly above the conduction band and with reducing quantum well thickness, the barrier offset between the conduction band and the center of the defect density distribution ($\Delta E_{CB-Defect}$) reduces. This reduction in the defect barrier offset, $\Delta E_{CB-Defect}$, degrades PBTI for $In_{0.7}Ga_{0.3}As$ QW FinFET.

Using the n, Γ, and E_A values, we can predict the time to failure (TTF) of these devices at the operating conditions. Assuming the operating temperature of III-V devices to be 85 °C, and a maximum ΔV_{Th} of 60mV, the TTF with respect to V_G-V_T of these devices are given in fig. 6. Fig. 6 also benchmarks the time to failure (TTF) of the devices in this letter with Al_2O_3/$In_{0.53}Ga_{0.47}As$ MOS-HEMTs [6] and Hf-based high-κ/Si MOS/FinFETs [9]. Fig. 6 also shows a more stringent TTF at ΔV_{Th} of 30mV (dash). Extrapolated time to 60mV V_{Th} shift at 85 °C operating temperature show that, the lifetime operation of 10 years would be ensured if $In_{0.53}Ga_{0.47}As$ Bulk, $In_{0.53}Ga_{0.47}As$ QW and $In_{0.7}Ga_{0.3}As$ QW FinFETs are operated at overdrive voltages of 0.30V, 0.18V and 0.10V, respectively. 0.10V of overdrive

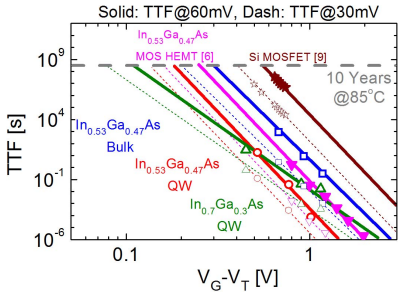

Fig. 6. Extrapolated times to 60mV ΔV_{Th} (solid) at 85 °C operating temperature show that $In_{0.7}Ga_{0.3}As$ QW FinFET needs to operate at 0.1V of overdrive for 10 years of lifetime operation. The dashed lines are extrapolation of time to failure (TTF) at a more stringent ΔV_{Th} of 30mV.

represents near threshold operation for $In_{0.7}Ga_{0.3}As$ QW FinFET. In order to take advantage of the high performance of III-V FinFETs in the future technology nodes, we need to improve PBTI reliability by developing a higher quality high-κ dielectric with shallower defect densities such that the defect barrier offset, $\Delta E_{CB-Defect}$, is high.

IV. Conclusion

In this letter, we investigated the PBTI reliability of three different III-V FinFET architectures with varying In percentage and quantization, namely, $In_{0.53}Ga_{0.47}As$ Bulk, $In_{0.53}Ga_{0.47}As$ QW, and $In_{0.7}Ga_{0.3}As$ QW FinFET. Highest performance is achieved with $In_{0.7}Ga_{0.3}As$ QW FinFET. However, there exists a tradeoff between performance and the PBTI reliability due to lowering of the barrier offset between the carriers and defect density in the oxide because of quantum confinement. To meet 10 years of operating lifetime for $In_{0.7}Ga_{0.3}As$ QW FinFET, the devices may need to operate at an overdrive of 0.10V i.e. near threshold. The need of high-κ oxide with shallower defect densities is crucial to improve PBTI reliability in III-V FinFETs.

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