Impact of Variation in Nanoscale Silicon and Non-Silicon FinFETs and Tunnel FETs on Device and SRAM Performance

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(*Invited Paper*)

***Abstract*— One of the key challenges in scaling beyond 10-nm technology node is device-to-device variation. Variation in device performance, mainly threshold voltage, V_T, inhibits V_{CC} scaling. In this paper, we present a comprehensive study of process variations and sidewall roughness (SWR) effects in silicon (Si) bulk n-/p-FinFETs, $In_{0.53}Ga_{0.47}As$ bulk n-FinFETs, germanium (Ge) bulk p-FinFETs, and gallium antimonide–indium arsenide (GaSb–InAs) staggered-gap heterojunction n-/p-tunnel FETs (HTFETs) using 3-D Technology Computer Aided Design numerical simulations. According to the sensitivity study, FinFET and tunnel FET (TFET) device parameters are highly susceptible to fin width, W_{FIN}, and ultrathin body thickness, T_b, variations, respectively. TFETs show higher variation in device performance than FinFETs. A Monte Carlo study of SWR variation on n- and p-FinFETs shows higher $3\sigma(V_{T\,Lin})$ of $In_{0.53}Ga_{0.47}As$ bulk n- and Ge bulk p-FinFETs than their Si counterparts. Furthermore, to study the variation impact on memory circuits, we simulate 6T and 10T static random access memory (SRAM) cells with FinFETs and HTFETs, respectively. The probability distribution of read failure in SRAM cells at different supply voltages, V_{CC}, shows that HTFETs require 10T SRAM cell architecture and less than 4% variation in T_b for their V_{CCmin} to approach 200 mV.**

***Index Terms*— III-V compound semiconductors, FinFET, heterojunction tunnel FET (HTFET), line edge/width roughness (LER/LWR), Schmitt–Trigger (ST2) static random access memory (SRAM), sidewall roughness (SWR), surface roughness (SR).**

I. Introduction

TRANSISTOR scaling has been the driving factor for the CMOS industry. It has resulted in providing superior performance as well as lowering dynamic power dissipation and, at the same time, enabled reduction in the cost per function. With the limitations in scaling planar bulk MOSFETs beyond the 32-nm technology node due to worsening short-channel effects (SCEs) and ever-increasing channel doping concentration, FinFETs were introduced in high volume manufacturing at the 22-nm technology node [1]. The improved electrostatic integrity of FinFETs not only mitigates the performance degradation due to SCEs but also leads to performance enhancement and improved variation due to reduction in channel doping concentration [2]. There is considerable effort in extending the life of FinFETs to sub-10-nm technology nodes by replacing the silicon (Si) channel with high-carrier-mobility materials like $In_xGa_{1-x}As$ (for nMOS) [3]–[6] and strained germanium (Ge) (for pMOS) [7]–[11]. Beyond non-Si FinFETs, heterojunction tunnel FETs (HTFETs) in the mixed arsenide–antimonide materials system with their promising sub-kT/q steep subthreshold behavior can outperform CMOS in terms of both dc and RF performances, particularly at lower supply voltages below 0.3 V [12], [13]. While there is a reasonable consensus in the community that aggressive supply voltage, V_{CC}, scaling while maintaining high transistor performance is achievable with these new transistor architectures and alternate materials as channel [14], it is critical that we conduct a detailed comparative study of the effect of process variations in these future device candidates and their impact on device and static random access memory (SRAM) performances.

Scaling reduces the feature sizes of the transistors but, in general, make the device parameters more sensitive to process variations. In comparison with planar MOSFETs, FinFETs and HTFETs have additional sources of variation such as fin width, (W_{FIN}), fin sidewall roughness (SWR), and fin height (H_{FIN}) in the case of FinFET or ultrathin body thickness (T_b) in the case of tunnel FET (TFET). In this paper, we consider the process-induced variation of W_{FIN}, T_b, gate length (L_G), and gate–source (gate–drain) overlap (underlap) lengths (L_{Ov_Un}) for sensitivity to ON-current (I_{ON}) and linear threshold voltage (V_{TLin}). Furthermore, line edge roughness (LER) or SWR is another additional factor contributing to parametric variation [15], [16]. At future scaled nodes, the critical dimensions of the transistors are expected to become comparable with the SWR or LER parameters, i.e., the root mean square (rms) amplitude (Δ) and correlation length (Λ) that do not necessarily scale with technology, leading to higher

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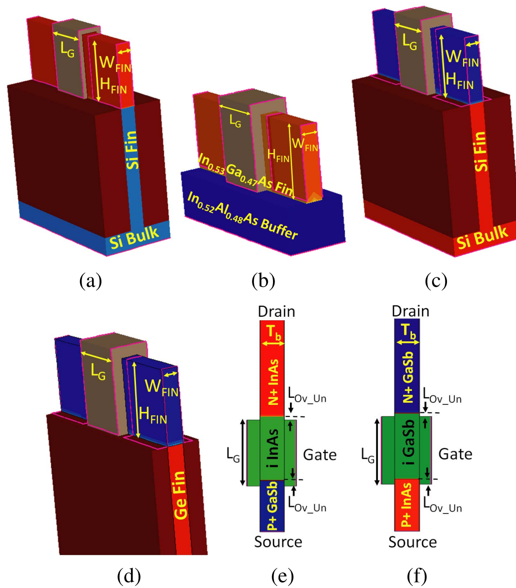

Fig. 1. 3-D TCAD schematic structures for (a) Si bulk n-FinFET, (b) $In_{0.53}Ga_{0.47}As$ bulk n-FinFET, (c) Si bulk p-FinFET, (d) Ge bulk p-FinFET, and 2-D TCAD schematic structures for (e) GaSb-InAs n-HTFET, and (f) InAs-GaSb p-HTFET used in this paper.

fluctuations of electrical parameters of the devices. In this paper, we study the effect of SWR by incorporating random roughness on the sidewall of FinFETs using a 1-D Fourier transform of Gaussian autocorrelation function as presented in [15]. Using Technology Computer Aided Design (TCAD), we then extract the statistical distribution of threshold voltage (V_{Th}) for the FinFETs considered in this paper. Random-dopant fluctuation (RDF) arising from channel dopants has also been a variation concern for transistors [17]–[19]. However, in this paper, we assume the channel region to be nominally undoped, thereby resulting in a very low RDF effect on these devices.

In this paper, we present a comprehensive study of process variation using 3-D numerical simulations in nMOS and pMOS FinFETs and HTFETs with Si (n- and p-FinFETs), $In_{0.53}Ga_{0.47}As$ (n-FinFET), InAs (n-HTFET), Ge (p-FinFET), and GaSb (p-HTFET) as channel materials. The impact of statistical variation on memory circuits is studied using 6T SRAM cells for FinFETs and Schmitt–Trigger (ST2) 10T SRAM cells for HTFETs [20]. Along with the bulk Si FinFET, we have also considered 6T SRAM cells with $In_{0.53}Ga_{0.47}As$ FinFET as nMOS and Ge FinFET as pMOS. Section II provides the details about the calibration of the simulation setup and the nominal device characteristics, which provides the foundation for the variation study. Section III deals with the nMOS and pMOS variation study that includes the sensitivity analysis with W_{FIN}, L_G and $L_{\mathrm{Ov_Un}}$ variation in FinFETs and HTFETs, and also the SWR statistical analysis of FinFETs. Section IV discusses the effects of statistical variation of W_{FIN} (in FinFETs) and T_b (in HTFETs) on read static noise margin (RSNM) of SRAM cells. We then conclude this paper in Section V.

II. Simulation Setup

Fig. 1(a)–(d) shows the schematic of the 3-D device architectures considered in this paper, namely, Si bulk n-FinFET,

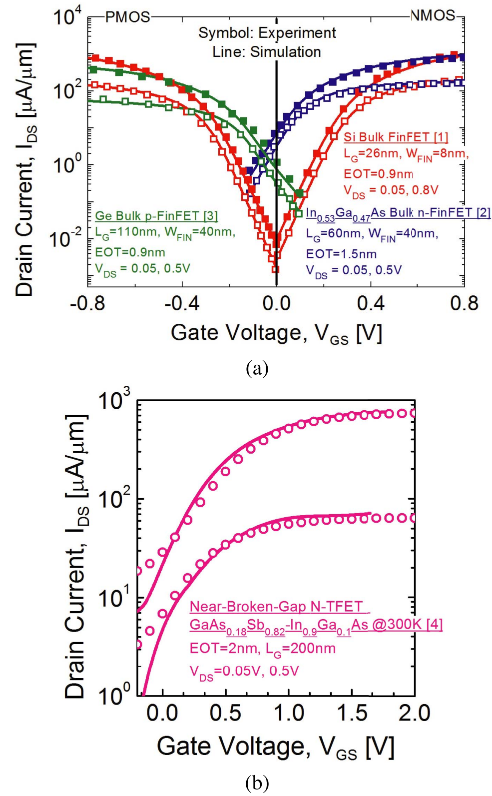

Fig. 2. 3-D and 2-D TCAD calibration of transfer characteristics of simulation with the experimental data of (a) FinFETs [1], [3], [7] and (b) HTFETs [12], respectively. The simulation models for FinFETs include field-dependent mobility models while for HTFETs BTBT model and density gradient model for quantum correction in both.

$In_{0.53}Ga_{0.47}As$ bulk n-FinFET, Si bulk p-FinFET, Ge bulk p-FinFET, respectively, while 2-D device architectures for HTFETs are shown in Fig. 1(e) and (f) as gallium antimonide–indium arsenide (GaSb–InAs) n-HTFET and InAs–GaSb p-HTFET, respectively. These 3-D FinFET and 2-D HTFET structures are studied using numerical drift–diffusion simulations with density gradient model for quantum correction in Sentaurus TCAD [21]. The simulation models for FinFETs are calibrated to the experimental data of Si n- and p-FinFET [1], $In_{0.53}Ga_{0.47}As$ bulk n-FinFET [3], and Ge bulk p-FinFET [7], as shown in Fig. 2(a). The calibrated mobility models for these structures include bulk mobility (μ_{bulk}), surface contribution due to acoustic phonon scattering (μ_{ac}), surface roughness scattering (μ_{sr}), and high field saturation-dependent Caughey–Thomas model (μ_{hf}) [22], which are combined using the Matthiessens rule [23] as follows:

$$\frac{1}{\mu} = \frac{1}{\mu_{\mathrm{bulk}}} + \frac{1}{\mu_{\mathrm{ac}}} + \frac{1}{\mu_{\mathrm{sr}}} + \frac{1}{\mu_{\mathrm{hf}}}. \quad (1)$$

In (1), $\mu_{ac} = (B/E)+(C/E^{1/3})$, $\mu_{\mathrm{sr}} = [(E^2/\delta)+(E^3/\eta)]^{-1}$ and $\mu_{hf} = \mu_{\mathrm{bulk}}/(1+(\mu_{\mathrm{bulk}} * E_{hf}/v_{\mathrm{sat}})^{\beta})^{1/\beta}$, where E is the transverse electric field normal to the channel while E_{hf} is the longitudinal electric field along the channel from source to the drain.

We validate our TCAD simulation models for HTFETs with the state-of-the-art $GaAs_{0.18}Sb_{0.82}$-$In_{0.9}Ga_{0.1}As$ n-HTFET

TABLE I
SUMMARY OF PHYSICAL AND CALIBRATION PARAMETERS OF ALL THE DEVICE ARCHITECTURES USED IN THIS PAPER

Parameters	Si Bulk n-/p- FinFET	$In_{0.53}Ga_{0.47}As$ Bulk FinFET	Ge Bulk FinFET	Heterojunction n- TFET ($GaAs_{0.18}Sb_{0.82}/In_{0.9}Ga_{0.1}As$)
		Physical Parameters		
L_G [nm]	26	60	110	200
W_{FIN}/T_b [nm]	8	40	40	350
EOT [nm]	0.9	1.5	0.9	2
H_{FIN} [nm]	34	30	30	-
N_{SD} [cm^{-3}]	$1x10^{20}$	$1x10^{19}$	$1x10^{20}$	$5x10^{19}$
N_{ch} [cm^{-3}]	$1x10^{16}$	$1x10^{14}$	$1x10^{17}$	-
		Calibration Parameters		
μ_{bulk} [cm^2/V-s]	190/160	1300	300	$2x10^4/1x10^4$
B [cm/s]	$1x10^7/1x10^7$	$4x10^7$	$8x10^7$	-
C [cm$^{5/3}$/V$^{2/3}$s]	$1x10^7/3x10^3$	$6x10^2$	$8x10^7$	-
δ [V/s]	$1x10^{14}/2x10^{14}$	$6x10^{14}$	$1x10^{10}$	-
η [V$_2$/cm-s]	$1x10^{30}/2x10^{30}$	$6x10^{33}$	$2x10^{30}$	-
β []	1.5/1.5	1.2	2	2/2
v_{sat} [cm/s]	$1.5x10^7/1.6x10^7$	$4.5x10^7$	$6.2x10^7$	$5x10^7/5x10^7$
APath1 [1/cm^3/s]	-	-	-	$1.62x10^{20}/1.73x10^{20}$
BPath1 [V/cm]	-	-	-	$5.92x10^{06}/1.90x10^{06}$
RPath1 []	-	-	-	1.1462/1
E_g [eV]	1.12	0.74	0.744	0.69/0.42

data in [12], as shown in Fig. 2(b). Transport in TFET is defined by the dynamic nonlocal band-to-band tunneling (BTBT) from source–gate junction. The recombination rate in this model is given by the following:

$$R_{\text{net}} = A\text{Path1}\left(\frac{F}{F_0}\right)^P \exp\left(\frac{B\text{Path1}}{F}\right). \quad (2)$$

In (2), F is the field in the tunneling region, $F_0 = 1$ V/cm and $P = 2$ for direct tunneling process while $P = 2.5$ for phonon-assisted tunneling process. The calibrated values of the parameters APath1 and BPath1 and the ratio of effective masses m_v/m_c, defined as RPath1 are given in Table I. The dynamic nonlocal BTBT model in TCAD is critical to determine the realistic subthreshold slope (SS) and ON-current (I_{ON}) performance in TFETs. The calibrated effective barrier height (E_{beff}) for $GaAs_{0.18}Sb_{0.82}$-source and $In_{0.9}Ga_{0.1}As$-channel is taken as 0.03 eV. The midbandgap interface states (D_{IT}) is taken as 5×10^{12} cm^{-2} corresponding to the experiment data. All physical and calibrated parameters considered for FinFET and HTFET devices of Fig. 2 are summarized in Table I.

Using the calibrated mobility models, we scale the device architectures to the 22-nm technology node to achieve the transistor characteristics of the six devices illustrated in Fig. 1. The transfer characteristics of nominal FinFETs with L_G of 26 nm, W_{FIN} of 8 nm, and equivalent oxide thickness (EOT) of 0.9 nm are shown in Fig. 3(a). We adjust the work function of these nominal FinFETs such that the I_{OFF} for each is 100 nA/μm. To normalize the raw current per fin of the simulated devices, we assume a layout density of 10 fins per μm [5]. $In_{0.53}Ga_{0.47}As$ n-FinFET shows higher ON-current performance at $V_{CC} = 0.5$ V and better short-channel control than their Si counterpart because of the high electron injection velocity, v_{inj} and larger effective channel length, L_{Eff}, respectively [16], [24].

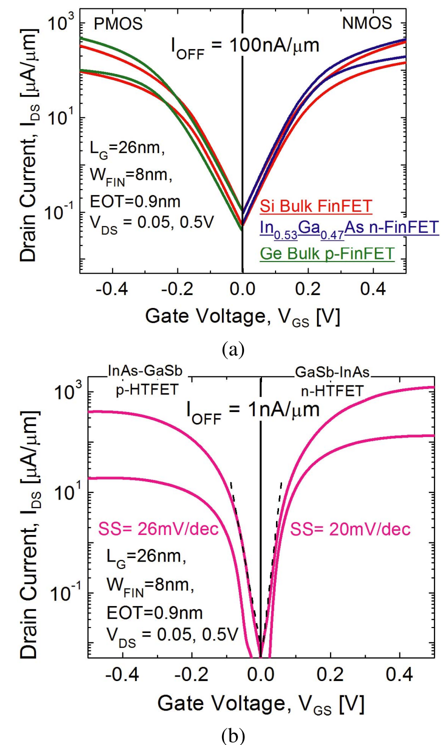

Fig. 3. Transfer characteristics of the nominal (a) FinFETs and (b) HTFET devices used for the variation study in this paper. FinFETs and HTFETs are work function adjusted to achieve 100 and 1 nA/μm of OFF-current, respectively.

Moreover, the higher ON-current performance of Ge p-FinFET compared with Si is attributed to the higher hole mobility in the former.

According to [25] and [26], to achieve the steep SS in a short-channel TFET, a more aggressive (e.g., EOT or body thickness, T_b) scaling for TFETs than that specified in

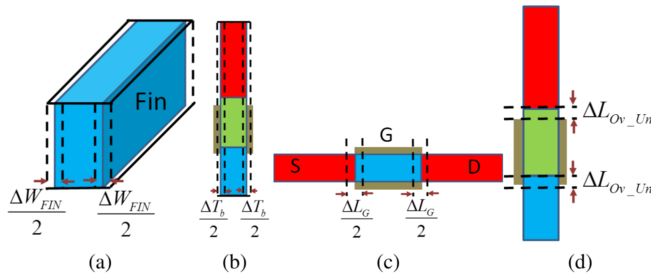

Fig. 4. Schematic of uniform process variations of (a) fin width of FinFET, ΔW_{FIN}, (b) ultrathin body thickness of TFET, ΔT_b, (c) gate length, ΔL_G, and (d) gate–source (gate–drain) overlap (underlap), $\Delta L_{\mathrm{Ov_Un}}$ considered in this paper.

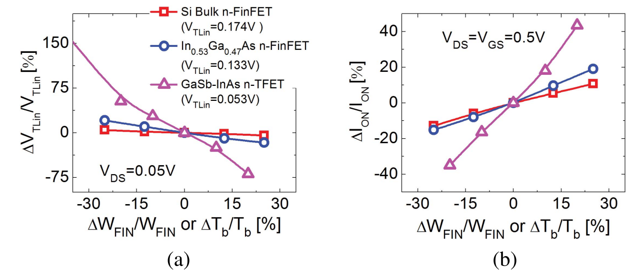

Fig. 5. Sensitivity analysis of (a) $V_{T\mathrm{Lin}}$ and (b) I_{ON} of nMOS FinFETs and HTFET show W_{FIN} (nominal $W_{\mathrm{FIN}} = 8$ nm) or T_b (nominal $T_b = 5$ nm) as the primary source of variation.

the International Technology Roadmap for Semiconductors node for MOSFETs [14] is required to maintain equivalent SCE performance and lower the drain-induced barrier thinning effect. Moreover, the direct tunneling leakage between the channel and the drain is also a primary factor for SS degradation and high OFF-state leakage in an extremely scaled double-gate TFET. Hence, an underlap of the gate-edge/drain region is required to suppress the ambipolar leakage in narrow gap channel HTFET. Therefore, we simulate GaAs–InAs n- and InAs–GaSb p-HTFETs having L_G of 26 nm, ultrathin body, T_b, of 5 nm, and EOT of 0.9 nm in pursuit of the improvement in the device electrostatics and the source/channel tunnel junction design. Fig. 3(b) shows the transfer characteristics of nominal n- and p-HTFETs with gate electrode work function adjusted to achieve I_{OFF} of 1 nA/μm. The material parameters used in the 22-nm node ultrathin body HTFET are taken from [25], which have been previously calibrated using the atomistic simulations in [27]. TFETs are also known to exhibit enhanced Miller capacitance effect [28] and the delayed saturation characteristics [29], which strongly impact the TFET circuit performance.

III. Device Variation Study

The aggressive scaling requirements of Si and non-Si FinFETs and HTFETs for advanced nodes leave them highly prone to process variations. This section shows a quantitative study of the effect of major process variation sources on FinFET and HTFET performance. The sources of variation considered here include the fin width of FinFET, ΔW_{FIN}, the ultrathin body thickness of HTFET, ΔT_b, the gate length, ΔL_G, and the gate–source (gate–drain) overlap (underlap) lengths, and $\Delta L_{\mathrm{Ov_Un}}$ (assuming the work function variation is well controlled during process integration using grain boundary free ultrathin amorphous metal layers), as shown in Fig. 4. Since the nominal T_b of HTFETs are more aggressively scaled to 5 nm than the nominal $W_{\mathrm{FIN}} = 8$ nm of FinFETs, a fair variation comparison between HTFET and FinFET would be in percentage variation of ΔW_{FIN} and ΔT_b, as shown in Fig. 5.

A. n-Channel FinFET and HTFET Variations

Fig. 5 shows the extracted linear threshold voltage, $V_{T\mathrm{Lin}}$, and ON-current, I_{ON}, percentage variation for $\Delta W_{\mathrm{FIN}}/W_{\mathrm{FIN}}$ of the nominal n-channel FinFET and $\Delta T_b/T_b$ HTFET devices. The device performance changes due to other two sources of variations, namely, ΔL_G and $\Delta L_{\mathrm{Ov_Un}}$, are not shown here because they have less than 1% of $V_{T\mathrm{Lin}}$ variation. The linear threshold voltage, $V_{T\mathrm{Lin}}$, for each device is extracted using the constant current method with the drain current, I_{DS}, set to a fixed value of 0.1 μA/μm at $V_{\mathrm{DS}} = 0.05$ V, while the I_{ON} is defined as I_{DS} at $V_{\mathrm{GS}} = V_{\mathrm{DS}} = 0.5$ V.

The gate electrostatic field from the three sides in FinFETs as well as the ultrathin body thickness of the fin causes quantum confinement of carriers that leads to splitting of the bands into sub-bands. The inverse dependence of sub-band splitting on $(W_{\mathrm{FIN}})^2$ makes the FinFETs highly sensitive to W_{FIN} variation. Similarly, in HTFETs, the quantum confinement due to aggressively scaled T_b changes the effective bandgap at the source–gate junction affecting the tunneling barrier width and height. Moreover, the low electron effective mass, m_{eff}, in the III-V semiconductors compared with the Si lead to higher quantum confinement, due to its inverse dependence to m_{eff}, with tighter fin widths in the former. These are the reasons why the W_{FIN} or T_b variations dominantly affect the device performance of FinFETs and TFETs among the three sources of variation considered in this paper. Furthermore, because the TFET tunneling transport is exponentially proportional to the bandgap variation, it shows higher sensitivity to T_b variation than what FinFET shows to W_{FIN} variation.

Another leading source of variation in FinFETs is the SWR. The critical dimension of W_{FIN} in today's devices ($W_{\mathrm{FIN}} = 8$ nm) is approaching the state-of-the-art SWR parameters ($\Delta = 0.5 - 3$ nm and $\Lambda = 20$ nm) [15]. It is, therefore, very crucial to quantify the 3σ of V_T variation in FinFETs due to the SWR. In this paper, we present a Monte Carlo implementation of SWR in FinFETs using 1-D Fourier synthesis of Gaussian autocorrelation function, as shown in Fig. 6 [30]. An ensemble of 100 variant 3-D devices having SWR with rms amplitude, $\Delta = 1$, 2, and 3 nm and correlation length, $\Lambda = 20$ nm is simulated using TCAD to study the statistical performance variation. The histogram plots of $V_{T\mathrm{Lin}}$ variation at $V_{\mathrm{DS}} = 0.05$ V due to SWR in Si bulk n-FinFET and $\mathrm{In_{0.53}Ga_{0.47}As}$ bulk n-FinFET are shown in Fig. 7. With increasing SWR rms amplitude (Δ), the 3σ of $V_{T\mathrm{Lin}}$ variation increases for both Si and $\mathrm{In_{0.53}Ga_{0.47}As}$ bulk n-FinFET. Higher $3\sigma(V_{T\mathrm{Lin}})$ of $\mathrm{In_{0.53}Ga_{0.47}As}$ bulk n-FinFET than Si is because of the lower m_{eff} and higher quantization effect in the former. Furthermore, the mean value of $V_{T\mathrm{Lin}}$ variation reduces with increasing SWR rms amplitude (Δ).

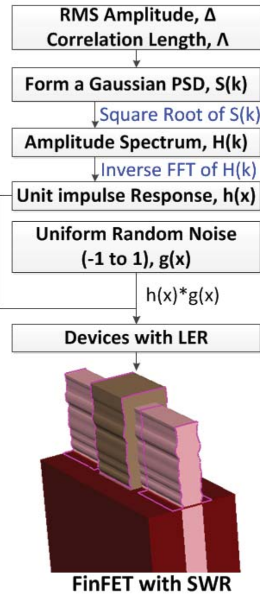

Fig. 6. Implementation of SWR into 3-D device simulations [30].

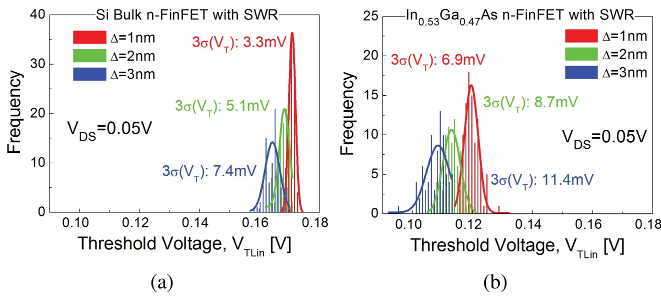

Fig. 7. Histogram plots of $V_{T\mathrm{Lin}}$ of (a) Si bulk and (b) $\mathrm{In}_{0.53}\mathrm{Ga}_{0.47}\mathrm{As}$ bulk n-FinFETs with 1-, 2-, and 3-nm rms amplitude (Δ) of SWR variation. $\mathrm{In}_{0.53}\mathrm{Ga}_{0.47}\mathrm{As}$ bulk n-FinFET shows higher 3σ of $V_{T\mathrm{Lin}}$ than Si owing to the lower electron effective mass in the former system.

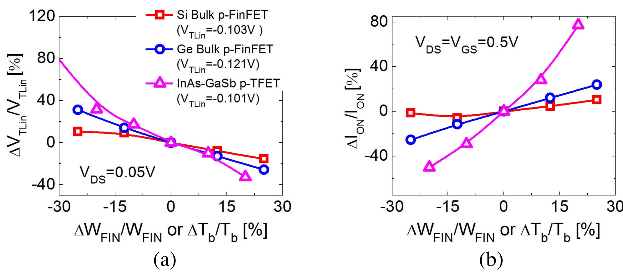

Fig. 8. Sensitivity analysis of (a) $V_{T\mathrm{Lin}}$ and (b) I_{ON} of NMOS FinFETs and HTFET show W_{FIN} (nominal $W_{\mathrm{FIN}} = 8$ nm) or T_b (nominal $T_b = 5$ nm) as the primary source of variation.

B. p-Channel FinFET and HTFET Variations

Similar to the n-channel device variation, we perform the sensitivity study for p-channel FinFET and HTFET devices considered in this paper. Among the three sources of variation, namely, W_{FIN} or T_b, L_G, and $L_{\mathrm{Ov_Un}}$, p-channel devices also show highest sensitivity to W_{FIN} and T_b variation for FinFETs and HTFETs, respectively, because of the quantum confinement effect. Fig. 8 shows the $V_{T\mathrm{Lin}}$ and I_{ON} variation with respect to the nominal devices for W_{FIN} or T_b variation in p-channel devices.

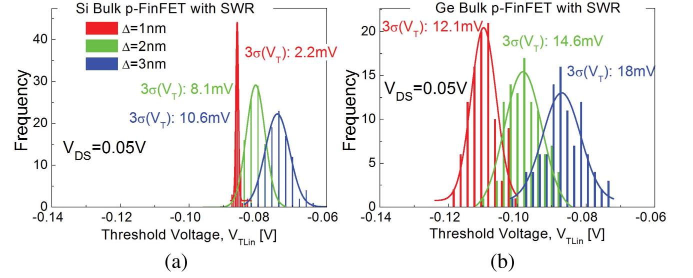

Fig. 9. Histogram plots of $V_{T\mathrm{Lin}}$ of (a) Si bulk and (b) Ge bulk p-FinFETs with 1-, 2-, and 3-nm rms amplitude (Δ) of SWR variation. Ge bulk p-FinFET shows higher 3σ of $V_{T\mathrm{Lin}}$ than Si owing to the lower electron effective mass in the former system.

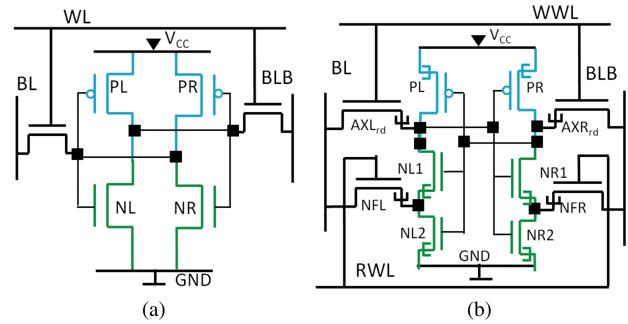

Fig. 10. Schematic of the SRAM cells with (a) 6T configuration having FinFETs and (b) 10T ST2 configuration having HTFETs [20].

An ensemble of 100 variant 3-D devices with SWR of $\Delta = 1$, 2, and 3 nm and correlation length, $\Lambda = 20$ nm are simulated for Si and Ge bulk p-FinFETs. Fig. 9 shows the histogram of $V_{T\mathrm{Lin}}$ variation at $V_{\mathrm{DS}} = 0.05$ V. With increasing SWR rms amplitude (Δ), the 3σ of $V_{T\mathrm{Lin}}$ variation increases for both Si and Ge bulk p-FinFET. The mean value of $V_{T\mathrm{Lin}}$ variation reduces with increasing SWR rms amplitude just like the n-channel counterparts.

The impact of W_{FIN} or T_b process variations on memory circuit performance is studied in the following section using SRAM cell configurations.

IV. SRAM Variation Analysis

To achieve robust circuit performance, it is important to study the impact of process variation on circuits for both high performance and power efficient electronic application with highly scaled near-threshold/subthreshold CMOS transistors. In this paper, to see the impact of variation (namely, W_{FIN} or T_b) on memory circuits, we simulate 6T SRAM cells for FinFETs and 10T ST2 SRAM cells for HTFETs. A 10T-based SRAM design with feedback is required for HTFETs to achieve a comparable RSNM at low supply voltages similar to subthreshold CMOS [20]. The schematics of the above-mentioned SRAM cells are shown in Fig. 10. The transistor sizing of SRAM cells in this paper are used as following the guidelines established in [20].

For 22-nm technology node, the targeted SRAM transistors have an L_G of 34 nm with 10 nA/μm as I_{OFF} [1]. We generate the nominal SRAM-target FinFETs and HTFETs using the

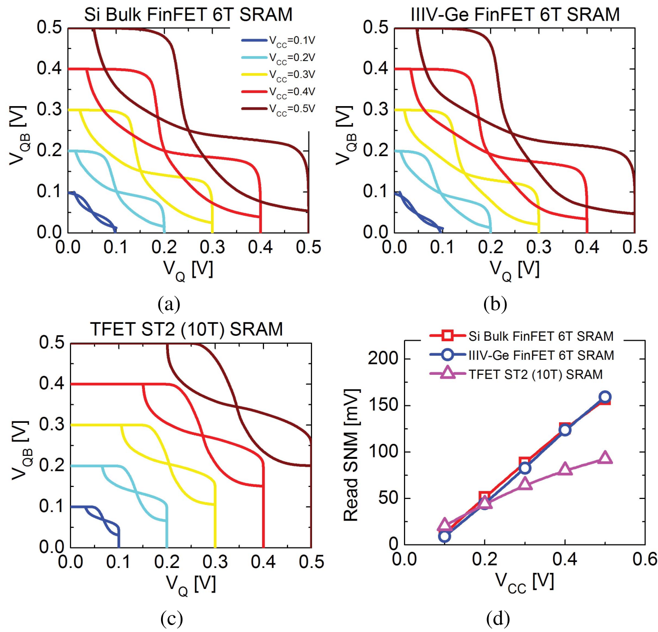

Fig. 11. SRAM butterfly curves as different supply voltages, V_{CC}, with (a) 6T Si bulk FinFET. (b) 6T $In_{0.53}Ga_{0.47}As$ n-FinFETs and Ge bulk p-FinFETs. (c) 10T ST2 HTFETs. (d) Extracted nominal RSNM versus V_{CC} for the three SRAM configurations. HTFET SRAM gives the highest RSNM below 0.2 V V_{CC}.

calibrated device model mentioned in Section II. In this paper, we have considered three cases of SRAM configurations in Fig. 11, namely, (a) 6T SRAM cell with Si bulk n- and p-FinFETs, (b) 6T SRAM cell with $In_{0.53}Ga_{0.47}As$ bulk n-FinFET and Ge bulk p-FinFET, and (c) 10T ST2 SRAM cell with GaSb source-InAs channel n-HTFET and InAs source-GaSb channel p-HTFET. Fig. 11(a)–(c) shows the butterfly curves of the read configured nominal SRAM cells of the above three cases for different V_{CC}. Fig. 11(d) summarizes the nominal RSNM for different V_{CC} operations. Fig. 11 shows that, without consideration of variation, the 10T HTFET SRAM cell is more suitable for sub-200-mV power supply voltage than both Si and III-V/Ge FinFETs, because the nominal RSNM crosses over and is higher for HTFETs than FinFETs.

To develop a statistical distribution of the impact of variation on memory arrays, we develop an ensemble of 100 6T (10T) SRAM cells with FinFETs (HTFETs) having 10% and 20% of ΔW_{FIN} (ΔT_b) variations. Fig. 12 summarizes the 3σ variation of RSNM [3σ(RSNM)] for all the above variation cases. The 3σ(RSNM) is the highest for 6T SRAM cell with $In_{0.53}Ga_{0.47}As$ n-FinFET and Ge bulk p-FinFET because of the low effective mass system while 3σ(RSNM) of ST2 (10T) HTFET SRAM is lower than the former because of the use of Schmitt Feedback, as discussed in [20].

To further determine the probability of read failure of the various SRAM cells considered in this paper, we generate 100 Monte Carlo samples of variant SRAM cells for each configuration with $\%\Delta W_{FIN}$ ($\%\Delta T_b$) of 10% at different supply voltages, V_{CC}. We have defined the probability of read failure ($Pr_{readfailure}$) in an SRAM cell as the probability at which the RSNM is less than the thermal noise,

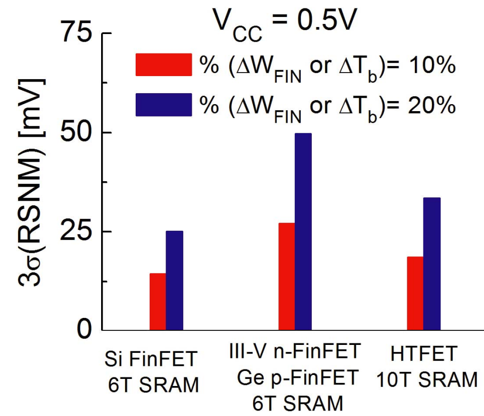

Fig. 12. Monte Carlo simulations of 100 variant SRAM cells with 6T (10T) configuration for FinFET (HTFET) having $\%(\Delta W_{FIN}$ or $\Delta T_b)$ of 10% and 20% at $V_{CC} = 0.5$ V show the highest 3σ (RSNM) for 6T SRAM cell with $In_{0.53}Ga_{0.47}As$ n-FinFET and Ge bulk p-FinFET because of the low effective mass system.

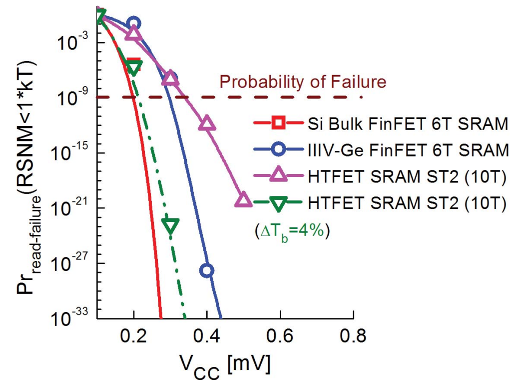

Fig. 13. Monte Carlo study of the SRAM cells with $\%\Delta(W_{FIN}$ or $T_b) = 10\%$ at different V_{CC} shows that the lowest V_{CCmin} of 196 mV is obtained for 6T SRAM cells with Si bulk FinFETs. In addition, ST2 (10T) HTFET SRAM cells can achieve this low V_{CCmin} if the $\%\Delta T_b$ is less than 4%.

i.e., kT = 26 mV [20]. $Pr_{readfailure}$ is calculated using the mean and standard deviation numbers obtained from the Gaussian fitting curves of the statistical distribution for each V_{CC}. Fig. 13 shows the $Pr_{readfailure}$ versus V_{CC} for the three SRAM configurations. The probability of read failure is higher in ST2 (10T) HTFET SRAM cell with $\%\Delta T_b = 10\%$ for $V_{CC} > 300$ mV than III-V-Ge FinFET SRAM because of the lower nominal RSNM, as observed in Fig. 11(d).

We also define the minimum supply voltage, V_{CCmin}, of the SRAM cell as the supply voltage, V_{CC}, at which the probability of read failure is one in a billion cell, i.e., $Pr_{readfailure} = 1e\text{-}9$. Fig. 13 shows that the probability of read failure of 10T HTFET SRAM is the highest when the percentage of fin width or body thickness variation for all devices is kept at $\%\Delta(W_{FIN}$ or $T_b) = 10\%$. This suggests that, despite higher nominal RSNM at lower supply voltage [Fig. 11(d)], TFET cannot be operated below 400 mV in the presence of similar variation as FinFET. Fig. 13 also shows that the $\%\Delta T_b$ in TFETs need to be improved to 4% to take advantage of the superior nominal RSNM of TFETs at supply voltage below 200 mV.

V. Conclusion

In this paper, we studied the impact of process variation and SWR on device and circuit performance using 3-D TCAD numerical simulations. The devices studied in this paper are Si bulk n-/p-FinFETs, $In_{0.53}Ga_{0.47}As$ bulk n-FinFETs, Ge bulk p-FinFETs, and GaSb–InAs n-/p-HTFETs. Among all the major process variations considered in this paper, W_{FIN} or T_b variation has the most predominant effect on device performance. Moreover, the Monte Carlo study of SWR variations in FinFETs reveals higher sensitivity to variation in $In_{0.53}Ga_{0.47}As$ bulk n- and Ge bulk p-FinFETs than their Si counterparts. Furthermore, we studied a 6T (10T) SRAM cell configuration with FinFETs and HTFETs, respectively, to see the impact of process variation on memory circuits. The probability of read-failure analysis shows that HTFETs with 10T SRAM cell configuration can achieve V_{CCmin} of 200 mV only if T_b variation is less than 4%.

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