Demonstration of p-type $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ and n-type $GaAs_{0.4}Sb_{0.6}/In_{0.65}Ga_{0.35}As$ Complimentary Heterojunction Vertical Tunnel FETs for Ultra-Low Power Logic

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Abstract: Extremely scaled high-k gate dielectrics with high quality electrical interfaces with arsenide (As) and antimonide (Sb) channels are used to demonstrate complimentary 'all III-V' Heterojunction Vertical Tunnel FET (HVTFET) with record performance at $|V_{DS}|$=0.5V. The p-type TFET (PTFET) has I_{ON} =30μA/μm and I_{ON}/I_{OFF} =10^5, whereas the n-type TFET (NTFET) has I_{ON} =275μA/μm and I_{ON}/I_{OFF}=3×10^5, respectively. NTFET shows 55mV/decade switching slope (SS) while PTFET shows 115mV/decade SS in pulsed mode measurement. Vertical TFET offers 77% higher effective drive strength than Si-FinFET for given inverter standard cell area. Energy-delay performance of TFET shows gain over CMOS for low V_{DD} logic applications.

Introduction: TFETs are promising devices for realization of transistors with *sub-kT/q* switching slope. Heterojunction TFET using mixed arsenide-antimonide materials can achieve high on-current (I_{ON}), high I_{ON}/I_{OFF} ratio, through source-side tunnel barrier height ($E_{b,eff}$) engineering. To implement energy-efficient complementary logic, both NTFETs and PTFETs need to be realized preferably in the same material system. Here, for the first time, we demonstrate complementary TFETs with high on-current, high I_{ON}/I_{OFF} in arsenide-antimonide material sharing the same metamorphic buffer layer. We demonstrate *sub-kT/q* switching slope (SS) for NTFETs. The advantages of complimentary HVTFET-based FO1 inverter over FinFET FO1 inverter are quantified from circuit layout and energy-delay performance perspective.

Fabrication: Fig. 1(a) illustrates the schematic of complimentary HVTFETs sharing a common metamorphic buffer. Figs. 1(b) and (c) depict the epitaxial hetero-structures and the cross-sectional TEM micrographs of N and PTFETs, respectively. The TFET fabrication process flow is outlined in Fig. 2. Due to the differences in channel composition (As vs. Sb), NTFET and PTFET employ separately optimized ZrO_2 and HfO_2 gate stacks, respectively.

Gate Stack Development: A primary bottleneck for steep slope III-V TFETs has been development of high-k dielectric/III-V channel interface with low interface trap density (D_{it}) and low leakage current. Particularly, in the case of antimonide (Sb) channel PTFET, the surface Fermi level movement is typically restricted due to high mid-gap D_{it}. For PTFET with $GaAs_{0.35}Sb_{0.65}$ channel, we achieve the highest accumulation capacitance density (C_{acc}) with a high temperature (250°C) plasma clean due to efficient desorption of native oxide, albeit with formation of elemental Sb which worsens D_{it} [1] (Fig. 3(a)). Optimization of the H_2 plasma surface clean temperature with 3.5 nm thick HfO_2 gate dielectric leads to the thinnest CET ~1.2 nm (capacitance equivalent thickness) with lowest mid-gap D_{it} (Figs. 3(b,c)). We achieve efficient Fermi level movement between valence band and the mid-gap but sluggish movement away from mid-gap, as observed from the normalized conductance maps in Fig. 3(d). For NTFET with $In_{0.65}Ga_{0.35}As$ channel we employ 4nm thick ZrO_2 high-k dielectric (Fig. 4(a-c)) and achieve CET of 1.1 nm [2] with low mid-gap D_{it}. The conductance peak maximum trace indicates efficient Fermi level movement with gate voltage. The dual gate stack approach is essential for realizing complimentary TFETs with high on-current, steep switching slope and high I_{ON}/I_{OFF} ratio.

DC and Pulsed I-V Characterization: Experimental room temperature transfer (I_{DS}-V_{GS}), switching (SS-I_{DS}) and output characteristics (I_{DS}-V_{DS}) for the fabricated PTFET and NTFET are shown in Fig. 5(a-c) and Fig. 5(e-g), respectively. $GaAs_{0.35}Sb_{0.65}$ channel PTFETs exhibit I_{ON} =30μA/μm at I_{ON}/I_{OFF} =10^5. The PTFET output characteristics exhibit negative differential resistance (NDR) and saturation at low temperature (77K, Fig. 5(d)) due to the suppression of mid-gap D_{it} response. $In_{0.65}Ga_{0.35}As$ channel NTFET shows I_{ON} =275μA/μm at I_{ON}/I_{OFF}=3×10^5. The mid-gap D_{it} with slow trap response time causes the DC switching slope (SS) in the fabricated N and PTFETs to exceed the thermal limit of 60 mV/decade at room temperature. We perform pulsed I_{DS}-V_{GS} measurements on TFETs with input gate voltage pulse with rise time varying from 10μs down to 300 ns to evaluate SS under actual switching environment. Fig. 6(a-d) shows the improvement in switching characteristics for both N and PTFET due to suppressed response of slow mid-gap D_{it}. *We achieve SS=55mV/decade for NTFET and SS=115mV/decade for PTFET at room temperature*. The high I_{ON} with *sub-kT/q* SS demonstration for NTFET and high I_{ON} with improved SS demonstration in case of PTFET, is a direct consequence of engineering high-quality scaled gate dielectrics and tunnel barriers in the As-Sb system.

Complementary HVTFET vs. FinFET Benchmarking: Fabricated HVTFETs are benchmarked against published results in Fig. 7. Previous PTFETs utilize Si/SOI/SiGe materials and some achieve sub-kT/q SS albeit with poor I_{ON} [3,4]. Sb-channel PTFET presented in this work shows superior performance and, in conjunction with As-channel NTFET demonstrates the potential of III-V complimentary TFET logic. Figs. 8(a-e) show 9-metal-track based standard cell layout for an FO1 inverter using FinFETs and VHTFETs. FinFET device width set by the maximum number of fins (e.g. 4 for a 9-metal-track standard cell) provides an effective drive strength improvement of 13% for an inverter (INV1) (2*H_{fin}/fin-pitch) over a planar MOSFET, assuming a fin-pitch of 60 nm and fin height H_{fin} of 34 nm at 22 nm node (Fig. 8(f)) [10]. For the same layout area, VHTFET improves the effective drive strength by 100% over planar MOSFET, benefiting from the double mesa edge gate structure. Fig.9 (a) shows the transfer characteristics of complimentary VHTFETs, calibrated using experimental results in this work, and benchmark against 22nm Si FinFETs. Assuming lower D_{it} than the experimental values, we obtain steep SS ~40 mV/decade for both P and NTFETs. Fig. 9(b) shows the energy-delay evaluation of a fan-out=1 (FO1) inverter, where TFETs show improved energy efficiency for below 0.3V applications.

Conclusions: Complimentary 'all III-V' heterojunction vertical Tunnel FET (TFET) with record I_{ON}, I_{ON}/I_{OFF} and SS performance are demonstrated at $|V_{DS}|$ = 0.5V. This work shows the feasibility of Tunnel FETs for low V_{DD} applications beyond FinFETs.

References: [1] A. Ali et al., APL, Oct. 2010 [2] V. Chobpattana et al., APL, May 2014 [3] R. Gandhi et al., EDL, Nov. 2011 [4] K. Jeon et al., VLSI 2010 [5] L. Knoll et al., EDL, June 2013 [6] G. Dewey et al., IEDM 2011 [7] M. Noguchi et al., IEDM 2013 [8] Bijesh et al., EDL 2014 [9] A. C. Seabaugh, Proc. IEEE Dec 2010 [10] C.-H. Jan et al., IEDM 2012

I. Complimentary III-V TFET Structure Detail

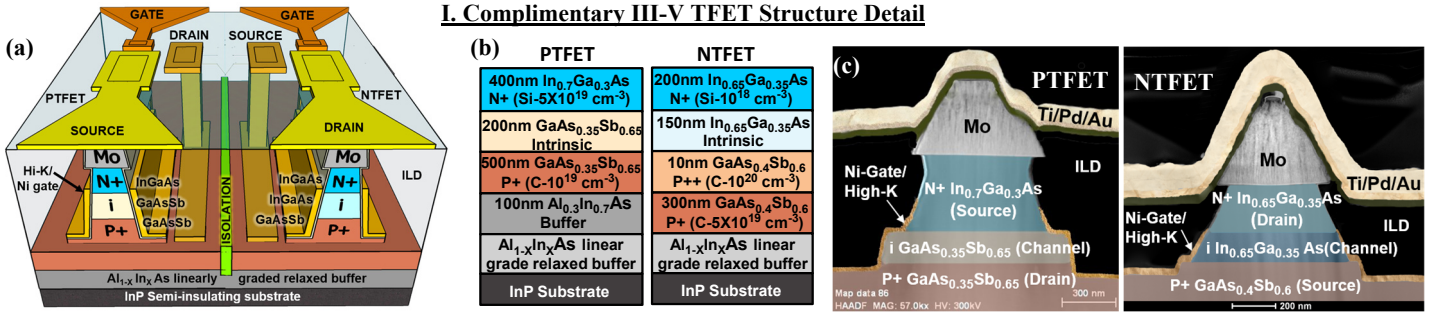


Fig. 1. (a) Schematic of complimentary PTFET and NTFET on common metamorphic buffer technology; **(b)** Starting hetero-structures, and **(c)** Cross-section TEMs

II. Process Details

TFET Process flow

- Mo Sputter. Ti/Cr etch mask formation
- MESA dry etch, wet etch undercut
- Gate Dielectric Deposition
- Ni (Thermal Evap.) gate deposition
- Source contact definition (Ti/Pd/Au)
- ILD (BCB) planarization and etch back
- Drain pad definition (Ti/Pd/Au)
- Selectively dry etch ILD to form Gate/Source Via
- Gate, Source pad definition (Ti/Pd/Au)

Gate Dielectric Deposition Steps

PTFET

- Ex-situ 40s (1:1) HCl:H_2O wet etch
- In-situ 1.5 min H_2 plasma at 150°C
- 3.5 nm HfO_2 ALD at 250°C
- 20 min FGA [65% Ar, 35% H_2] at 350°C

NTFET [2]

- Ex-situ 3 min BOE
- In-situ 9 cycles N_2 /TMA at 300°C
- 4 nm ZrO_2 ALD at 300°C
- 15 min FGA [95% N_2, 5% H_2] at 400°C

Fig. 2. Process flow details for vertical TFET

III. Scaled PTFET Gate Stack: CET of 1.2 nm on p-GaAsSb

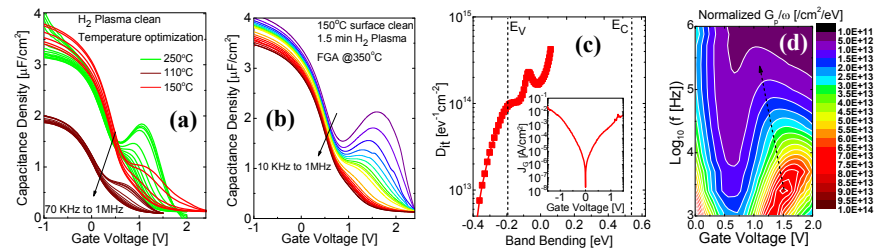


Fig. 3. (a) CV characteristics of p-type $GaAs_{0.35}Sb_{0.65}$ MOSCAPs with 3.5 nm HfO_2 with H_2 plasma surface clean at various temperatures; (b) CV characteristics of optimized gate stack; (c) D_{it} extraction using Terman method. Gate leakage is shown in the inset; (d) Normalized parallel conductance plot with dotted line trace showing movement of the conductance peak maximum.

IV. NTFET Gate Stack [2]: CET 1.1 nm on n-InGaAs

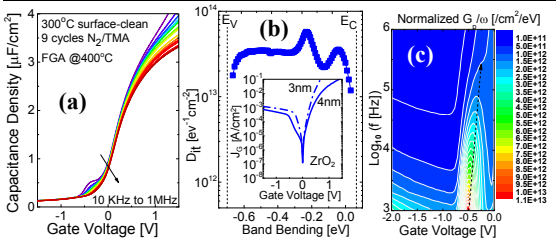


Fig. 4. (a) CV characteristics of n-type $In_{0.53}Ga_{0.47}As$ MOSCAPs with 4nm ZrO_2 with N_2 plasma/TMA clean [2]; (b) D_{it} extraction using Terman method. Gate leakage for both 3nm and 4nm ALD ZrO_2 is shown in the inset; (c) Normalized parallel conductance plots for 4nm ZrO_2. Dotted line trace shows the movement of conductance peak maximum.

V. DC I-V Characterization

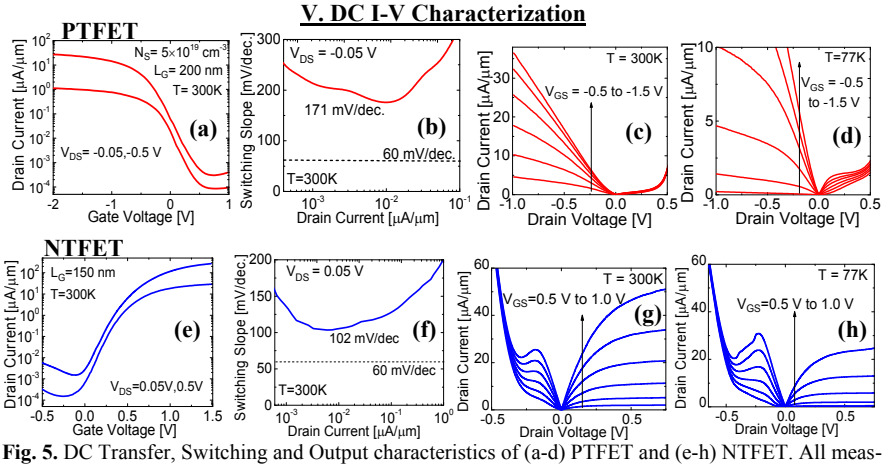


Fig. 5. DC Transfer, Switching and Output characteristics of (a-d) PTFET and (e-h) NTFET. All measurements are at T=300K, except the additional T=77K data in (d) and (h). NDR is visible in PTFET output characteristics at T=77K, due to the suppression of trap response. N_S denotes PTFET source doping concentration.

VI. Pulsed I-V Characterization

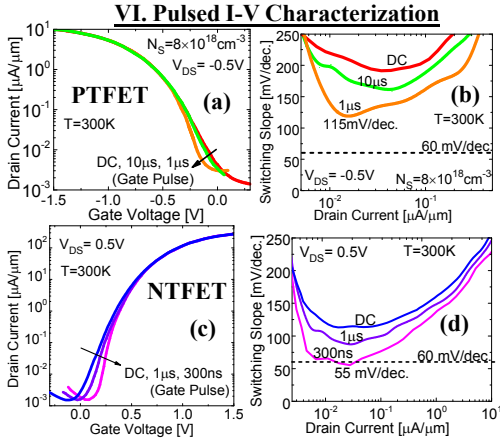


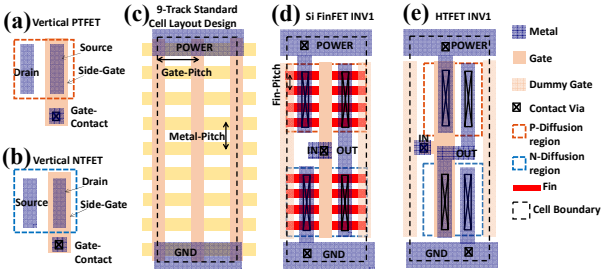
Fig. 6. Pulsed mode transfer and switching characteristics of (a-b) PTFET and (c-d) NTFET. All measurements at 300K

VII. TFET Device Benchmark

	PTFET				NTFET				
	[3]	[5]	This work	This work	[6]	[7]	[8]	This Work	This work
Structure	SiNW GAA	SiNW	III-V N_S=5X10^{19}cm^{-3}	III-V [Pulsed I-V] N_S=8X10^{18}cm^{-3}	III-V	III-V	III-V	III-V	III-V [Pulsed IV]
V_{DS} [V]	-0.6	-0.5	-0.5	-0.5	0.3	0.3	0.5	0.5	0.5
I_{ON} [μA/μm]	1.8	10	14	10	12	6	109	245	275
I_{MIN} [μA/μm]	1.2X10^{-6}	2.0X10^{-6}	3.0X10^{-4}	2X10^{-3}	1.0X10^{-4}	2.0X10^{-6}	2.9X10^{-4}	1.4X10^{-3}	1.4X10^{-3}
I_{ON}/I_{MIN}	1.4X10^{6}	5.0X10^{6}	4.7X10^{4}	5X10^{3}	1.2X10^{5}	3.0X10^{6}	3.8X10^{5}	1.8X10^{5}	2.0X10^{5}
SS_{Eff} [mV/dec.]	122	112	161	202	89	85	134	143	132
SS_{Min} [mV/dec.]	30	90	171	115	58	64	97	102	55
EOT [nm]	4.5	0.7	0.8	0.8	1.1	1.4	0.7	0.7	0.7
Lg [nm]	140	200	200	200	100	-	150	150	150

Fig. 7. Benchmark of Si and III-V TFETs. SS_{Eff}= (V_{ON}-V_{MIN})/ (2log (I_{ON}/I_{MIN})) [9]; V_{ON} (V_{MIN}) corresponds to the gate voltage at I_{ON} (I_{MIN}). $|V_{ON}|$ is limited to 1.5V from $|V_{MIN}|$.

VIII. TFET Inverter layout and Performance Benchmark



(f)

Technology	22 nm Planar MOSFET INV1	22nm FinFET INV1	22nm Vertical HTFET INV1
Layout Induced Drive Strength Enhancement at the same Device Area	1X	1.13X	2X

Fig. 8. Device layout of (a) vertical P-HTFET and (b) vertical N-HTFET; (c) Layout illustration of a 9-metal-track standard cell library design. Layout area is determined by 9N×Gate-pitch×9metal-pitch. N is number of gate-pitches in the lateral direction. Inverter layout of (d) Si FinFETs at a maximum fin number of 4 and (e) proposed complementary vertical HTFETs; (f) Layout induced device drive strength enhancement (effective device width at a given device area) comparing the INV1 using 22 nm planar MOSFETs, 22 nm FinFETs and 22 nm vertical HTFETs

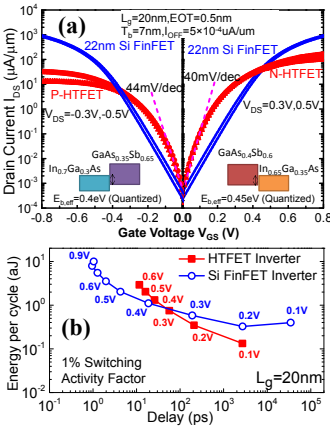


Fig. 9. (a) Simulated device characteristics of the proposed complementary HTFET (b) Energy vs. delay of a FO1 inverter comparing 22nm Si FinFET and HTFET with 1% switching activity factor at different supply voltages. Cross-over at 0.3V shows energy efficiency advantage of HTFET inverter.