Analysis of Local Interconnect Resistance at Scaled Process Nodes

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Introduction: M0/M1 local interconnects exhibit steadily increasing resistance with Line-width (LW) and Critical Dimension (CD) scaling. Enhanced electron scattering from metal surface and grain boundaries as well as increased volume of highly resistive liners/diffusion barriers in the interconnect bulk are key contributors for this trend [1]. Via0 resistance was identified as dominant component of local interconnect resistance at 22 nm process node [1]. Consequently at 14 nm process node back end of line (BEOL) process relaxes Via0 CD [2]. We show that with the latest trend of M0/M1 LW scaling along with Via0 and Contact CD scaling, M0 and Contact emerge as prominent contributors to local interconnect resistance at 5 nm process node. We present comprehensive analysis of local interconnect resistance for interconnects fabricated from both dual damascene and single damascene processes. Additionally, we investigate impact of replacing Tungsten in Contact and M0 line by a lower resistivity Tungsten, at 5 nm process, and quantify subsequent improvement in transistor on-state performance.

Local Interconnect Simulation: Numerical simulator Sentaurus TCAD [3] is used to model transport in 3-Dimensional (3D) M0/M1 local interconnect structure (Fig.1 (a)), with technology scaling from 22 nm to 5 nm node. In dual damascene (DD) interconnect (Fig. 1(b)), both metal line and via are fabricated simultaneously. On the contrary, in single damascene (SD) process metal line and via are formed in separate steps which results in an additional Metal-Nitride liner in between metal line and via (Fig. 1(c)). While DD process is preferable due to fewer number of steps, still it has challenges of lining and filling high aspect ratio metal line and via features which become significant with process scaling. We assume three fins contacted per Via0 at every process node. Fins make electrical connection with Tungsten (W) based local interconnect M0 through W Contact with Ti/TiN serving as liner/diffusion barrier. Copper via (Cu Via0) connects M0 to the first metal layer Cu M1 where TaN/Ta acts as barrier/liner layer. Contact and Via0 geometries as well as M0/M1 local interconnect (both bulk metal and liner) dimensions are adopted from published data for 22 nm and 14 nm processes [2,4]. Dimensions at 10 nm, 7 nm and 5 nm processes are estimated from ITRS 2013 projections (Fig. 1(d), [1]). Impact of increasing interconnect resistivity with LW and CD scaling is accounted in simulation by employing size-dependent resistivity for local interconnects from [5]. Resistance of each region is extracted from the solution of Fermi potential across each metal layer and corresponding current magnitude.

Local Interconnect Resistance Analysis: Figure 2 shows the current density plot of 3D M0/M1 interconnect stack simulated at 22 nm and 5 nm process nodes. High current density is observed in Cu Via0 whereas the current density falls by nearly 2 orders of magnitudes in significantly resistive liners. Potential distribution and resistance breakdown for DD and SD interconnects is depicted in Fig. 3. In DD interconnect, at 22 nm process, major potential drop occurs Cu Via0 TaN/Ta layers as a result of narrow Via0 CD and high TaN/Ta resistivity (Fig. 3(a)). At 14 nm process, Via0 CD is relaxed to alleviate this bottleneck [2]. However with further interconnect scaling, W M0 and Contact become significant contributors to total M0/M1 resistance as shown in Fig 3(b). At 5 nm process W M0 and Contact comprise 65% of total M0/M1 stack resistance due to narrow CD as well as higher bulk metal resistivity. For SD interconnect the total resistance is even further degraded due to additional contribution from high resistivity liner layer interposing metal and via, which results in 12% higher total resistance compared to DD interconnect at 5 nm process (Fig. 3(c-d)). We further explore replacing W in both M0 and Contact by a lower resistivity W metal W_{lo} (in this case we assumed hypothetical resistivity equal to Cu). We assume a single diffusion barrier (TiN) for W_{lo} process. Figure 4(a) shows that replacement of bulk metal by W_{lo} reduces M0/M1 interconnect resistance by 43%. Benefits of introducing a lower resistivity W in M0 local interconnect are more pronounced for M0 lines (Figs. 4(b-c) show 75% improvement with low resistivity W) which connect devices over distances so that the current flows horizontally and effectively occupies entire volume of low resistivity fill metal. A 3D-FinFET set-up (Fig. 5(a-b)) initially calibrated to 22 nm process [6] and scaled to dimensions of 5 nm process with on-current (I_{ON}=1.5mA/μm) adjusted corresponding to ~15% rise with every process generation change at a constant off-current I_{OFF}=10nA/μm, is employed to evaluate impact of parasitic M0/M1 interconnect resistance on FinFET performance. As observed from Fig. 5(c), I_{ON} improves by 5% on replacing W in M0 and Contact by lower resistivity W, providing significant saving at 5 nm process.

Conclusion: A detailed analysis of local interconnect resistance with process scaling to 5 nm technology node is presented for both SD and DD interconnects. W M0 and Contact are identified as key resistance contributors at 5 nm process. Introducing a lower resistivity W for metal fill in M0 and Contact shows 43% reduction in M0/M1 resistance along with 5% gain in I_{ON} which are significant for ultra-low V_{cc} based 5 nm process.

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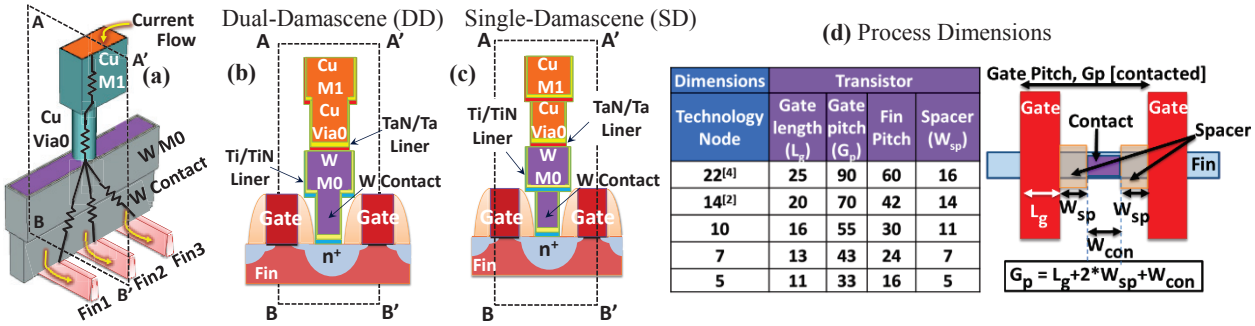

Dimensions	Transistor			
Technology Node	Gate length (L_g)	Gate pitch (G_p)	Fin Pitch	Spacer (W_{sp})
22[4]	25	90	60	16
14[2]	20	70	42	14
10	16	55	30	11
7	13	43	24	7
5	11	33	16	5

Fig. 1. (a) 3D schematic of simulated M0/M1 local interconnect structure. Three contacted fins are also shown for reference. 2D cross-section of the interconnect stack fabricated by **(b)** Dual-Damascene, and **(c)** Single-Damascene processes. (d) Process dimensions used in simulation.

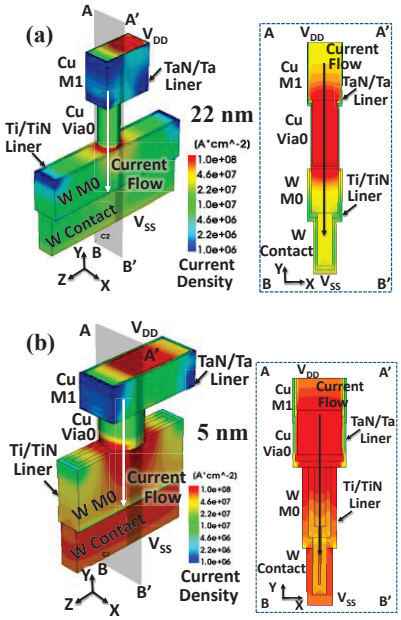

Fig. 2. Simulated 3D structure with 2D cross-section for DD interconnect at (a) 22nm and (b) 5 nm process. High magnitude of current density through Cu Via0 (along with W M0 and W Contact in 5nm process) in contrast with low current density through liners is observed.

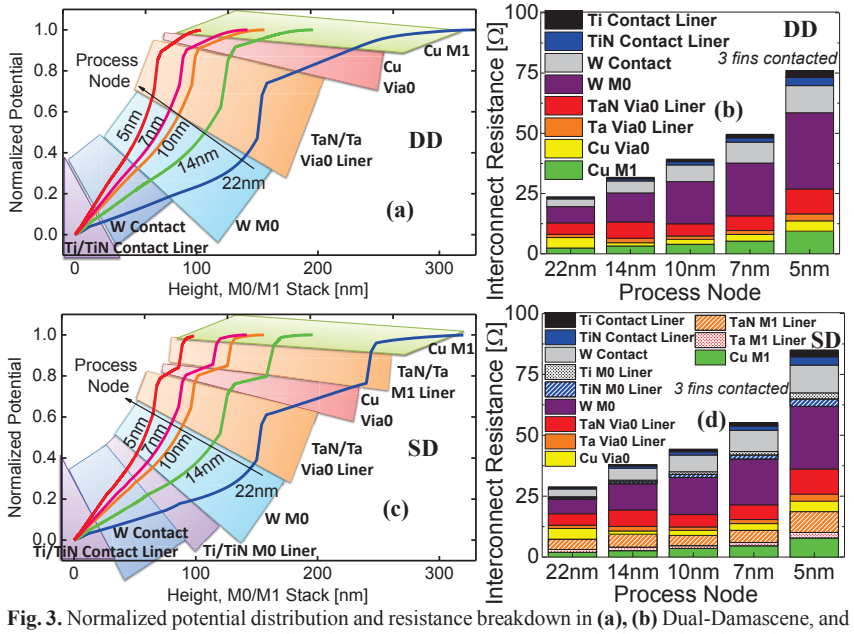

Fig. 3. Normalized potential distribution and resistance breakdown in **(a), (b)** Dual-Damascene, and **(c), (d)** Single-Damascene M0/M1 interconnect structure, respectively as function of process technology scaling. W M0 and W Contact emerge as prominent contributors to local interconnect resistance at 5 nm process.

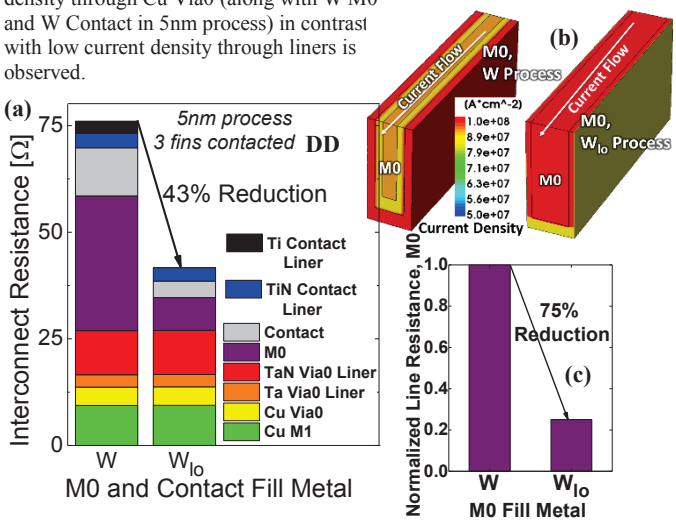

Fig. 4. **(a)** M0 and contact resistance is reduced significantly at 5 nm process node by replacing in M0 and Contact fill by low resistivity W_{lo}. **(b)** 3D simulation of M0 local interconnect at 5 nm process, showing 75% line resistance reduction in W_{lo} M0 process compared to W M0 process **(c).**

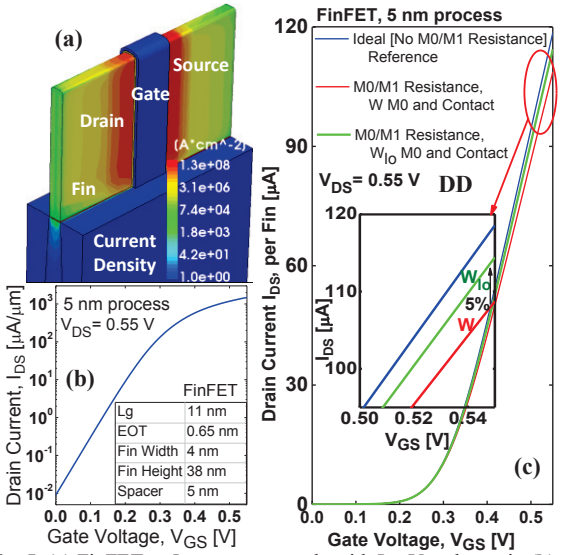

Fig. 5. (a) FinFET at 5 nm process node with I_{DS}-V_{GS} shown in **(b).** **(c)** Impact of M0/M1 (DD) interconnect resistance on on-current I_{ON}. W_{lo} based M0 and Contact process improve I_{ON} by 5% compared to W based process, providing significant saving at ultra-low Vcc based 5 nm process technology.

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