Electron Trapping Dominance in Strained Germanium Quantum Well Planar and FinFET devices with NBTI

Nidhi Agrawal[1], Ashish Agrawal[1], Subhadeep Mukhopadhyay[2], Souvik Mahapatra[2], and Suman Datta[1]

[1]The Pennsylvania State University, University Park, USA

[2]Indian Institute of Technology Bombay, Mumbai, India

Abstract: We perform a comparative study of Negative Bias Temperature Instability (NBTI) reliability on compressively strained Germanium (s-Ge) Quantum Well (QW) Planar and FinFET p-type devices. We see electron trapping from the gate electrode in all these devices with applied negative stress. FinFETs show less ΔV_T than Planar but with 1.8 times higher stress time exponent (n) and slower recovery rate than Planar. Also, $\Delta g_m/g_{m0}$ of FinFETs improves with increasing stress.

Introduction: With CMOS scaling, the thinner gate dielectrics suffer with increased electric fields. This results in higher Negative Bias Temperature Instability (NBTI) making it harder to guarantee a ten-year of lifetime at the expected operating voltages. Meanwhile, high mobility materials like SiliconGermanium (SiGe) or Germanium (Ge) are considered as promising candidates for Silicon (Si) replacements. In this paper, we present a comparative study of NBTI reliability on Strained Ge (s-Ge) Quantum Well (QW) Planar and s-Ge QW FinFET p-type devices.

Experimental setup: The s-Ge QW Planar and FinFET devices used in this study were fabricated using the process described in [1]. Fig. 1 shows the schematic of (a) s-Ge QW Planar wafer stack and (b) s-Ge QW FinFET cross-section profiles. The gate stack deposited in these devices is 25A HfO_2/ 7A Al_2O_3/ 6A GeO_x with an EOT between 1.2-1.5nm. Fig. 2 shows the transfer characteristics of s-Ge QW Planar and FinFET with fin width, W_{FIN} of 20nm at V_{DS} = -0.05V and -0.5V showing high ON current, I_{ON} and excellent I_{ON}/I_{OFF} = $2x10^4$ [1]. The Ultra Fast Measure-Stress-Measure (UF-MSM) NBTI reliability study using Agilent B1530 Parameter Analyzer is performed on these devices. Fig. 3 shows the schematic of the stress and recovery DC bias waveform applied at the gate. After every stress (or recovery after stress) bias, experiment is interrupted for 10μs long measurement time to sweep the gate voltage and record the device current. This fast measurement time ensures negligible recovery when measured during stress intervals and no stress when measured during recovery periods. The NBTI stress on s-Ge QW Planar and FinFET p-types devices used in this study show dominant electron trapping from the gate electrode into the oxide than hole trapping from the substrate (Fig. 4).

Results and Discussions: Threshold voltage, V_T, from the transfer characteristics is extracted using the peak transconductance, g_m, method. Due to electron trapping from gate, the $|V_T|$ reduces with increasing negative stress. Fig. 5 (a) and (c) plots the $|\Delta V_T|$ with increasing stress and recovery times for different gate stress voltages, $V_{G,str}$, at 25°C for s-Ge QW Planar while Fig. 5 (b) and (d) plots the same for FinFETs. The extracted time exponents at higher stress times for Planar and FinFET devices are 0.12 and 0.22, respectively even though FinFETs show lower $|\Delta V_T|$ than Planar. Both Planar and FinFET devices fully recover after 1000s of recovery time but the rate of recovery is slower in FinFET devices. This indicates a possible hole trapping compensation occurring in FinFETs that takes longer time to recover. Fig. 6 plots the normalized transconductance degradation, $\Delta g_m/g_{m0}$, vs. ΔV_T for Planar and FinFET devices. With increasing stress, $\Delta g_m/g_{m0}$ of Planar devices increases while for FinFETs it decreases. Table 1 compares the NBTI parameters of Planar vs. FinFET devices.

Conclusion: In this paper, we present an NBTI study done on s-Ge QW Planar and FinFET devices using UF-MSM scheme. We observe dominant electron trapping in the oxide with applied negative stress in both types of devices. Although, ΔV_T of FinFET is less than Planar, yet the stress time exponent is 1.8 times higher and recovery rate is slower than Planar. This indicates a possible hole trapping compensation occurring in FinFETs. Also, $\Delta g_m/g_{m0}$ of FinFETs improves with increasing stress.

Reference: [1] A. Agrawal et al., IEDM 2014

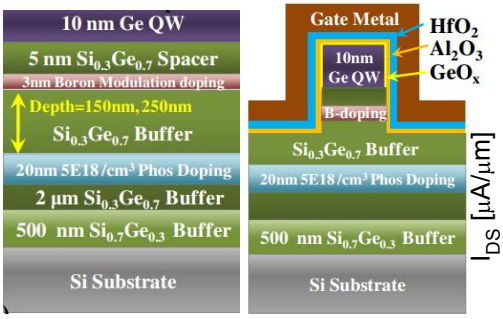


Fig1. Schematic of (a) s-Ge QW Planar wafer stack, and (b) FinFET stack with 25A HfO_2/ 7A Al_2O_3/ 6A GeO_x gate and Ti/Au gate metal contact. [1]

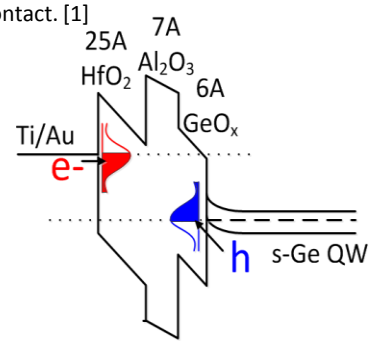


Fig4. Schematic Band Diagram of the gate stack under negative bias. Ge QW devices used in this study are dominated by electron trapping from gate electrode rather than hole from channel under NBTI.

Fig5. The $|V_T|$ shift at 25°C under NBTI reduces with stress indicating electron trapping. (a) and (c) show stress and recovery ΔV_T for Ge QW Planar devices while (b) and (d) show the same for FinFET devices. Planar devices have higher ΔV_T shift than FinFET though n is lower in the former. Also, we observe that FinFET devices recover slower than Planar.

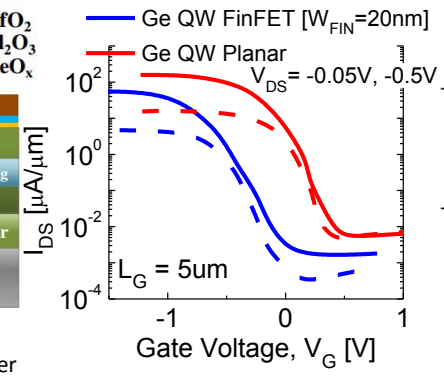


Fig2. IDVG comparison of Ge QW Planar with FinFET architecture shown in [1]

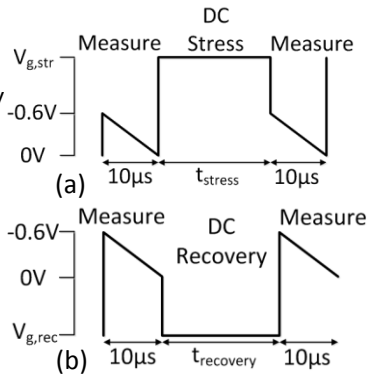
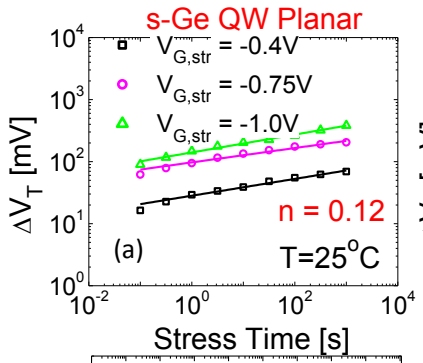
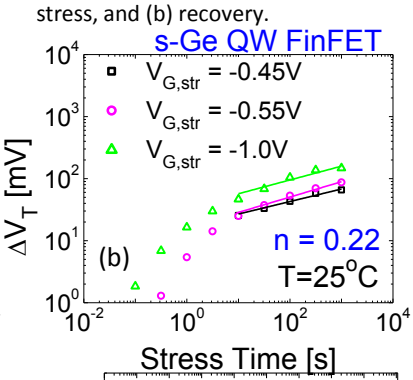
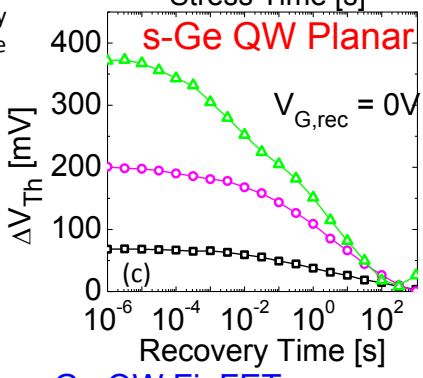
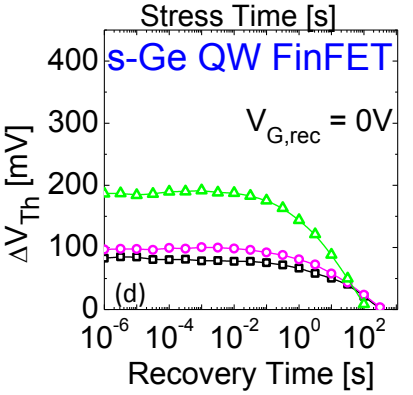


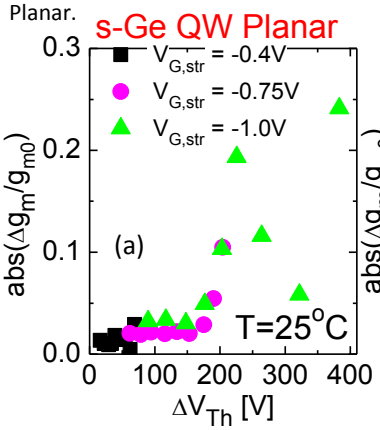
Fig3. DC Measurement schematic of Ultra Fast-MSM using Agilent B1530 Parameter Analyzer with measurement time of 10μs for (a) stress, and (b) recovery.











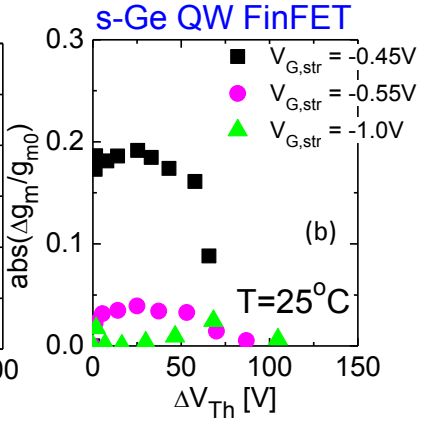


Fig6. absolute value of Normalized Transconductance degradation of (a) s-Ge QW Planar and (b) s-Ge QW FinFET. Planar devices' transconductance degrades with increasing stress while for FinFET it improves.

Table 1: NBTI parameter comparison between s-Ge QW Planar and FinFET devices.

Parameter	Planar	FinFET
time factor, n	0.12	0.22
ΔV_T@-1V, 1000s [mV]	383	148
Recovery	Faster	Slower
$\Delta g_m/g_{m0}$@-1V, 1000s [%]	24	0.6