Indium Arsenide (InAs) Single and Dual Quantum-Well Heterostructure FinFETs

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Abstract: This work presents experimental demonstration of InAs single and dual quantum well (DQW) heterostructure FinFETs (FF) and their superior performance over $In_{0.7}Ga_{0.3}As$ QW FF. Peak mobility of 3,531 cm^2/V-sec and 3,950 cm^2/V-sec are obtained for InAs single QW FF and InAs DQW FF, respectively, at a fin width (W_{fin}) of 40nm and L_G = 2μm. Peak g_m of 480 μS/μm , 541 μS/um; I_{DSAT} of 121 μA/μm, 135 μA/μm; and SS_{SAT} of 101 mV/dec,103 mV/dec is demonstrated for single and DQW FF, respectively, at L_G=300nm (V_D = 0.5V, I_{OFF}=100 nA/μm). Finally, InAs DQW is shown to be a viable alternate channel for high aspect ratio n-channel FinFET.

Motivation: Superior electron mobility at higher indium percentage (In%) is readily evidenced by Hall measurements (Fig 1) [1-3]. The resulting benefit is demonstrated in planar FETs [4-7] and multi-gate FETs [8,9]. Multi-gate FFs offer robust electrostatics [10,11] and higher effective width per layout area [9]. This motivates design of tall InAs fin devices. Pseudomorphic growth on InP substrate however, limits InAs to QWs of <5nm thickness. This necessitates stacking of multiple QWs to create InAs heterostructure FF. In this work, we explore InAs heterostructure FF design. Stacking InAs QWs to increase fin height leads to higher charge density per fin, but can reduce mobility due to increased sidewall roughness exposure [12]. Further, adding $In_xGa_{1-x}As$ cladding layers to stack InAs QWs results in reduced sub-band spacing which increases carrier density but may enhance inter sub-band scattering.

Heterostructure Fin Design: Fig 2 shows schematic cross-section of three different heterostructure FinFETs. Fig 3 shows the energy band diagrams and band offsets for the heterostructures (zero bias) using 1-D Schrodinger-Poisson (SP) simulations. The separation between the first and second sub-bands (ΔE_{1-2}) reduces monotonically as we go from $In_{0.7}Ga_{0.3}As$ QW to single and dual InAs QW. This arises from the wavefunction spreading out of the InAs QWs into the cladding layers resulting in a composite wavefunction for the heterostructure fin. This allows the DQW FF to support higher inversion charge. Fig 5 shows the FF electron density profiles from 2D S-P simulations. The electrons preferentially localize in the InAs QWs for all operating voltages.

Heterostructure FinFET Fabrication: InAs single and dual QWs are grown on InP substrates by MBE. Fig 4 outlines the process flow. We demonstrate a new side wall image transfer (SIT) process for fin formation (Fig 7). A high temperature (180°C) Cl_2/N_2 plasma based RIE is used to etch the fins resulting in excellent sidewall profile with a fin pitch of 105 nm (Fig 10). The high-k gate stack is formed using alternate cycles of N_2 plasma and TMA pulses for surface passivation followed by thermal ALD of 3.25nm HfO_2 and thermal evaporation of Nickel for gate stack formation.

FinFET Characterization: Due to the spatial non-uniformity of the electrons in the heterostructure fin (Fig 5), we introduce an effective fin width, W_{eff}, using a weighted average of carrier density. Extracted W_{eff} shows 8% reduction for the InAs single QW and 13% reduction for the InAs dual QW FFs, respectively, compared to $In_{0.7}Ga_{0.3}As$ QW FF (Fig 6). Fig 8 shows the I_DV_D characteristics for long channel FF (L_G=2μm;W_{fin}=40nm). The left axis shows I_D normalized to W_{eff} and right axis shows raw I_D as measured per fin. Fig 9 shows the CV for planar $In_{0.53}Ga_{0.47}As$. Ultra-thin CET (capacitance equivalent thickness) of 1.15nm is obtained with reduced frequency dispersion indicating low band-edge and mid-gap D_{IT}. Fig 11 shows transfer characteristics of the three FFs normalized to W_{eff}. Both single and dual QW InAs FFs fabricated in this work show excellent sub-threshold slope (SS) of 87 and 94mV/dec, respectively. Fig 12 shows the split-CV measurements on long channel (L_G = 5 μm) multi-fin devices at 1MHz yielding CET of 1.3nm. The DQW FFs show 5% higher capacitance indicating higher carrier density. Field effect mobility is extracted through inverse modeling, after calibration to the experimental I_DV_G (Fig 13). Peak mobility of 3,950 cm^2/V-sec and 3,531 cm^2/V-sec are obtained for dual and single QW FFs at carrier density of $3.2x10^{11}$ cm^{-2} and $2x10^{11}$ cm^{-2}, respectively. At higher V_G, however, InAs DQW FF mobility rolls off faster, due to higher exposure to sidewall roughness and inter sub-band scattering. Fig 14 shows the experimental I_DV_G and g_{m_SAT} for L_G = 300nm devices. DQW FF shows 9% higher I_{DSAT} and 12.5% higher g_{m_max} over single QW FF counterpart.

Benchmarking: Fig 15 shows the simulated electron velocity profiles, based on experimental calibration, for short channel Si FF [11], InAs QW FF and InAs DQW FF at L_G = 26nm and W_{Fin} = 8nm (V_{DD} = 0.5V). The injection velocities at virtual source (v_{inj}) are $5.3x10^6$, $1.34x10^7$ and $1.67x10^7$ cm/sec for Si FF, InAs single and DQW FFs, respectively. Fig 16 summarizes the expected performance gain. The InAs DQW FF provides 478μA/μm compared to 417μA/μm in Si FF at I_{OFF} = 100nA/μm and V_{DD} = 0.5V.

Conclusion: In this work, we demonstrate novel InAs QW heterostructure FinFETs as an alternate n-channel option beyond Si FinFET. Both InAs single and dual QW channels demonstrate peak mobility >3000 cm^2/V-sec. InAs DQW FF outperforms the single QW counterpart due to higher carrier density in the fin. SIT patterning and high temperature fin etch along with N_2 plasma-TMA passivated gate stack provide excellent SS across all FinFETs. Long channel (L_G=2μm) InAs Single and Dual QW FFs demonstrate I_{ON} = 84μA/μm and 100μA/μm, respectively, at V_G-V_T=0.6V and V_{DS} = 0.5V (19% gain). Intermediate channel length (L_G=300nm) DQW FF shows 12.5% g_{m_max} gain over QW FF. Projected short channel (L_G=26nm) InAs DQW FinFET is shown to exhibit 15% higher I_{ON} with comparable DIBL and SS as Si FinFETs making InAs Heterostructure FinFETs a viable option in the future.

References [1] T. Suemitsu, et al, *IEEE TED*,49,2002, pp. 1694 [2] I. Watanabe, et al, *IEEE EDL*,26,2005, pp. 425 3[5] J. B. Boos, et al, *IEEE TED*,45,1998, pp.1869 [4] D.-H. Kim et al, *IEDM* 2009, pp. 861 [5] S-H. Lee et al, *VLSI symp.*, 2014, pp. 54 [6] J. Lin et al, *IEDM* 2013, pp. 421 [7] S. W. Chang et al, *IEDM* 2013, pp. 417 [8] S. H. Kim et al, *IEDM* 2013, pp. 429 [9] Arun V. T. et al, *VLSI Symp.* 2014, pp. 72 [10] M. Radosavljevic et al, *IEDM* 2011, pp. 765 [11] C. H. Jan et al, *IEDM* 2012, pp.44 [12] A. V. Thathachary, *Nano. Lett.*, Jan. 2014, pp. 626

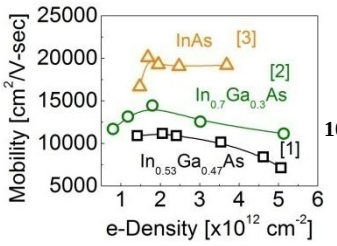
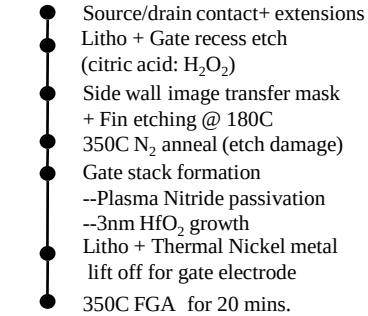


Fig1. Electron Hall mobility for III-V quantum-wells with varying Indium percentage [1-3]



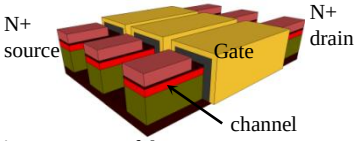


Fig4. FinFET fabrication process flow and schematic representation of device structure

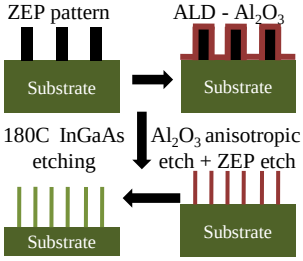


Fig7. Schematic fabrication process flow for sidewall image transfer (SIT) technique for fin formation

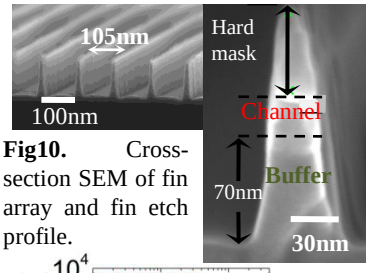


Fig10. Cross-section SEM of fin array and fin etch profile.

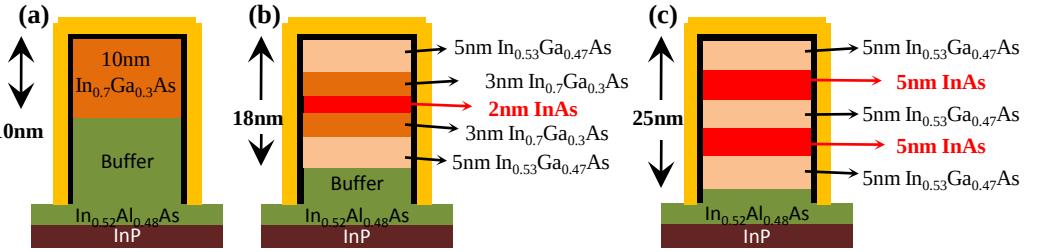


Fig2. Cross-section schematic of **(a)** InGaAs QW **[9]** and **(b)** InAs QW , **(c)** InAs dual QW (DQW) FinFETs (FF). Structures **b** & **c** are investigated in this work as alternate high performance n-channel FFs

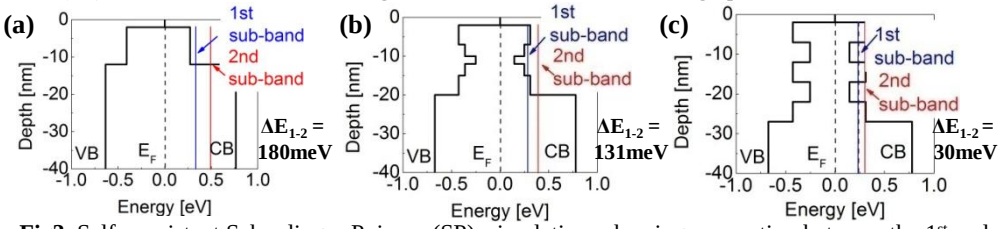


Fig3. Self-consistent Schrodinger-Poisson (SP) simulations showing separation between the 1st and 2nd sub-band monotonically reduces going from structure **a** to **b** and **c.**

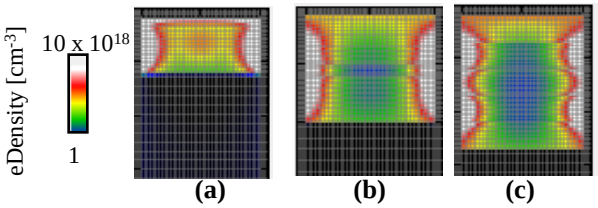


Fig5. Two-dimensional SP simulations showing electron density profiles for FinFET structures **(a),(b)** and **(c)** at $V_G - V_T$ = 0.5V and W_{fin} = 40nm. Inversion charge preferentially localizes in the InAs layers for structures **b** and **c.**

FinFET	$W_{eff} = W_{Tot} \times \frac{\sum N_S W}{W_{Tot} \cdot N_{S\_MAX}}$
$In_{0.7}Ga_{0.3}As$ QW	(40 + 2x10) **x1** = 60nm
InAs QW	(40 + 2x18) **x0.92** = 70nm
InAs DQW	(40 + 2x25) **x0.87** =78.3nm

Fig6. Estimation of effective fin width, W_{eff}, using weighted average of carrier density (scaling factor in bold font).

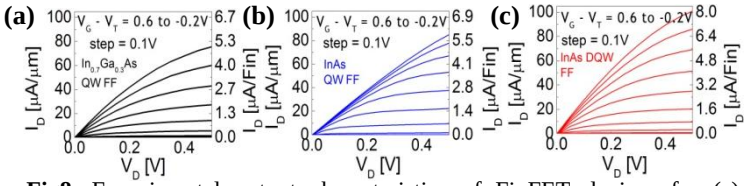


Fig8. Experimental output characteristics of FinFET devices for (a) InGaAs QW **(b)** InAs QW and **(c)** InAs DQW architectures with L_G = 2μm, W_{fin} = 40nm. **Left axis:** current normalized to W_{eff} **Right axis:** raw current as measured per fin

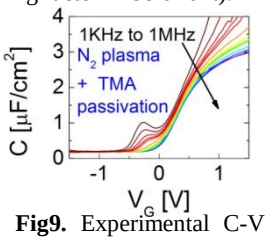


Fig9. Experimental C-V for planar 3.25nm HfO_2 /$In_{0.53}Ga_{0.47}As$ MOSAPs with CET = 1.15nm

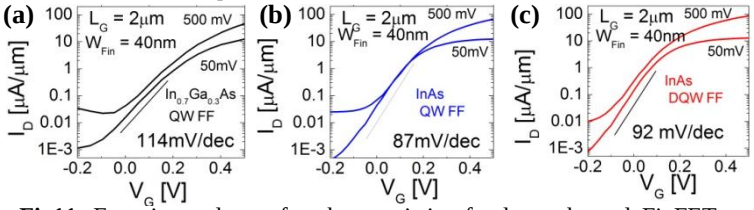


Fig11. Experimental transfer characteristics for long channel FinFET devices. Current is normalized to W_{eff} .

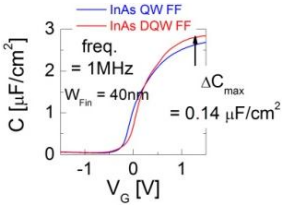


Fig12. Experimental multi-fin split-CV measurement

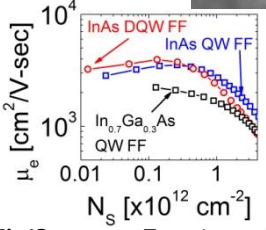


Fig13. Experimental electron field effect mobility extracted by inverse modeling from long channel FinFET I_D-V_G and split C-V measurements.

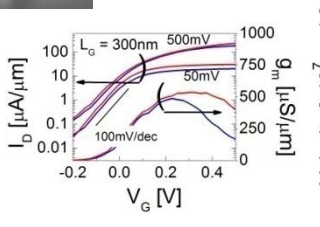


Fig14. Experimental I_D-V_G for L_G =300nm showing gain in I_D and g_m for InAS DQW over InAs QW FF (normalized to We_{ff})

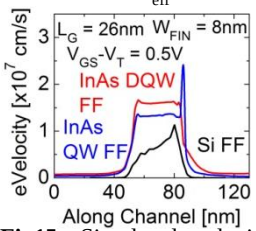


Fig15. Simulated velocity profiles for L_G = 26nm after calibration to experimental data showing highest V_{inj} gain for InAs DQW FF.

V_D = 0.5V; I_{OFF} = 100nA/μm					
Substrate	I_{DLIN} μA/μm	I_{DSAT} μA/μm	DIBL mV/V	SS_{SAT} mV/dec	G_{m_max} μA/μm
Si FF [7]	131.5	417.5	30	71	1768
InAs QW	145.2	309.2	39	87	1125
InAs DQW	238.9	478.3	32	76	1734

Fig16. Benchmarking of simulated performance (calibrated to experiment) of InAs QW and DQW FinFET against 22nm Silicon FinFETs [11]