NANO LETTERS

LETTER

pubs.acs.org/NanoLett

Enhanced Transport and Transistor Performance with Oxide Seeded High-κ Gate Dielectrics on Wafer-Scale Epitaxial Graphene

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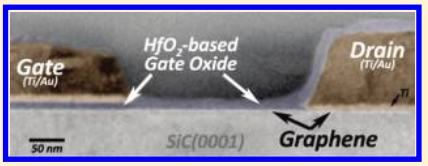
Supporting Information

ABSTRACT: We explore the effect of high-κ dielectric seed layer and overlayer on carrier transport in epitaxial graphene. We introduce a novel seeding technique for depositing dielectrics by atomic layer deposition that utilizes direct deposition of high-κ seed layers and can lead to an increase in Hall mobility up to 70% from as-grown. Additionally, high-κ seeded dielectrics are shown to produce superior transistor performance relative to low-κ seeded dielectrics and the presence of heterogeneous seed/overlayer structures is found to be detrimental to transistor performance, reducing effective mobility by 30−40%. The direct deposition of high-purity oxide seed represents the first robust method for the deposition of uniform atomic layer deposited dielectrics on epitaxial graphene that improves carrier transport.



KEYWORDS: Graphene, epitaxial graphene, gate dielectric, atomic layer deposition, physical vapor deposition, Al_2O_3, HfO_2, SiO_2, field effect transistor

Since its recent discovery,[1,2] graphene has attracted much interest due to its exceptional properties, including high saturation velocity,[3] high current carrying capacity,[4] excellent possibility for scaling,[5] and high transconductance.[6,7] These attributes, and a sufficiently low noise level,[8] could make graphene suitable for radio frequency (rf) applications.[7,9] Various techniques have been used to implement top-gate dielectrics for use in GFETs, including electron-beam physical vapor deposition (EBPVD),[10,11] functionalized atomic layer deposition (ALD),[12−14] seeded ALD (either through use of a thin oxidized metal layer[15,16] or a polymer buffer layer[17]), and other more unconventional techniques.[18,19] While current implementations of the GFET have shown great promise using these techniques, top-gate dielectrics often cause an undesirable degradation in transport properties of the underlying graphene, often reported as a decrease in carrier mobility.[17,20,21] Alternatively, calculations have shown that high dielectric constant (high-κ) materials should have the effect of suppressing charged impurity scattering in the underlying graphene, leading to an increase in carrier mobility.[22,23] Such an increase in carrier mobility has been shown variously by increasing the dielectric constant of a solvent overlayer[24,25] or by use of an ice overlayer,[26] but increase in carrier mobility with deposition of high-κ dielectric by conventional means such as EBPVD, chemical vapor deposition (CVD), or ALD has yet to be experimentally demonstrated. In this Letter, we investigate multiple gate dielectrics for use in GFETs and show that an increase in carrier mobility up to 70% can be achieved with ALD dielectric overlayers utilizing a novel seeding technique where physically evaporated high-κ dielectric seed layers are deposited directly on epitaxial graphene (EG) from a high purity oxide source. Additionally, we show that effective mobility and GFET performance are increased for high-κ seed layers relative to low-κ seed layers and that the presence of heterogeneous seed/overlayer structures can be detrimental to GFET performance.

Epitaxial graphene is grown on the Si face of semi-insulating 6H-SiC (II-VI, Inc.) substrates using low-pressure, Ar-mediated sublimation at 1625 °C.[27] Subsequently, test structures and transistors are fabricated using standard UV photolithography techniques. Van der Pauw (VdP) structures for Hall effect measurements are 5 × 5 μm squares (Figure 1a), while transistors in this work utilize two-finger gates dimensioned 2×(3 × 1) μm or 2×(3 × 1.5) μm ($W \times L$) (Figure 1b,c) with 1 μm source−drain spacing. Source/drain contacts (Ti/Au 10/50 nm) with transfer length values averaging 1 (±0.2) × 10^{-5} cm, and contact resistance values averaging 200 (±100) Ω μm (3 (±2) × 10^{-7} Ω cm^2) are prepared using an oxygen plasma pretreatment as detailed in previous work.[28] Integration of the gate dielectric with graphene is comprised of various steps, with ALD and EBPVD being utilized to prepare either EBPVD seeded ALD films or EBPVD-only films. ALD dielectrics utilize a ∼2−3 nm seed layer of SiO_2, Al_2O_3, or HfO_2 deposited via nonreactive EBPVD at <10^{-6} Torr. Immediately following EBPVD seeding, ∼8−10 nm of Al_2O_3 or HfO_2 is deposited via ALD (Cambridge Nanotech, Inc., "Savannah") to complete the gate stack (Supporting Information). The seeded ALD process in this work can be considered similar to previous work utilizing oxidized metal seeds (metal → metal

Received: April 22, 2011
Revised: July 20, 2011

   dx.doi.org/10.1021/nl201358y | *Nano Lett.* XXXX, XXX, 000–000

oxide),[20,21] but with one important distinction: the seed is deposited directly from a high-purity oxide source. This process, referred to as oxide seeded ALD (O-ALD), omits the metal to metal oxide phase transition of the oxidized metal seeded process (M-ALD), which may be a source of transport degradation in graphene. In addition to seeded ALD dielectrics, we also explore 5 and 10 nm EBPVD dielectrics composed solely of Al_2O_3 or HfO_2. None of the dielectrics are subjected to a postdeposition heat treatment. Table 1 details the composition and thickness of the various gate dielectrics studied, which are schematically illustrated in panels d and e of Figure 1.

Seeding via O-ALD is found to be an effective technique for the nucleation and conformal growth of dielectric films by ALD. Panels f, g, h, and i of Figure 1 are TEM cross sections of O-ALD gate stacks of various seed/overlayer combinations. Figure 1f shows the EG/dielectric interface and indicates that O-ALD processing does not significantly alter the structure of the underlying graphene. Transmission electron microscopy results are supported by Raman spectra taken after deposition of O-ALD dielectrics, which demonstrate negligible change in the D/G peak ratio (Supporting Information). Root mean square (rms) surface roughness of O-ALD dielectrics measured by AFM is found to be 0.84 and 1.7 nm for Al_2O_3/Al_2O_3 and HfO_2/HfO_2 (seed/overlayer), respectively, and 2.4 and 3.2 nm for HfO_2/Al_2O_3 and Al_2O_3/HfO_2, respectively. Increased surface roughness for heterogeneous gate stacks correlates well with TEM results (Figure 1f,g), which show a nonuniform interfacial region between the seed and overlayer. Although TEM results for homogeneous gate stacks (Figure 1f,i) lack the contrast to discern any interface, the 2× reduction in rms surface roughness for these stacks suggests that the presence of a nonuniform seed/overlayer interface is a primary source of increased surface roughness. The presence of interfacial roughness near the graphene channel is expected to lead to interface roughness scattering that could degrade transport properties, while increased surface roughness is anticipated to negatively affect gate leakage uniformity in the GFETs.

Table 1. Composition and Thickness of Investigated Gate Dielectrics

deposition technique	seed layer[a]	seed thickness (nm)	dielectric layer	dielectric thickness (nm)
O-ALD	SiO_2	2	HfO_2	10
O-ALD	HfO_2	2	Al_2O_3	8
O-ALD	HfO_2	2	HfO_2	8
O-ALD	Al_2O_3	2	Al_2O_3	8
O-ALD	Al_2O_3	2	HfO_2	8
EBPVD			HfO_2	5
EBPVD			HfO_2	10
EBPVD			Al_2O_3	5
EBPVD			Al_2O_3	10

[a] Dielectrics deposited by O-ALD utilize an EBPVD deposited oxide seed layer for subsequent growth by ALD, while dielectrics deposited by EBPVD do not.

In order to evaluate the effect of O-ALD deposited dielectrics on carrier transport, Hall effect measurements are made under high vacuum ($<5 \times 10^{-8}$ Torr) at 300 K in a ± 0.5 T magnetic field *prior to* and *following* deposition of the gate dielectric. Hall effect measurements allow direct sampling of carrier density and Hall mobility and have the advantage of removing any uncertainty due to the accurate measurement of back or top gate capacitances, which is important for the case of top-gated graphene.[29] Samples are annealed in situ at 400 K for 60 min before measurement in order to ensure desorption of water or other contaminants from the surface of the graphene, preventing any extrinsic doping of the EG except that caused by the gate dielectric or the substrate. Prior to deposition of an O-ALD dielectric, as-grown samples (Figure 2a) exhibit Hall mobility (μ_{Hall}) values of 700−1100 $cm^2/(V \cdot s)$ and carrier concentration (n_s) values of $(5 - 8) \times 10^{12}$ cm^{-2} (n-type), typical of Si-face EG.[30,31] From Figure 2a, we see that as-grown samples appear to follow a $\mu_{Hall} \propto n_s^{-1}$ trend (gray shaded region), which has been previously reported for Si-face EG.[30] Although it is unclear whether this trend is due only to a change in carrier concentration or also a change in sample quality, gated Hall effect

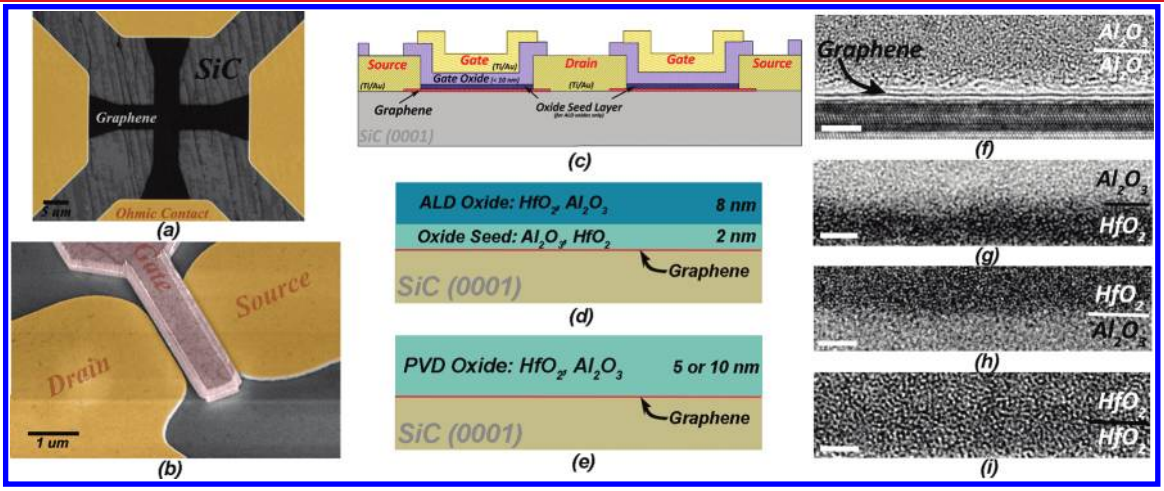


Figure 1. Scanning electron micrographs of a graphene Van der Pauw test structure (a) provide a means to extract carrier transport properties prior to and following dielectric deposition. Subsequently graphene FETs (b, c) that utilize atomic layer deposited (d) or e-beam physical vapor deposited (e) gate dielectrics are fabricated to evaluate device performance. TEM micrographs show the interface between oxide seed and ALD dielectric for Al_2O_3/Al_2O_3 (f), HfO_2/Al_2O_3 (g), Al_2O_3/HfO_2 (h), and HfO_2/HfO_2 (i) gate stacks, where heterogeneous O-ALD films (g) and (h) display a rough interfacial region. The scale bar is 3 nm.

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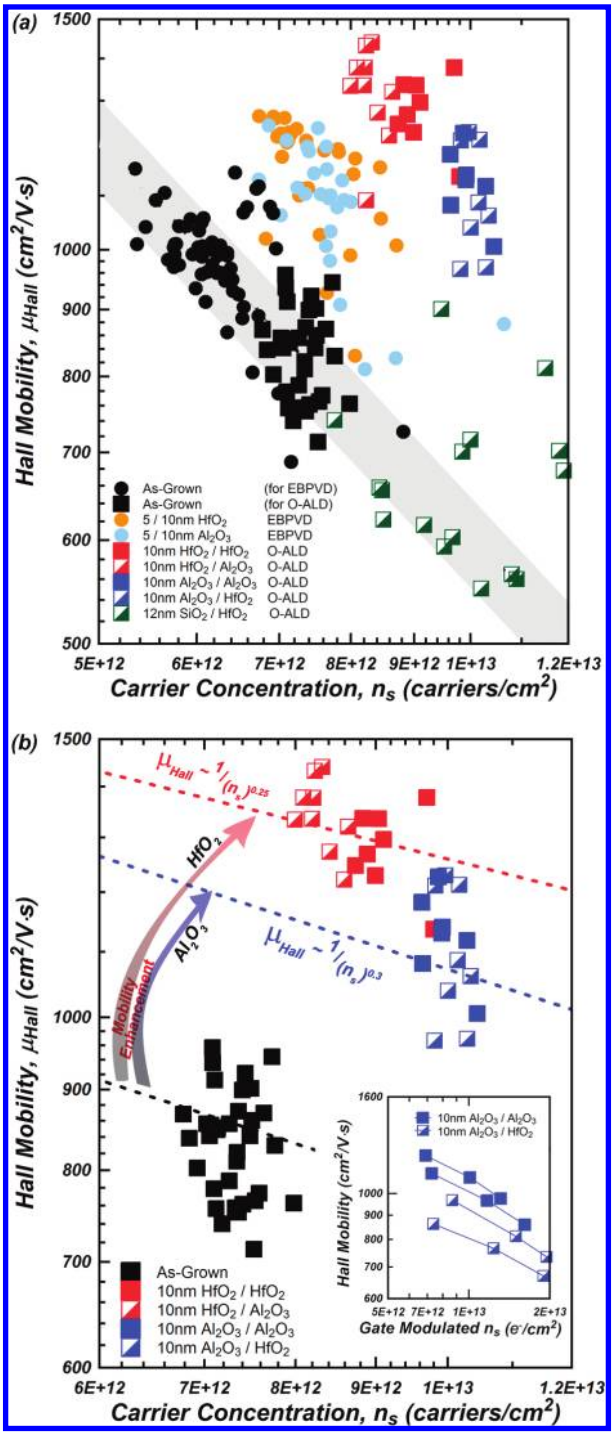

Figure 2. Evaluation of μ_{Hall} and n_s (a) indicates that deposition of high-κ dielectrics by O-ALD and EBPVD can lead to improved μ_{Hall} through dielectric screening. Gated Hall effect measurements (b, inset) reveal a dependency for μ_{Hall} and gate modulated carrier concentration, n_s, where $\mu_{Hall} \propto n_s^{-X}$ and X ranges from ~0.2 to 0.3. The measured dependencies for the HfO_2/HfO_2 and Al_2O_3/Al_2O_3 samples are plotted along with Hall effect data for the O-ALD and corresponding as-grown samples (b).

measurements of O-ALD coated samples (Figure 2b) reveal a μ_{Hall} dependency on gate modulated carrier concentration of $\mu_{Hall} \propto n_s^{-X}$, where X ranges from ~0.2 to 0.3.

Both measured and observed dependencies confirm that an increase in n_s after deposition of dielectric should lead to a subsequent decrease in μ_{Hall}, unless deposited dielectrics also act to modify the scattering physics within the graphene. In this work, all dielectrics are found to cause an increase in n_s, which can be attributed to the presence of oxygen vacancies or other charged defect complexes that dope the graphene through a charge transfer process.[20,32] Although all dielectrics cause an increase in n_s not all dielectrics subsequently cause a decrease in μ_{Hall}. Figure 2a shows that high-κ seeded dielectrics deposited by EBPVD and O-ALD result in an increase in n_s *and* an increase in μ_{Hall}, similar to the case of high-κ solvents on exfoliated graphene.[24] Conversely, low-κ seeded dielectrics deposited by O-ALD lead to a decrease in μ_{Hall} and increase in n_s. The measured increase of μ_{Hall} with deposition of high-κ seed is attributed to dielectric screening,[22−26] signifying a reduction in scattering by remote charged impurities, and represents the first time such an increase has been observed using conventional deposition techniques on EG. As illustrated in Figure 2, HfO_2 seeded O-ALD dielectrics enhance carrier mobility by an estimated 57−73%, while Al_2O_3 seeded O-ALD dielectrics increase mobility by 43−52%, and EBPVD dielectrics increase mobility by ~15% (Supporting Information). We note that the measured change in mobility with O-ALD dielectrics is lower than that predicted by theory, where Al_2O_3/Al_2O_3 (ε_r ~7)[33] and HfO_2/HfO_2 (ε_r ~ 16)[33] on a SiC substrate (ε_r ~ 10; 6H polymorph)[34] should result in a 1.6× and 2.5× increase in μ_{Hall}, respectively,[24,35] which may be a result of a high density of charged defects within the dielectrics.

The presence of fixed charge or charged defects within the dielectrics is a likely source of remote charged impurity scattering, which could act to mask the benefits of enhanced dielectric screening. This is evident when comparing μ_{Hall} for EBPVD dielectrics to O-ALD, where EBPVD dielectrics typically contain higher intrinsic defect concentrations. The dependency of μ_{Hall} on film thickness found for EBPVD films (Supporting Information) supports the presence of such charge. This phenomenon has also been observed for M-ALD dielectrics on exfoliated graphene,[20] where a decrease in mobility is attributed to an increase in the charged impurity concentration with increasing thickness due to a charge transfer process between the graphene and oxygen vacancies within the dielectric. While no true mobility *decrease* is found for EBPVD deposited dielectrics in this work, we note that this is likely due to the lower intrinsic mobility of the EG system (μ ~ 1000) as compared to the exfoliated graphene on SiO_2 studied by Fallahazad et al. (μ ~ 10000).[20] Additionally we note that Fallahazd et al. make use of a heterogeneous seed/overlayer structure,[20] which may also lead to reduced mobility.

Hall effect measurements for O-ALD and EBPVD dielectrics clearly indicate that successful integration of a top-gate dielectric is possible without disrupting the transport properties of EG and that proper choice and deposition of dielectrics are critical in optimizing the performance of top-gate dielectrics on EG. However, in addition to optimizing the effect of the overlayer on transport properties, the choice of material and deposition technique must produce top-gates that satisfy the main functions of a gate dielectric, which are to sufficiently isolate the channel from the gate and to capacitively couple the gate to the channel. Table 2 summarizes the ability of the investigated dielectrics to perform these tasks, showing maximum leakage currents during $I_{ds} - V_{gs}$ sweeps, C_{ox}/q, β, and n_0, where β is defined as $n_s \cong \beta V_{gs} + n_0$ with n_s as the carrier density in the channel, V_{gs} as the applied gate bias, and n_0 as the carrier density at zero-bias conditions.

dx.doi.org/10.1021/nl201358y |*Nano Lett.* XXXX, XXX, 000–000

Table 2. Gate Leakage and Carrier Modulation for O-ALD Gates of Varying Seed/Overlayer Combination

seed/dielectric combination	I_{leak} @ V_{gs} = 3 V (A/μm^2)	C_{ox}/q (e$^-$/V × 10^{12})	β^a (e$^-$/V × 10^{12})	$n_0{}^b$ (e$^-$/cm^2)
HfO_2/HfO_2	5.6×10^{-12} to 8.4×10^{-12}	7.5	2.12	5.5×10^{12}
HfO_2/Al_2O_3	1.7×10^{-11} to 6.7×10^{-7}	6.3	1.43	5.6×10^{12}
Al_2O_3/Al_2O_3	4.4×10^{-12} to 7.3×10^{-12}	5.0	1.57	7.2×10^{12}
Al_2O_3/HfO_2	5.8×10^{-12} to 8.8×10^{-12}	5.6	2.27	8.2×10^{12}

[a] β is defined as the dependency of the gate modulated carrier concentration on the applied gate bias ($n_s \cong \beta V_{gs} + n_0$, where n_s is the carrier density in the channel, V_{gs} is the applied gate bias, and n_0 is the carrier concentration at V_{gs} = 0 V). β is extracted from gated Hall effect measurements in air at room temperature. β is reduced roughly 60−80% from expected (C_{ox}/q) values, strongly indicating the presence of a high density of charge traps in the dielectrics. [b] n_0 (carrier concentration) is measured by the Hall effect in air at room temperature with V_{gs} = 0 V.

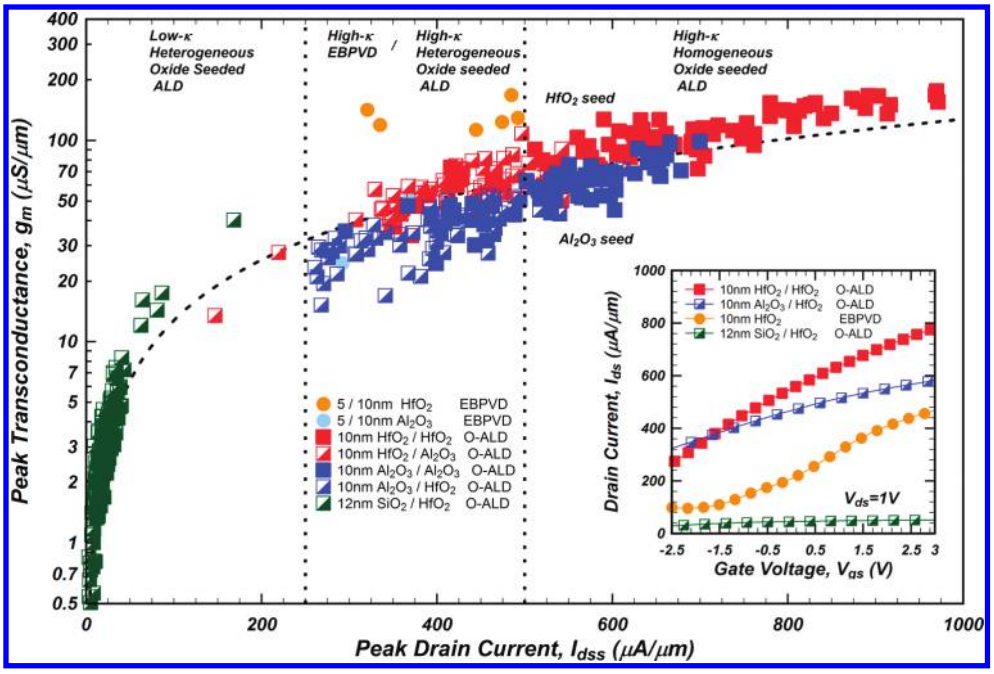

Figure 3. Plot of peak transconductance versus peak drive current for over 500 GFETs utilizing gate dielectrics deposited by EBPVD and O-ALD techniques. Homogeneous high-κ seeded O-ALD gate dielectrics produce the highest performance GFETs (rightmost portion of the plot) attributed to improved dielectric screening relative to low-κ O-ALD gates, lower defect concentrations relative to EBPVD gates, and reduced interface roughness scattering relative to heterogeneous O-ALD gates. The inset shows transfer curves for four representative GFETs, providing clear evidence of enhanced performance with high-κ dielectrics.

While the majority of the O-ALD gate stacks average 5×10^{-12} to 8×10^{-12} A/μm^2, leakage currents for O-ALD HfO_2/Al_2O_3 gates exhibit significant variability, ranging from 2×10^{-11} to 7×10^{-7} A/μm^2 (V_{gs} = 3 V), which is attributed to a high rms roughness relative to others. Low leakage currents for the O-ALD dielectrics confirm oxide seeding as a robust functionalization technique ensuring uniform coverage of ALD dielectrics. Most gate stacks exhibit hard breakdown of 4−9 MV/cm with little correlation to composition or deposition technique. For breakdown at this field strength, B-mode failure is expected[36] and suggests the presence of dielectric thinning, confirming AFM results indicating thickness variability on the order of ±2 nm. Additionally, we note that the measured dependency of n_s on V_{gs} is significantly less than that anticipated by measurements of C_{ox} indicating the presence of charge traps in the gate dielectric.[37,38]

Direct current (dc) measurements of GFETs utilizing O-ALD and EBPVD gate dielectrics are compared and confirm the benefits of high-κ EBPVD and O-ALD as techniques for optimizing GFET performance. Figure 3 plots peak transconductance ($g_{m,max}$) and peak drive current, I_{dss} (I_{ds} @ V_{gs} = 3 V, V_{ds} = 1 V), extracted from $I_{ds} - V_{gs}$ sweeps for more than 500 devices, while Figure 3-(inset) plots representative transfer curves for four GFETs utilizing the different gate dielectrics.[39] GFETs utilizing low-κ SiO_2 seeded O-ALD gates (Figure 3; left-most section) exhibit average I_{dss} < 50 μA/μm and average $g_{m,max}$ < 10 μS/μm and represent the lowest performance dielectric in this work. Low I_{dss} and $g_{m,max}$ for SiO_2 seeded O-ALD is attributed to reduced mobility relative to high-κ seeded gates (Figure 2a). Additionally, high contact resistances (R_c) were found for this sample, where the oxygen plasma pretreatment was omitted. For all other samples, the use of plasma pretreatment reduces R_c to less than 200 Ω μm, making contact resistance negligible under depletion conditions and roughly 20% of the total resistance under accumulation. For the case of SiO_2 seeded GFETs, it is anticipated that reduction of R_c should lead to a shift in the average I_{dss} and $g_{m,max}$ closer to 100 μA/μm and 20 μS/μm in accord with the highest performing SiO_2 seeded GFETs. On the other hand, GFETs utilizing *high-κ* EBPVD or *high-κ* seeded heterogeneous O-ALD gates (Figure 3, middle section) show a 3−4× increase in I_{dss} to 340−440 μA/μm and $g_{m,max}$ to 40−70 μS/μm,

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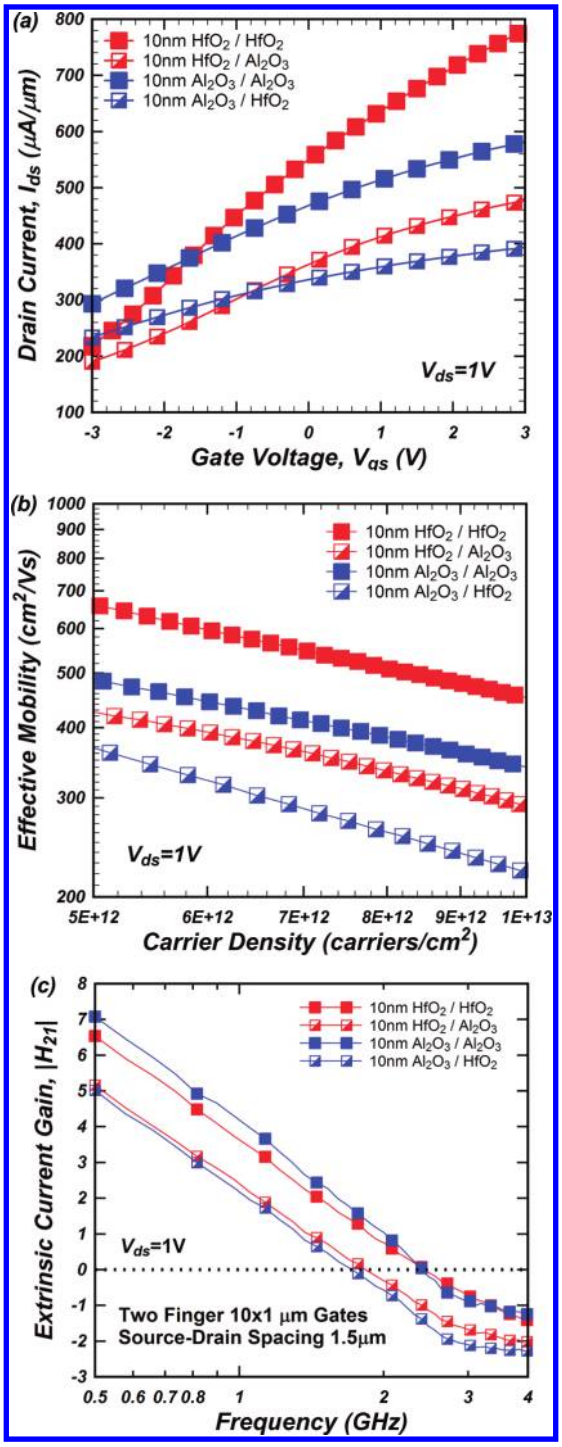

Figure 4. Transfer curves of four representative GFETs utilizing high-κ O-ALD gates (a) illustrating increased I_{dss} and $g_{m,max}$ for GFETs utilizing homogeneous gate stacks. Extracted μ_{eff} plotted as a function of n_s (b) confirms a degradation in μ_{eff} of 30−40% for GFETs with heterogeneous O-ALD gate dielectrics. Finally, *extrinsic* small signal current gain as a function of frequency for GFETs (c) demonstrates that rf performance follows a similar trend to dc FET performance, where heterogeneous composition gate dielectrics lead to lower f_T.

with 5 nm EBPVD HfO_2 gated GFETS displaying $g_{m,max}$ up to 140 μS/μm. Homogeneous O-ALD gated GFETs (Figure 3, right-most section) exhibit exceptional FET characteristics with average I_{dss} = 550−780 μA/μm and average $g_{m,max}$ = 66−134 μS/μm depending on gate composition. Of the homogeneous O-ALD gated GFETs, HfO_2/HfO_2 GFETs are found to be superior to all others with I_{dss} up to 971 μA/μm and $g_{m,max}$ up to 175 μS/μm. The increase in performance for GFETs utilizing high-κ EBPVD and high-κ O-ALD dielectrics is attributed to a reduction of remote charged impurity scattering through dielectric screening, leading to increased carrier mobility. The superior performance of homogeneous O-ALD gated GFETs relative to heterogeneous O-ALD is attributed to removal of the seed/overlayer interface which is thought to negatively affect carrier transport in the channel through increased interface roughness scattering. We note that transfer curve hysteresis in O-ALD GFETs ranges from 0.5 to 0.7 V with no statistically significant trending according to gate composition. Additionally, we find an increase in hysteresis for EBPVD gates to 1 V, which is in agreement with a higher density of charge traps. The passivation or reduction of these traps by thermal processing or optimized reactive depositions is anticipated to significantly reduce hysteresis.

The difference in performance between homogeneous and heterogeneous high-κ seeded O-ALD gated FETs (Figure 3a,b) highlights a key consideration for gate dielectric implementation: the effect of seed/overlayer interface on carrier transport. Figure 4a shows representative transfer curves for O-ALD gated GFETs of varying seed/overlayer composition. Evident from Figure 4a, heterogeneous gate dielectrics lead to a decrease in I_{ds} of more than 30% compared to homogeneous gate dielectrics. The absolute difference in average (postdielectric) μ_{Hall} and n_s between samples with the same oxide seed is <4% (Figure 2a) and does not provide sufficient explanation for the differences found in I_{ds}. Alternatively, the effective mobility (μ_{eff}) of the GFETs can be extracted using a simple charge control model: $J_{ds} = \mu_{eff}(C_{ox}/A)(V_{gs} - V_{NP})V_{ds}$, where J_{ds}, is drain current normalized by width, $(C_{ox})/(A)$ is the gate capacitance normalized by area, V_{gs} is the applied gate bias, V_{NP} is the neutrality point (NP), and V_{ds} is the driving voltage.[7] In this work, we have modified the charge control model to become $J_{ds} = \mu_{eff}(\beta V_{gs} + n_0)V_{ds}$, where n_0 is the measured intrinsic n_s at zero-bias conditions (Table 2) and β relates the charge carrier density to the applied gate bias (Table 2) and is extracted from gated Hall effect measurements. The modified model alleviates the V_{NP} constraint by directly sampling the carrier concentration at zero-bias conditions and uses gated Hall effect measurements in place of C_{ox} to make a more accurate estimation of carrier density in the channel in the presence of a large number of traps and any quantum capacitance effects. The model does not address contact resistance, although R_c was found to be uniform between the high-κ seeded O-ALD samples. Figure 4b plots μ_{eff} as a function of n_s and provides evidence that the degraded performance of heterogeneous dielectric GFETs is the result of an approximate 40−30% degradation in μ_{eff} compared to homogeneous gate stacks. We speculate that interface roughness scattering has a great impact on GFET measurements while only minimally impacting Hall effect measurements. The strong dependency of interface roughness scattering on carrier energy,[40] yet weak dependency of remote charged impurity scattering on carrier energy[40] help to explain why the overall contributions of these two scattering processes could change significantly between Hall effect and dc FET characterization at high drain biases.

Similar to dc performance of GFETs, the presence of a seed/overlayer interface is found to impact the small signal *extrinsic* current gain, $|H_{21}|$. Figure 4c plots $|H_{21}|$ as a function of frequency

dx.doi.org/10.1021/nl201358y |*Nano Lett.* XXXX, XXX, 000–000

for O-ALD gated GFETs biased close to peak transconductance. Clearly evident in Figure 4c, homogeneous gate stacks outperform heterogeneous gate stacks and demonstrate *extrinsic* $f_T > 2$ GHz at $V_{ds} = 1$ V and up to 4.9 GHz at $V_{ds} = 3$ V. The excellent *extrinsic* rf performance of the O-ALD gated GFETs is attributed to improved mobility relative to other dielectric deposition techniques and low contact resistance. On the basis of dc performance, we expect superior *extrinsic* rf performance for homogeneous HfO_2/HfO_2 gated GFETs; however, the results indicate similar performance for both $HfO_2/HfO_2$and Al_2O_3/Al_2O_3 seeded GFETs. We speculate that this is the result of device processing variation between samples. Ideally, the measured f_T should be a measure of mobility; however, *extrinsic* GFET measurements like those presented in this work will deviate from direct measurement due to parasitic capacitances and resistances, which may vary due to processing variation. None-the-less, we have clearly demonstrated that the presence of a heterogeneous dielectric in GFETs can significantly degrade both dc and rf performance.

We have considered several factors for integrating dielectrics with EG for device applications including the importance of choice of seed layer on transport properties and FET performance, as well as the effect of seed/overlayer interfaces on dc and rf FET performance. High-κ EBPVD and O-ALD dielectrics have been investigated and shown to improve μ_{Hall} by reducing remote charged impurity scattering through dielectric screening. Additionally, GFETs utilizing high-κ EBPVD and O-ALD gates have been demonstrated and show dramatic performance improvements relative to GFETs utilizing low-κ O-ALD gates. Finally, the work presented here serves as a building block for improved dielectric gate stack engineering on EG and may lead to improved and technologically viable graphene based technologies for use in radio frequency applications

■ ASSOCIATED CONTENT

Supporting Information. ALD growth of dielectric overlayers, Raman analysis of graphene pre/postdielectric, detailed fitting of Hall effect data with gated Hall measurements used to estimate percent increase in Hall mobility, thickness dependence of n_s and μ_{Hall} for EBPVD films, and detailed extraction of effective mobility. This material is available free of charge via the Internet at http://pubs.acs.org.

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■ ACKNOWLEDGMENT

The authors thank D. Tomich and T. Cooper of The Air Force Research Lab for assistance with Hall mobility measurements. M. J.H. acknowledges support from the II-VI Foundation. Additionally, support for the Cambridge ALD System, WiteC Raman system, and JEOL 2010F TEM was provided by the National Nanotechnology Infrastructure Network at Penn State. This work was supported by the Naval Surface Warfare Center Crane, Contract No. N00164-09-C-GR34.

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