A Low-Voltage Low-Power *LC* Oscillator Using the Diode-Connected SymFET

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***Abstract*—In this paper, a low-voltage low-power *LC*-tank oscillator design using the symmetric graphene tunneling field-effect transistor (SymFET) diode is presented. The SymFET takes advantage of the resonant current tunneling through two graphene layers, with a large current peak exhibiting negative differential resistance (NDR) when the drain-to-source voltage aligns the Dirac point. A Verilog-A SymFET model is presented with noise performance for circuit design and evaluation. The NDR phenomenon of the diode-connected SymFET is further explored, and oscillator design considerations are discussed for performance optimization. Simulation results show that the proposed SymFET 3.05 GHz oscillator has a simulated phase noise of -117 dBC/Hz at 1.0 MHz offset, with a power consumption of only 0.23 mW from a 0.30 V supply.**

Keywords—low-power; low-voltage; negative differential resistance; oscillator; phase noise; SymFET

I. INTRODUCTION

For the purpose of further device miniaturization and power consumption reduction, emerging devices with the potential of being alternatives to conventional complementary metal-oxide-semiconductor (CMOS) transistors have been actively explored [1][2]. Recently, a symmetric tunneling field-effect transistor (SymFET) of a graphene-insulator-graphene (GIG) structure has been presented [3][4]. This device shows a large resonant tunneling current when the Dirac points are aligned in a particular drain-to-source bias range. The SymFET on/off current ratio increases with the graphene coherence length and doping, and thus provides an opportunity to achieve much higher power efficiency than current electronic logic devices. It is also anticipated that SymFET is a good candidate for high-speed analog applications like frequency multiplication. For comprehensive evaluation, it is essential to explore possible SymFET analog/RF applications.

In this paper, we focus on the negative differential resistance (NDR) of the SymFET resonant tunneling current to obtain possible analog/RF applications. Fig. 1 illustrates the SymFET I_D-V_G-V_{DS} curve. It is important to notice that NDR occurs in both V_G and V_{DS} orientations, and is insensitive to insulator thickness and dielectric constant variations [3]. Such unique characteristics differ from conventional FETs, thus enabling SymFETs to be used in a whole new range of potential applications. Section 2 discusses these characteristics with more details.

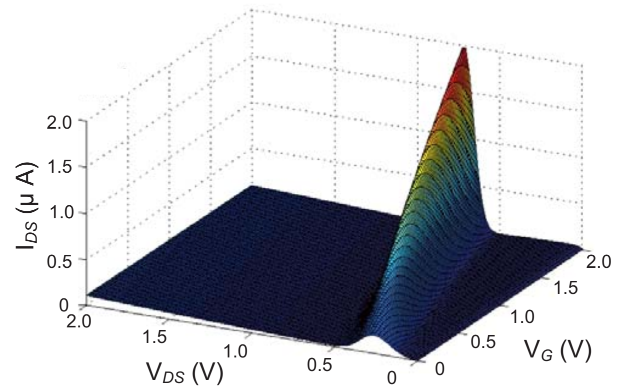

Fig. 1. Typical SymFET I_{DS}-V_G-V_{DS} curve showing NDR characteristics.

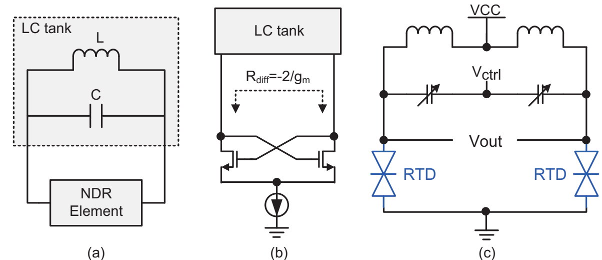

Fig. 2. Oscillators based on NDR. (a) Resistive loss compensation using NDR element; (b) CMOS oscillators using a coupled feed-back pair as an NDR element; (c) RTD oscillators.

NDR has been widely employed in amplifiers and LC oscillators. In amplifiers, the overall output impedance can be significantly increased by substituting the load of the amplifier output stage by a feed-back differential pair with negative resistance [5]. Such a feed-back pair can also be applied in oscillators to compensate the energy loss in the oscillator, as shown in Fig. 2(a-b) [6]. Resonant tunneling diodes (RTDs) have also been found to maintain NDR characteristics to enable oscillation as shown in Fig. 2(c) [7]-[10].

In this paper, the NDR characteristic of SymFET is explored in LC oscillators. The contributions of this paper mainly include two aspects:

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a) A Verilog-A SymFET model is generated based on [3]. We also integrate it with the parasitic capacitance, and build its noise model. The existing SymFET model in [3] has strict terminal voltage requirements. In this paper, a diode-connected SymFET is proposed to satisfy such requirements by configuring the SymFET as a two-terminal device, of which the NDR is explored for the first time.

b) The diode-connected SymFET oscillator is developed and simulated, and its power, frequency range, and phase noise performance are also discussed and compared with other types of oscillators, showing that the diode-connected SymFET oscillator is a promising candidate for low-voltage low-power applications.

In the rest of this paper, Section 2 will introduce the SymFET model, the diode-connected SymFET, and their characteristics. Section 3 will introduce the proposed diode-connected SymFET oscillator, design considerations, and performance. Section 4 will give the conclusion.

II. SYMFET AND DIODE-CONNECTED SYMFET

A. SymFET Analytical Model

The SymFET has a device structure as shown in Fig. 3, in which a GIG structure is sandwiched between the top gate and the bottom gate [3]. The two n-type and p-type graphene layers represent the source (S-terminal) and drain (D-terminal) of the transistor, respectively. The voltages of the top gate and the bottom gate, i.e. V_{TG} and V_{BG}, are used to control the quasi-Fermi levels of the top and bottom graphene layers to be ΔE above/below the Dirac point in the top/bottom graphene layer, respectively. When the drain-source voltage V_{DS} equals $2\Delta E/q$, where q represents the single electron charge, the two Dirac points align and electrons at all energies between the quasi-Fermi levels satisfy the energy and momentum conservation, and thus a large tunneling current occurs. When $V_{DS}\neq 2\Delta E/q$, however, the tunneling current is much smaller because only a single energy in the Dirac cone meets requirement of the simultaneous energy and momentum conservation [3].

In the analytical model in [3], providing satisfied terminal voltage requirement (neglecting the DC voltage offset on the terminals) of

$$V_{TG} = -V_{BG} = V_G, V_D = -V_S, \tag{1}$$

the drain-to-source current I_{DS} could be model as [3]

$$\begin{aligned} I = & \underbrace{G_1 \left| V_{DS} - \frac{2\Delta E}{q} \right| \tanh\left(\frac{qV_{DS}}{4k_B T}\right) \tanh\left(\frac{LqV_{DS}}{\pi\hbar v_F}\right)}_{I_1} \\ & \underbrace{+ T_{coeff} \frac{1.6G_1}{\sqrt{2\pi}} \frac{L\Delta E^2 (2u_{11}^4 + u_{12}^4)}{u_{12}^4 q\hbar v_F} \exp\left[-\frac{L^2}{4\pi}\left(\frac{qV_{DS} - 2\Delta E}{\hbar v_F}\right)^2\right]}_{I_2}, \end{aligned} \tag{2}$$

where the terms I_1 and I_2 represent the misaligned non-resonant tunneling current and the aligned resonant tunneling current, respectively. In Eq. (2), T_{coeff} is the temperature coefficient, and G_1 is the pre-factor conductance which could be modeled as

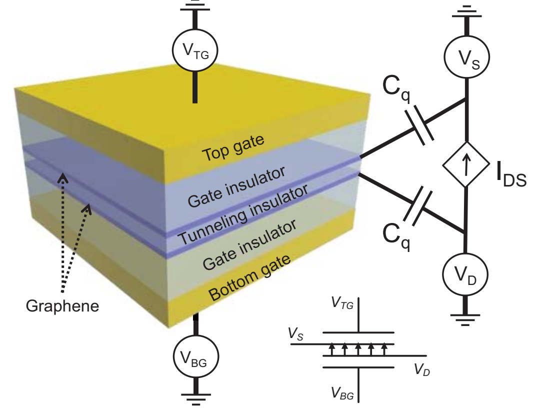

Fig. 3. Sketch of the SymFET [3].

TABLE I. DEFINITIONS AND DEFAULT VALUES OF THE TERMS IN THIS PAPER

Terms	Definitions
k_B	Boltzmann constant
$\hbar$	Reduced Planck constant
v_F	Fermi velocity in graphene, $v_F \approx$1.0e6 m/S
u_{11}, u_{12}	Constant of order unity, $u_{11}= u_{12}=1$
κ	Decay constant for tunneling current in the barrier, set as κ=6.1nm^{-1}.
d	Normalization constant for the graphene z-component wavefunction, d ≈ 0.335 nm
m	Free electron mass
t_t	Tunneling insulator thickness, t_t=1.34 nm
t_g	Gate insulator thickness, t_g=5.0 nm
ε_g	Permittivity for the gate dielectric, $\varepsilon_g=3.9\varepsilon_0$
ε_t	Permittivity for the tunnel dielectric, $\varepsilon_t=3.9\varepsilon_0$

$$G_1 = \frac{q^2 L^2}{2\hbar}\left(\frac{\hbar\kappa u_{12}^2 e^{-\kappa t_t}}{m d v_F}\right)^2. \tag{3}$$

The definitions and values of other terms to calculate I_{DS} using Eq. (2)-(3) are listed in Table I. By sweeping V_G and V_{DS}, the I_{DS}-V_G-V_{DS} curve could be generated, as shown in Fig. 1.

It is important to notice that the graphene coherence length L is not equal to the graphene sheet length when structural imperfections exist [11]. Also, if the graphene sheet is composed of M perfect areas, each with area of l^2, then the total tunneling current would be given by M times the current in Eq. (2) with $L=l$.

B. Proposed SymFET Verilog-A Model

Based on the drain-to-source current in Eq. (1), we present a Verilog-A SymFET circuit model which supports DC, transient and also noise simulations. Fig. 4 shows the circuit model. The quantum capacitance C_q is modeled as

$$C_q = \frac{2|\Delta E|}{\pi(\hbar v_F / q)^2}, \tag{4}$$

where v_F is the Fermi velocity in graphene, and $\hbar$ is the reduced Planck constant [3]. Because calculating the temperature coefficient T_{coeff} in Eq. (2) is very time-consuming, the Verilog-A model builds a V_G-V_{DS}-I_{DS} look-up table for acceleration. This look-up table is dense enough so that the interpolating error during simulations is negligible (< 0.01% in this paper).

In the SymFET circuit model, we also model the impact of noise. Three types of typical noise are integrated into the Verilog-A SymFET model, including thermal noise, shot noise, and low-frequency $1/f$ noise. The thermal noise is dominated by the temperature and the drain-to-source resistance, and is modeled as

$$\overline{I_{DS,\,\text{thermal noise}}^{\;2}} = 4k_B T G_{DS}, \tag{5}$$

where G_{DS} represents the drain-to-source conductance. The shot noise is modeled as

$$\overline{I_{DS,\,\text{shot noise}}^{\;2}} = 2q|I_D|. \tag{6}$$

The third type of noise, i.e. low-frequency $1/f$ noise, is crucial for the diode-connected SymFET VCO, in which the nonlinear up-conversion of low-frequency $1/f$ noise during the oscillations limits the VCO phase noise performance [12]. Based on the SymFET stacking structure and the sequential electron flowing path, graphene noise and tunneling noise are two sources of the low-frequency $1/f$ noise that need to be considered for SymFET. It is generally reported that the $1/f$ graphene noise is attributed to fluctuations in mobility, which can arise from the traps/impurities associated with oxide substrates/insulators [13]-[17]. Published measurement reports on the low-frequency $1/f$ noise of single-layer graphene can be characterized as

$$\frac{S_I}{I^2} = n \times 10^{-7} \times \frac{1}{f \times A}, \tag{7}$$

where f represents frequency in Hz, A represents the channel area in µm^2, and n is in the range of 1~10 [15]. In the Verilog-A SymFET model, the $1/f$ graphene noise spectral density is modeled as Eq. (7) with n=5.

The $1/f$ tunneling noise is compared with $1/f$ noise in similar conductor-insulator-conductor structures (e.g. Josephson tunneling junctions). Such structures and SymFET are the same in that $1/f$ noise can both arise from the slow filling and emptying of localized electron states in the tunneling barrier, which leads to changes in the local tunneling barrier and thus the tunneling current [18][19]. It is reported that $1/f$ noise in the metal-insulator-metal tunnel junction is more than two orders of magnitude less than Eq. (7) [18]. Therefore, we model the SymFET $1/f$ noise by considering only the dominant graphene $1/f$ noise.

C. Proposed Diode-Connected SymFET

As introduced above, the terminal voltage requirement in Eq. (1) makes the SymFET analytical model inconvenient for the simulations of 3-terminal transistor applications, in which such requirement could hardly be satisfied. However, configuring the SymFET to be a 2-terminal diode ensures that the terminal voltage requirement is always satisfied. To get this diode-connected SymFET, we configure the SymFET by connecting the top-gate port to the drain port, and also connecting the bottom-gate port to the source port. Fig. 5(a) illustrates the diode-connected SymFET.

Using the model described above, we obtain the I_{DS}-V_{DS} curves of the diode-connected SymFET with different parameter values (gate insulator thickness t_g, tunneling insulator thickness t_t, coherence length of graphene layers L),

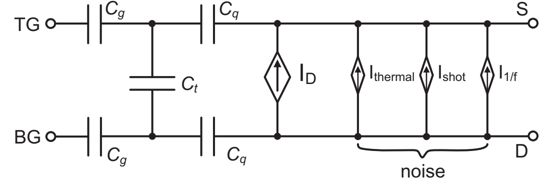

Fig. 4. SymFET circuit model.

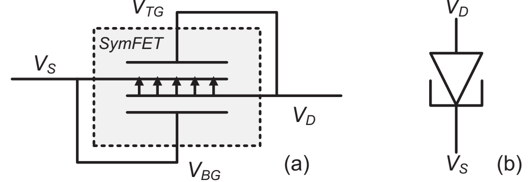

Fig. 5. Diode-connected SymFET: (a) Configuration; (b) Symbol.

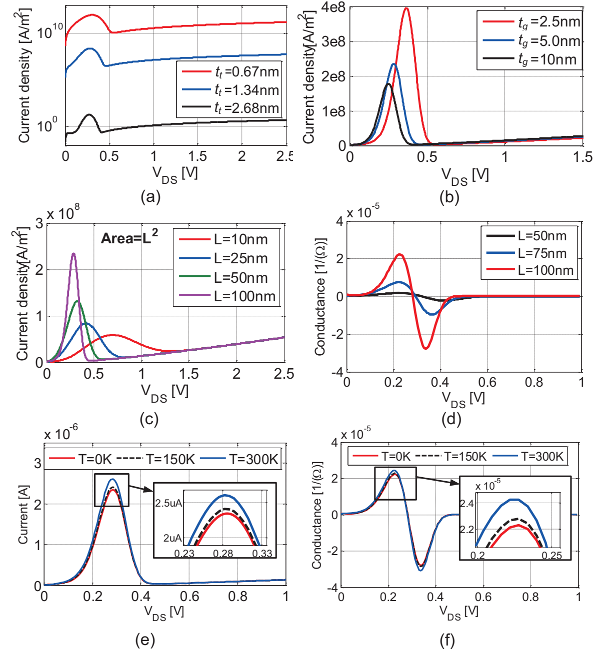

Fig. 6. IDS-VDS and conductance-VDS of diode-connected SymFET with varying parameters of tunneling insulator thickness in (a), gate insulator thickness in (b), coherence length L in (c-d), and temperature in (e-f).

as shown in Fig. 6(a-c). One exciting feature of the diode-connected SymFET is possible NDR region with V_{DS} <0.5 V and large range of adjustable I_{DS}, which is promising for low-voltage low-power applications. Fig. 6(a-b) shows that tunneling current increases by reducing the insulator thickness. If the coherence length L is increased, the tunneling current peak increases, the width of the peak reduces, and the NDR range shifts to a lower V_{DS} bias with narrower range. Fig. 6(d) shows the differential resistance with varying V_{DS} bias and fixed L (=100 nm), which clearly shows a highly nonlinear characteristic.

Another feature of the diode-connected SymFET is the NDR robustness against variations of temperature, insulator thickness and device size, which can also be seen from Fig. 6. As the gate insulate thickness t_g, tunneling insulator thickness t_t, the device coherence length L, or the temperature changes, the NDR does not vanish.

III. PROPOSED OSCILLATOR USING DIODE-CONNECTED SYMFET

This section presents the proposed VCO based on the diode-connected SymFET. Circuit topology, power consumption, frequency range, and phase noise performance are discussed. Circuit simulations results using Cadence Virtuoso based on the Verilog-A model are also provided.

A. Topology

Fig. 7(a) illustrates the proposed basic VCO topology with differential output, where R_s represents the resistance in the power supply line (for simulations), C_v represents the capacitively-coupled varactors. The two diode-connected SymFETs in Fig. 7(a) have the same parameters, operating as negative differential resistance components to compensate the losses associated with the LC tank. Differential mode oscillation is not obligatory but help to resist against power supply and ground noise. For a first order approximation, the expression of the oscillation frequency f_{osc} can be derived:

$$f_{osc} \approx \frac{1}{2\pi\sqrt{L_v(C_v + C_{DS})}}, \tag{8}$$

where C_{DS} represents the intrinsic capacitance of each diode-connected SymFET.

The employed diode-connected SymFET has a gate insulator thickness of 5.0 nm with ε_g = 3.9ε_0, leading to a capacitance of $C_g = \varepsilon_g/t_g \approx 6.9\times10^{-6}\ fF/nm^2$. The tunneling insulator in each SymFET diode is set to be 1.34 nm, which corresponds to four layers of hexagonal boron nitride (h-BN) and a capacitance of $C_t = \varepsilon_t/t_t \approx 2.6\times10^{-5} fF/nm^2$. The coherence length L of the graphene layers is set to be L = 100 nm, and the total tunneling area is 2 µm × 2 µm. Setting the tunneling area to be micrometer-scale helps to reduce the $1/f$ low-frequency noise (see Eq. (7)) and thus the phase noise. On the other hand, keeping the coherence length L to be around 100 nm helps to keep a large V_{DS} range with sufficient NDR effect.

The other parameters of the diode-connected SymFET are summarized in Table. I. Fig. 7(b) plots a typical simulated transient differential output waveform oscillating at 3.05 GHz

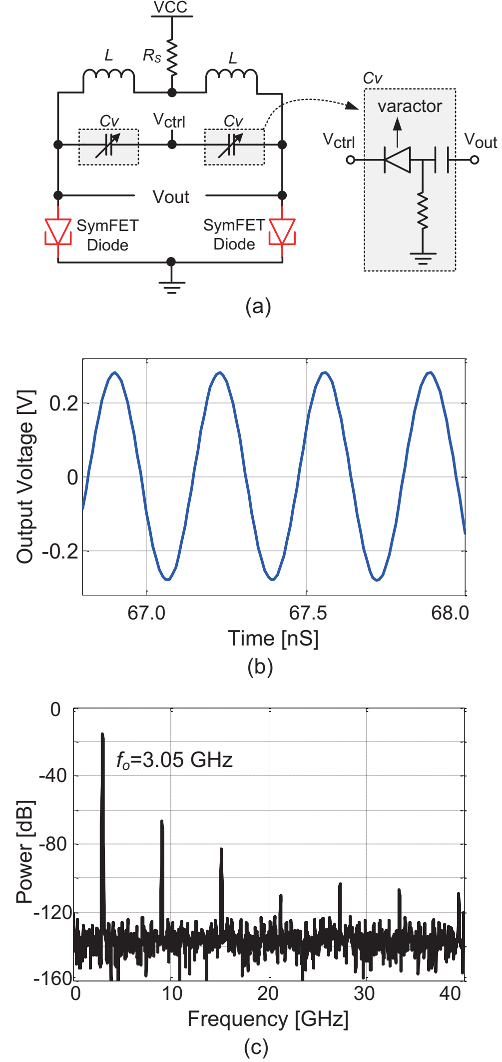

Fig. 7. The proposed diode-connected SymFET oscillator: (a) Topology; (b) Typical transient output (fO=3.05 GHz, VCC=0.30 V); (c) Output spectrum of (b).

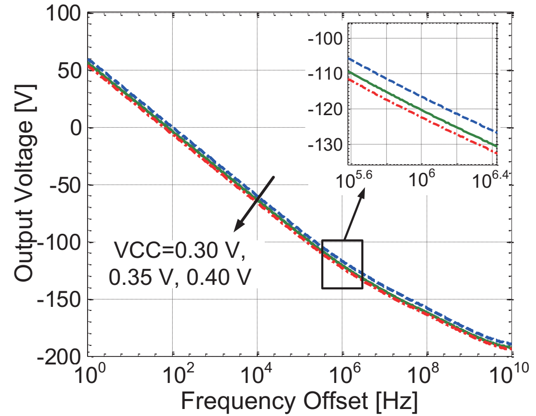

Fig. 8. Simulated phase noise of the proposed diode-connected SymFET oscillator.

with a power supply of VCC=0.30 *V*, along with the spectrum plot in Fig. 7(c).

B. Supply Voltage and Power Consumption

The NDR region of the diode-connected SymFET with *L*=100 nm is around 0.30 V-0.50 V, as illustrated in Fig. 6, which leads to possible low-voltage low-power operation. If the power supply voltage is too small, the oscillation is not able to stay within the NDR range, and the oscillation vanishes. However, if the power supply is too high, the NDR effect does not tend to be strong enough for the entire V_{DS} range in the oscillation. As a result, the oscillation does not hold in this case, either. Table II summarizes the differential output amplitude and the power consumption of the oscillator under different power supply voltages. With a 0.35 V power supply, the VCO power consumption is only 0.19 mW.

TABLE II. SIMULATED OUTPUT AMPLITUDE AND POWER CONSUMPTION OF THE PROPOSED DIODE-CONNECTED SYMFET OSCILLATOR

VCC (mV)	Output Amplitude (mV)	Power (mW)
300	280	0.23
350	412	0.19
400	492	0.20

C. Frequency Range

As given by Eq. (8), the oscillation frequency f_{osc} is determined by the inductance and the sum of the capacitance in the oscillation loop. The inductance in the oscillator could be realized through a spiral inductor, or an appropriate length of coplanar waveguide for a small inductance and high oscillation frequency f_{osc}. If the inductance L_v and the capacitance C_v are arbitrarily chosen, the proposed VCO is able to oscillate at a frequency as high as 89 GHz with L_v=0.05 nH and only the intrinsic capacitance. Smaller sized diode-connected SymFETs help for larger f_{osc} with smaller intrinsic capacitance, but tend to behave worse in phase noise due to more $1/f$ noise.

Oscillation frequency tuning is necessary for some applications. Using a diode-connected SymFET with fixed parameters described above, the oscillation frequency f_{osc} could be adjusted through capacitance tuning or inductance tuning. A common way is to tune the voltage bias of the varactors, which acts as voltage-controlled capacitors, as shown in Fig. 7(a). The simulated tuning range is around 1.0% using a varactor diode in 130 nm CMOS process, as summarized in Table III. The tuning range in this low-voltage design is limited by the small tuning range [0, VCC] of the varactor tuning control voltage *Vctrl* in Fig. 7(a).

D. Phase Noise

As introduced earlier, the highly nonlinear oscillation operation shifts the low-frequency $1/f$ noise to near the oscillation frequency [12]. Considering the thermal noise, shot noise, and $1/f$ noise, periodic steady state analysis (PSS) and periodic noise analysis (PNOISE) simulations are performed to evaluate the phase noise performance of the oscillator, as shown in Fig. 8 and summarized in Table III. When the power supply increases from 0.30 V to 0.40 V, the simulated phase noise at 1.0 MHz frequency offset drops from -117 dBc/Hz to -123 dBc/Hz.

It has been reported that the $1/f$ low-frequency noise of the graphene layer could be reduced by enlarging the device area, and the $1/f$ low-frequency graphene noise could be further reduced by up to an order through stacking more layers of graphene together [15]. Therefore, the phase noise performance has the opportunity to be further improved.

E. Variations

Considering possible insulator thickness variations and temperature fluctuations, simulations with variations of 10% of gate insulator thickness t_g and 250 K – 350 K temperature are performed. The simulation results are summarized in Table IV, showing the robustness of diode-connected SymFET against those variations.

TABLE IV. SIMULATED OSCILLATION FREQUENCY FOSC AND PHASE NOISE WITH VARYING GATE INSULATOR THICKNESS AND TEMPERATURE T (VCC=0.40 V)

t_g (nm)	f_{osc} (GHz)	Phase noise (dBc/Hz)
4.5	3.04	-122
5.0	3.05	-123
5.5	3.06	-124
T (K)	**f_{osc} (GHz)**	**Phase noise (dBc/Hz)**
250	3.07	-123
300	3.05	-123
350	3.05	-122

F. Performance Comparison and Discussions

For comprehensive evaluation of a high frequency VCO, a figure-of-merit (*FOM*) is included in Table III, with the definition of [20][22]

$$FOM = \left(\frac{f_{OSC}}{\Delta f}\right)^2 \frac{1}{L\{\Delta f\} \bullet P}, \quad (9)$$

where $L\{\Delta f\}$ is the VCO phase noise at a frequency offset of Δf,

TABLE III. PERFORMANCE COMPARISONS BETWEEN THE SYMFET OSCILLATOR AND MEASURED CMOS/RTD OSCILLATORS

	This work			[20]	[21]	[22]	[23]	[7]	[8]	[9]
Publication year				2012	2010	2005	2010	2009	2013	2005
Process	**SymFET**	**SymFET**	**SymFET**	130 nm CMOS				RTD		
VCC (V)	**0.30**	**0.35**	**0.40**	0.60	0.40	0.50	0.30	0.36	1.42	0.34
f_O (GHz)	**3.05-3.07**	**3.05-3.08**	**3.05-3.08**	5.6	4.9	3.8	3.58	14.9	28.7	17.6
Δf (MHz)	**1.0**	**1.0**	**1.0**	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Phase noise (dBc/Hz)	**-117**	**-121**	**-123**	-122	-122	-119	-117	-100	-114	-112
Power (mW)	**0.23**	**0.19**	**0.20**	4.2	1.9	0.57	0.23	0.087	289	1.42
FOM (10^{19}/mW)	**2.03**	**6.16**	**9.28**	1.18	2.00	2.01	2.78	2.72	0.07	3.46

and P is the VCO power consumption at the oscillation frequency of f_{osc}. A higher *FOM* represents higher power efficiency. The proposed SymFET oscillator has a *FOM* of 2.03×10^{19}/mW, 6.16×10^{19}/mW, and 9.28×10^{19}/mW under 0.30 V, 0.35 V, and 0.40 V, respectively.

Table III summarizes the performance comparisons between the proposed diode-connected SymFET oscillator and CMOS/ RTD oscillators. As shown in Table III, compared with the low-voltage low-power CMOS VCOs [20]-[23] oscillating at a similar frequency, the proposed diode-connected SymFET oscillator has the lowest power consumption (as low as 0.19 mW) and the lowest phase noise (as low as -123 dBc/Hz). Therefore, the SymFET oscillator has the highest *FOM* when the power supply is 0.40 V. Compared with the RTD VCOs in [8] and [9], the proposed diode-connected SymFET oscillator has much better phase noise performance, consumes much less power, and achieves a higher *FOM*. Compared with the lowest-power VCO in [7], the proposed SymFET oscillator still outperforms with a higher FOM due to much less phase noise.

It is noted that our results are based on simulation due to the infancy of the technology while most of the reported efforts are based on measured devices. We have extensively accounted for noise effects, device and temperature variations that will influence a real device to reduce the gap. Our projected performance can also benefit from further SymFET device optimization that is still ongoing as compared to more mature CMOS process. For example, stacking graphene layers could reduce the flicker noise for better phase noise. While it is challenging to factor the exact contributions of these effects, the comparisons indicate that SymFET oscillators are competitive in low-power applications.

IV. CONCLUSION

This paper has presented a new type of LC-tank oscillator through the exploration of the NDR characteristic of the proposed diode-connected SymFET. This is so far, to the authors' knowledge, the first SymFET analog/RF demonstration after SymFET was presented. The Verilog-A SymFET circuit model has been developed with the integration of both capacitance and noise components. The proposed diode-connected configuration has been applied to satisfy the SymFET terminal voltage requirements, and the device characteristics of the diode-connected SymFET is also explored for the first time. Simulation results of the SymFET oscillator and comparisons with the state-of-art CMOS and RTD oscillators have revealed that the proposed SymFET oscillator has the capability of low-voltage low-power operation and high-robustness against the device size and temperature variations. This makes the SymFET oscillator promising for low-power and high-stability applications. Future work on circuit fabrication experiments, and SymFET noise verification and optimization is of significance.

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REFERENCES

[1] Alan C. Seabaugh *et al*, "Low-voltage tunnel transistors for beyond CMOS logic," Proceedings of the IEEE, vol. 98, no. 12, pp. 2095-2110, Dec. 2010.

[2] Dmitri E. Nikonov *et al*, "Overview of beyond-CMOS devices and a uniform methodology for their benchmarking," Proceedings of the IEEE, pp. 2498-2533, 2013.

[3] Pei Zhao *et al*, "SymFET: a proposed symmetric graphene tunneling field-effect transistor. IEEE transactions on electron devices," vol. 60, no. 3, pp.951-957, Mar. 2013.

[4] L. Britnell, R. V. Gorbachev, A. K. Geim *et al*, "Resonant tunnelling and negative differential conductance in graphene transistors," Nature Communications, 4:1794, pp. 1-5, April 2013.

[5] Rongtai Wang and Ramesh Harjani, "Partial positive feedback for gain enhancement of low-power CMOS OTAs," Analog Integrated Circuits and Signal Processing, vol. 8, no.1, pp. 21-35, July 1995.

[6] Luca Fanori *et al*, "A 2.5-to-3.3GHz CMOS Class-D VCO," In IEEE International Solid-State Circuits Conference, pp. 346-347, 2013.

[7] Yongsik Jeong *et al*, "A sub-100 µW Ku-band RTD VCO for extremely low power applications," IEEE Microwave and Wireless Components Letters, vol. 19, no. 9, pp. 569-571, Sep. 2009.

[8] J. Wang et al, "28 GHz MMIC resonant tunnelling diode oscillator of around 1mW output power," Electronics Letters, vol. 49, no. 13, 2013.

[9] Sunkyu Choi *et al*, "Low DC-power Ku-band differential VCO Based on an RTD/HBT MMIC technology," IEEE Microwave and Wireless Components Letters, vol. 15, no. 11, pp. 742-744, Nov. 2005.

[10] Michael Feiginov *et al*, "Resonant tunnelling-diode oscillators operating at frequencies above 1.1 THz," Applied Physics Letters, vol. 99, no. 23, pp. 233506-233509, 2011.

[11] R. M. Feenstra *et al*, "Single-particle tunneling in doped graphene-insulator-graphene junctions,". J. of Applied Physics, vol. 111, no. 4, pp. 043711, 2012.

[12] Thomas H. Lee *et al,* "Oscillator phase noise: a tutorial," IEEE J. Of Solid-State Circuits, vol. 35, no. 3, pp. 326-336, March 2000.

[13] Atindra Nath Pal, Ageeth A. Bol, and Arindam Ghosh, "Large low-frequency resistance noise in chemical vapor deposited graphene," Applied Physics Letters, vol. 97, no. 13, pp. 133504, 2010.

[14] Nan Sun *et al,* "Electrical noise and transport properties of graphene," J. of Low Temp. Physics, vol. 172, no. 3-4, pp. 202-211, 2013.

[15] Alexander A. Balandin, "Low-frequency 1/f noise in graphene devices," Nature Nanotechnology, vol. 8, pp. 549-555, 2013.

[16] Y.-M. Lin *et al*, "Strong suppression of electrical noise in bilayer graphene nanodevices," ACS Nano Letters, vol. 8, pp. 2119-2125, 2008.

[17] Aravind Vijayaraghavan, "Graphene – properties and characterization," Springer Handbook of Nanomaterials, 2013.

[18] C. T. Rogers *et al,* "Composition of 1/f noise in metal-insulator-metal tunnel junctions," Physical Review Letters, vol. 53, no. 13, pp. 1272-1275, 1984.

[19] Fred W. Schmidlin, "Enhanced tunneling through dielectric films due to ionic defects," Journal of Applied Physics, vol. 37, pp. 2823-2832, 1966.

[20] Feng Zhao and Fa Foster Dai, "A 0.6-V quadrature VCO with enhanced swing and optimized capacitive coupling for phase noise reduction," IEEE Trans. Circuits and Sys.–I, vol. 59, no. 8, pp. 1694-1705, 2012.

[21] Thomas W. Brown *et al,* "A 475 mV, 4.9 GHz Enhanced Swing Differential Colpitts VCO With Phase Noise of -136 dBc/Hz at a 3 MHz Offset Frequency," IEEE J. of Solid-State Circuits, vol. 46, no. 8, pp. 1782-1795, Aug. 2011.

[22] KaChun Kwok and Howard C. Luong, "Ultra-low-voltage high-performance CMOS VCOs using transformer feedback," IEEE J. Of Solid-State Circuits, vol. 40, no. 3, pp. 652-660, March 2005.

[23] Sheng-Lyang Jang *et al*, "A 0.3 V cross-coupled VCO using dynamic threshold MOSFET," IEEE Microwave And Wireless Components Letters, vol. 20, no. 3, pp. 166-168, March 2010.