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IMPACT OF INTERFACE STATES ON SUB-THRESHOLD RESPONSE OF III-V MOSFETs, MOS HEMTs AND Tunnel FETs

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ABSTRACT

In the past four decades, logic transistor scaling following Moore's Law has resulted in unprecedented increase in logic performance. However, the exponentially rising transistor count has also led to increased energy consumption in modern VLSI devices. In order to aggressively scale the supply voltage (V_{cc}) for logic transistors, high mobility channel transistors (such as III-V based transistors) [32,33] and steep sub-threshold slope transistors will be needed. It has already been demonstrated that ultra-high mobility compound semiconductor-based MOSFETs and quantum well FETs (QWFETs) (e.g. $In_{0.7}Ga_{0.3}As$ and InSb) [32,33] operate at low V_{cc} with high performance, InGaAs MOSHEMTs with InP composite barrier stack has been demonstrated with 3.5 times higher effective carrier velocity than strained Si n-MOSFETs [35].

In this thesis, we first provide a literature survey regarding the origin of interface states at high-k dielectric/III-V semiconductor interface and the experimental methods of extracting interface state density (D_{it}) and we approximate the D_{it} profile [27] and included in the simulation. By using a drift-diffusion based numerical simulator, we investigate the device performance in the sub-threshold region of three different types of III-V based transistor architectures. We analyze the impact of the D_{it} present at the high-k dielectric and $In_{0.53}Ga_{0.47}As$ interface on the sub-threshold response of each design, and discuss the advantages and disadvantages of each of the three architectures. The results shows that the same exact D_{it} distribution at the high-k dielectric/III-V semiconductor interface can affect the sub-threshold response of different transistor architecture in different ways and highlight the potential of each device.

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1. INTRODUCTION

1.1 Interface states

We often treat silicon dioxide as an ideal insulator, where there are no traps or states at the interface of silicon and silicon dioxide. But in real devices, the silicon/silicon dioxide interface and bulk silicon dioxide is far from electrically neutral. These may be caused by positive or negative charges at the silicon/silicon dioxide interface or by mobile ionic charges and fixed charges trapped within the oxide and itself, which are often created during the fabrication process. The electronic properties of a device which has a semiconductor/oxide interface are very sensitive to the interface state density and its distribution along the semiconductor bandgap [1].

The interface states are located at or very close to the semiconductor/oxide interface with energy distributed along the bandgap of the semiconductor. Electrons or holes get trapped in these states and act like charges at the interface. Figure 1.1 illustrates the localized interface states schematically. The probability that an electron or hole to occupies a given interface state depends on the energetic location of the interface state relative to the Fermi energy, just like the impurity energy states in the bulk of a semiconductor. The energy level of the interface states are fixed relative to the semiconductor band edge at the interface, so when the surface potential changes, the occupation probability of the interface states will also change, according to the relative position of the Fermi-level and the energy level of the interface states.

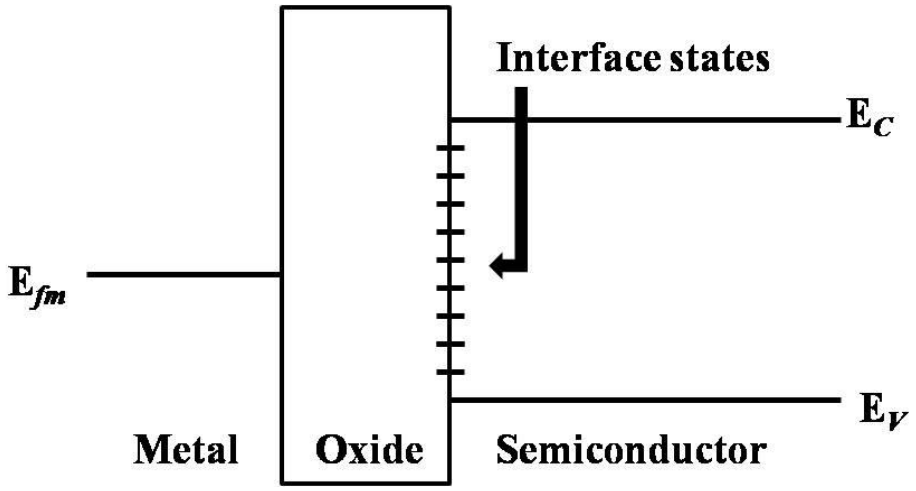


Figure 1.1: Energy-band diagram of a MOS structure, depicting the distribution of interface states along the bandgap of the semiconductor at the semiconductor/oxide interface.

Similar to the impurity energy states in the bulk semiconductor, if a state is neutral and become positively charged when donating an electron, we consider it as a donor state. On the other hand, if a state is neutral and become negatively charged when accepting an electron, we consider it as an acceptor state. For donor states, the probability of occupation is

$$F_{SD}(E_d) = \frac{1}{1+2\exp\left[\frac{E_F-E_d}{kT}\right]} \qquad (1.1)$$

For acceptor states, the probability of occupation is

$$F_{SA}(E_a) = \frac{1}{1+4\exp\left[\frac{E_a-E_F}{kT}\right]} \qquad (1.2)$$

where E_d is the energy of the donor state with respect to the valence band edge, and E_a is the energy of the acceptor state with respect to the valence band edge.

1.2 Fermi-level Pinning and Charge Neutrality Level

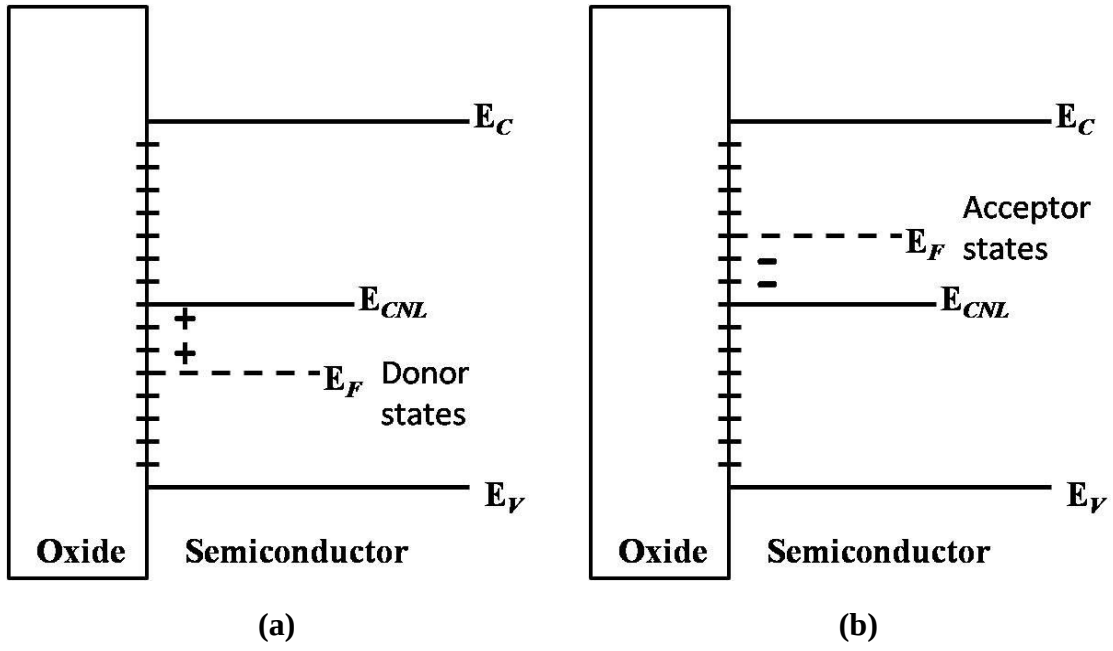


Figure 1.2: General interface states system consisting of (a) donor and (b) acceptor states. This is often expressed by an equivalent distribution with a charge-neutrality level E_{CNL} above which the states are acceptor type and below which they are donor type. When E_F is above E_{CNL}, net charge is positive and when E_F is above E_{CNL}, net charge is negative.

Presumably, every interface has both kind of states, donor state and acceptor state. There is a convenient notation to express the sum of these states on an equivalent

interface states density (D_{it}) distribution with a characteristic energy level called the charge-neutrality level E_{CNL}. Interface states which are above the E_{CNL} are acceptor states, and if the Fermi level E_F is above E_{CNL}, the states are negatively charged if the states are occupied. Interface states which are below the E_{CNL} are donor states, and if the Fermi level E_F is below E_{CNL}, the states are positively charged if the states are occupied, as shown in Figure 1.2.

In order to calculate the concentration of trapped charge at the interface, we assume that at room temperature, the occupancy of a trap takes a value of 0 when above E_F and 1 when below E_F. With this assumption, we can easily calculate the interface-trapped charge by:

$$\boldsymbol{Q_{it} = -q \int_{E_{CNL}}^{E_F} D_{it} dE} \qquad E_F \text{ above } E_{CNL} \quad C/cm^2$$

$$\boldsymbol{= -q \int_{E_F}^{E_{CNL}} D_{it} dE} \qquad E_F \text{ below } E_{CNL} \qquad \textbf{(1.3)}$$

The charges are the effective net charges per unit area (C/cm^2). The interface trap levels are distributed across the energy bandgap at the interface and this distribution can be expressed as:

$$\boldsymbol{D_{it} = \frac{1}{q}\frac{dQ_{it}}{dE}} \qquad \#\text{ of traps/cm}^2\text{-eV} \qquad \textbf{(1.4)}$$

The change in Q_{it} arises from the Fermi level movement at the surface, E_F or the change in the surface potential φ_s, and this can be used to determine the interface trap density D_{it} experimentally. More details will be discussed in the next chapter. Eq. 1.4 can only determine the magnitude of D_{it} but cannot distinguish whether the interface states are donor states or acceptor states.[2]

When a voltage is applied to the gate metal of a MOS structure, the Fermi level in the semiconductor moves up or down with respect to the band edges, thereby changing the occupation probability of the interface states. When the Fermi level energy, E_F coincides with the charge-neutrality level E_{CNL}, the whole interface is charge neutral. A slight deviation of E_F from E_{CNL} causes the interface states to be charged: the interface states will be negatively charged if E_F is higher than E_{CNL} and positively charged if E_F is below than E_{CNL}. The band bending within the semiconductor is determined by the charge balance between the interface trap charge, Q_{it} and the space charge, Q_{SC} in the depletion region of the semiconductor.

For typical areal densities of atoms at the interface, the interface state density can reach as high as 10^{14} cm^{-2}. Typically, the interface states are distributed over an energy range of 0.1 to 1eV within the forbidden bandgap at the interface, so the interface state density per unit energy can be as high as 10^{15} cm^{-2} eV^{-1}. Such a high density of interface state will cause the Fermi level, E_F to be pinned very close to the charge-neutrality level E_{CNL}, known as Fermi level pinning. Higher the deviation of E_F from the charge-neutrality level,

higher is the amount of interface states that will be charged, causing the charge density at the interface to be so high that it cannot be compensated by the space charge within the semiconductor. The change in space charge, Q_{SC} caused by varying the semiconductor doping or external electric fields, only shifts the Fermi level with respect to the charge-neutrality level by a small amount [3], this is called Fermi level pinning.

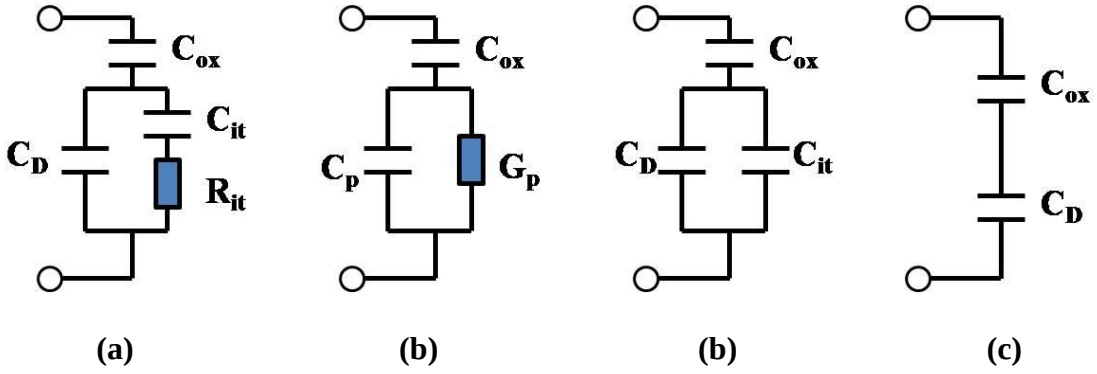


Figure 1.3: (a)(b) Equivalent circuits including interface state effects, C_{it} and R_{it}.[5] (c) Low-frequency limit. (d) High-frequency limit

A change in the interface trap charge density, Q_{it} will affect the MOS capacitance and alter the ideal MOS curve. The basic equivalent circuit [5] that incorporates the interface state effect is shown in Figure 1.3(a). In Figure 1.3(a), C_{ox} and C_D represent the oxide capacitance and the depletion region capacitance in the semiconductor respectively. C_{it} and R_{it} are the interface states capacitance and resistance associated with interface states, they are also a functions of energy. $C_{it}R_{it}$ product will define the interface trap life time τ_{it}. The trap life time τ_{it} determines the frequency behavior of the interface states. Figure

1.3(a) can be converted into an equivalent circuit as shown in Figure 1.3(b), where C_p is the frequency-dependent capacitance and G_p is the frequency-dependent conductance,

$$C_p = C_D + \frac{C_{it}}{1+\omega^2\tau_{it}^2} \tag{1.5}$$

and

$$\frac{G_p}{\omega} = \frac{C_{it}\omega\tau_{it}}{1+\omega^2\tau_{it}^2} \tag{1.6}$$

Also of particular interest are the equivalent circuits in the low-frequency and high-frequency limits, included in Figure 1.3. R_{it} is set to zero in the low-frequency limit, and C_D is parallel to C_{it}. The C_{it} –R_{it} branch is ignored or open in the high-frequency limit. This means that the interface trap life time τ_{it} is not short enough to respond to the high-frequency signal. For the low-frequency C_{LF} and the high-frequency C_{HF}, the total terminal capacitance will be [2]:

$$C_{LF} = \frac{C_{ox}(C_D+C_{it})}{C_{ox}+C_D+C_{it}} \tag{1.7}$$

$$C_{HF} = \frac{C_{ox}C_D}{C_{ox}+C_D} \tag{1.8}$$

The position of charge-neutrality level, E_{CNL} is different in different semiconductors, table 1.1 gives the location of E_{CNL} in various semiconductors. A recent review on charge-neutrality level (CNL) relevant for III-V materials can be found in [4].

Table 1.1 Parameters for the various semiconductors – bandgap, electron affinity (χ) and charge-neutrality level (CNL) with respect to the valence band edge [4]

	Gap (eV)	χ (eV)	CNL (eV)
Si	1.12	4.05	0.2
Ge	0.67	4.13	0.1
SiC 3C	2.35	4.55	1.3
SiC6H	3.05	3.85	1.55
SiC4H	3.25	3.65	1.55
AlP	2.56	2.8	1.3
GaP	2.25	3.2	0.8
InP	1.34	4.4	0.6
AlAs	2.16	3.54	0.92
GaAs	1.45	4.15	0.55
InAs	0.36	4.9	0.50
AlSb	1.7	3.6	0.4
GaSb	0.75	4.06	0.06
InSb	0.17	4.59	0.15
InN	0.76	5	1.87
GaN	3.2	3.3	2.3
AlN	6.2	0.6	2.8
ZnO	3.4	4.6	3.27

1.3 Origin of Interface States at the III-V semiconductor/oxide interface

In a silicon system, the interface state distribution at the Si/SiO_2 interface depends on two transitions associated with adding one or two electrons to the defect, i.e. the Silicon dangling bond [6]. A similar model is used in the GaAs system. Recently a model for the origin of GaAs gap states has been proposed based on the concept of metal-induced gap states (MIGS) [7][8]. In this model, it is suggested that the higher on-state current and lower sub-threshold slope of $In_{0.53}Ga_{0.47}As$ based n-type FETs compared to GaAs based n-type FETs might be due to larger density of metal-induced gap states below the conduction band edge for GaAs, and the base energy of the charge neutrality level in GaAs.

There is another model that has been introduced and adapted to the case of III-V semiconductor/oxide interface [9]. It points out that interface states at the III-V semiconductor/oxide interface cannot be due to metal-induced gap states MIGS, but originate from the native interface defects. There is no MIGS in the semiconductor bandgap next to a wider bandgap oxide. It shows that the Fermi level movement will be inhibited by the native interface states in an n-type FET, similar to the doping limit to account for the observation.

If the Fermi level pinning is not caused by the metal-induced gap states (MIGS), then the Fermi level pinning must be due to the native defect states of the semiconductor. At the Silicon surface, Si dangling bonds give rise to partially occupied surface states near

the mid-gap. But for III-V semiconductor, such as GaAs, the surface Ga and As relax so that their dangling bond states are pushed out of the bandgap. [10] The sites of Ga become planar such that the empty dangling bonds moves into the conduction band. Also the sites of As become more pyramidal resulting in filled dangling bonds that move into the valance band. The Fermi level does not pin in HfO_2 or Al_2O_3 on Si, thus, the Fermi level pinning caused by the gap states must be due to the native III-V semiconductor defects, as sub-monolayer oxygen does introduce the extrinsic gap states on GaAs.[11]

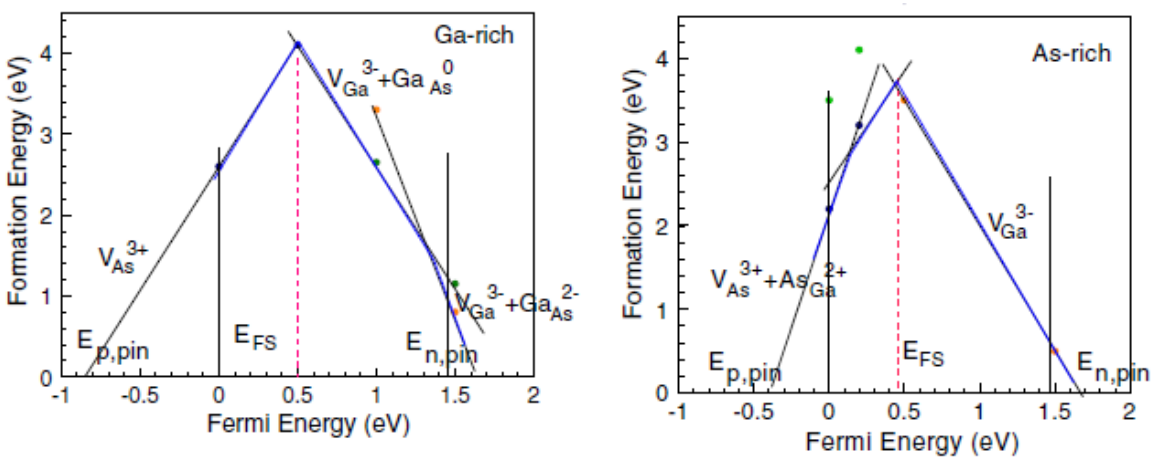


Figure 1.4 Formation energy of intrinsic defects vs. Fermi energy for GaAs for Ga- and As-rich chemical potentials.[13]

The concentration of the native III-V defect states depends on their formation energies. The Fermi level energy in a heavily irradiated bulk III-V semiconductor will be pinned at the Fermi level stabilization energy E_{FS}, due to the creation of the native defects.[12] Figure 1.4 shows the defect stabilities expressed as formation energies versus Fermi energy. E_{FS} is the energy at which the number of positively and negatively charged defects are equal. E_{FS} is relatively similar in both Ga- and As-rich stoichiometries.

As in Figure 1.4, the charged defect's formation energy varies with the Fermi energy. The formation energy will become zero when the Fermi level is far enough above or below the defect level.[14] Thus, if the Fermi level is shifted by doping to that energy, it will spontaneously create a native defect that compensates that dopant. It turns out that the limit to n-type doping of major semiconductor class lies at constant pinning energy above the Fermi level stabilization energy E_{FS} when the semiconductor bands are aligned with equal E_{FS} as in Figure 1.5. For GaAs, the pinning energy $E_{n,pin}$ limiting n-type doping lies just into the conduction band, and the pinning energy $E_{p,pin}$ limiting p-type doping lies well below the valence band. For InAs, it has a narrower bandgap, the valence band lies at similar energy to GaAs, but the conduction band is much lower leadind to high n-type doping. As shown in Figure 1.5, unlike GaAs, the n-type doping limit for InAs and InGaAs lies well above its conduction band.[14]

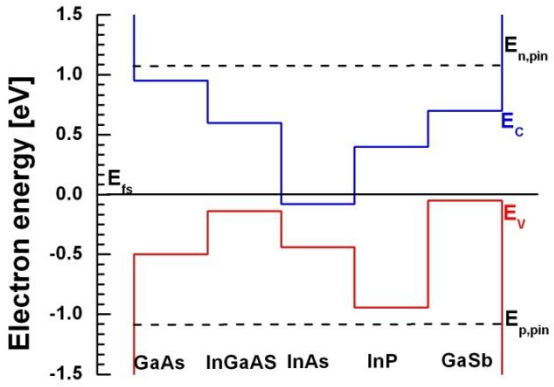


Figure 1.5 Band edges of GaAs, $In_{0.53}Ga_{0.47}As$, InAs, GaP and GaSb aligned according to their Fermi level stabilization energy E_{FS} and n-type and p-type pinning energy

For the case of interface states at III-V semiconductor/oxide interface, the interface defect states are not only due to the anti-sites and vacancies, but also due to like-atom bonds and dangling bonds. The Ga-Ga bonding states (σ) lies near the valence band edge and the As-As anti-bonding states (σ*) lies near the conduction band edge[9]. Figure 1.6 is the schematic diagram of bulk bonding and the defect energy levels in GaAs.

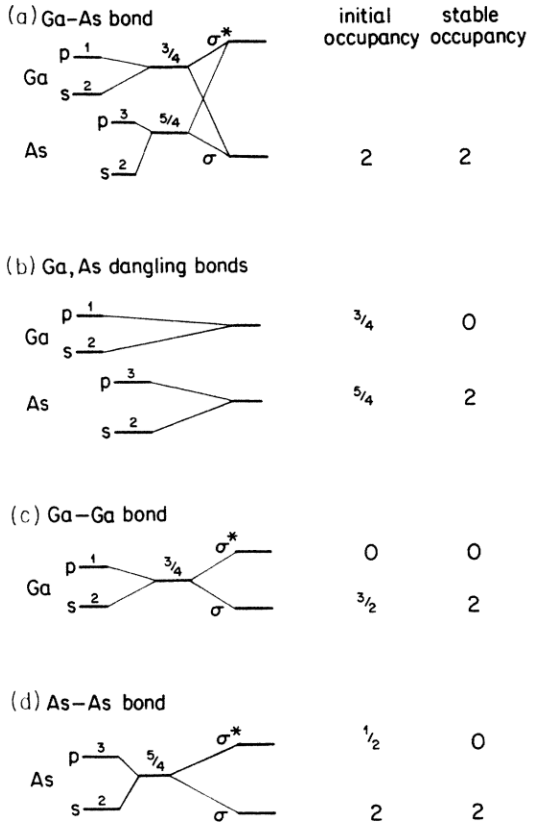


Figure 1.6 Schematic diagram of (a) bulk bonding and (b)(c)(d) the defect energy levels in GaAs. For each energy level, the number in the first column indicates the formal occupancy of an isolated level, and the number in the second column indicates the preferred number of electrons in the level.[15]

Some native defect states are also be created during the oxidation process because not all of the Ga-As bonds are converted in to Ga-O or As-O bonds, or because other sorts of defect states are created [13]. Just as in the Si case, these defect states created during the oxidation can also cause the pinning at the interface. The interface states distribution will be widened from the basic states due to the vacancy and anti-site defects[9]. Figure 1.7 shows a schematic of the density of interface states for GaAs and InAs. The Ga dangling bonds produce a distribution which tails down from inside the conduction band, and the As dangling bonds give a distribution that tails up from below the valence band edge. The like-atom bonds as to this distribution[13].

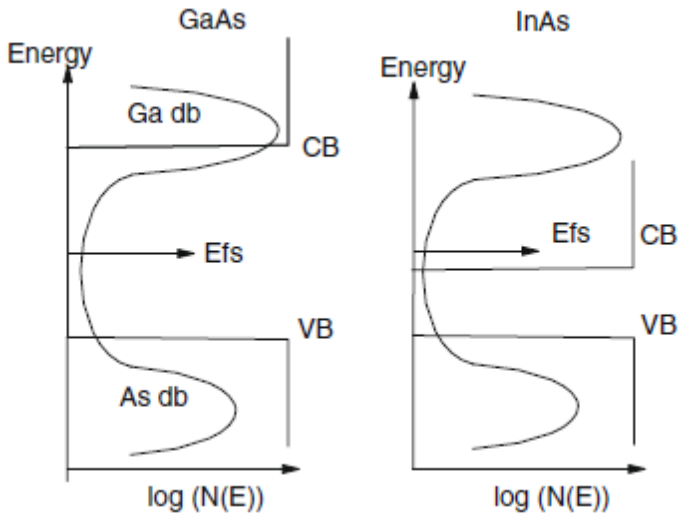


Figure 1.7 Schematic of the density of interface states for GaAs and InAs, compared to the bulk band states, and their charge neutrality levels (CNL)/Fermi level stabilization energies.[13]

Oxygen has a higher electron affinity for Ga than As, so that the interface might be locally As-rich. As the As dangling bond defect states lie in the valence band, and the

problematic states are closer to the conduction band, we can say that the states are most likely due to the As-As anti-bonding states (σ*).

There is an important difference between the native defect states model and the induced gap states, MIGS model in which the native defect states are intrinsic. The concentration of the native defect states depends on the conditions during processing, but the MIGS are intrinsic and cannot be changed. In other words, the native defect state can minimized by optimizing the fabrication process, but the MIGS will always be the same in GaAs, independent of the fabrication process.

In all semiconductors, the pinning energy E_{FS} in the native defect model and the pinning energy E_{CNL} in the MIGS model are numerically similar, it is very easy to get confused between these two models. However, the nature of the responsible states is different[9]. For GaAs, the E_{CNL} is ~0.55eV and the E_{FS} is ~0.5eV. For InAs, the E_{CNL} is ~0.5eV and the E_{FS} is ~0.45eV[4]. It is similar for the chemical trends in both the models. Both E_{Fs} and E_{CNL} have a similar value because both native defect states and MIGS have acceptor states (-/0) above and donor states (0/+) below.

In III-V based FETs, the native defect states will limit the Fermi level E_F movement. In GaAs nFETs, the E_F movement will be limited, but will not be limited in the InAs nFETs because of the lower conduction band. The defects in InAs are at a similar energy with respect to the valence band in GaAs. For GaAs pFETs, E_F will not be limited because the defects lie deeper in to the valence band and do not spill much into the energy bandgap.

In this section, we discussed the origin of the native defect states and its formation. We also pointed out the difference between the Fermi level stabilization energy E_{FS} in the native defect model and the charge-neutrality level E_{CNL} in the metal-induced gap states MIGS model. At the III-V/oxide interface, the pinning of the Fermi level energy arise due to native defects.

2. EXTRACTION OF INTERFACE STATE DENSITY

Interface trapped charge, also called as the interface states or traps, as we discussed in the last chapter, these interface traps are attributed to dangling bonds and other native defects at the semiconductor/insulator interface. In order to evaluate the interface trap density D_{it}, we can use either capacitance measurement or the conductance measurement technique. In this chapter, we are going to explain these methods and the extracted D_{it} profile.

2.1 High-Low Frequency Capacitance Method

Before discussing high-low frequency capacitance method, we will first derive some useful terms. The relationship between the interface trap associated capacitance C_{it} and interface trap density D_{it} is derived as follow. Since $dQ_{it}=qD_{it}dE$, and $dE=qd\varphi_s$, we obtain

$$C_{it} \equiv \frac{dQ_{it}}{d\varphi_s}$$

$$= q^2 D_{it} \qquad (2.1)$$

We can also derive the surface potential φ_s versus applied voltage V curve in relationship to the interface traps using the low-frequency equivalent circuit in Figure 1.3(c). Since $V=V_{ox}+\varphi_s$, we obtain

$$\frac{d\varphi_s}{dV} = \frac{C_{ox}}{C_{ox}+C_D+C_{it}} \qquad (2.2)$$

Substitution of equation (2.1) into equation (2.2) gives

$$D_{it} = \frac{C_{ox}}{q^2}\left[\left(\frac{d\varphi_s}{dV}\right)^{-1} - 1\right] - \frac{C_D}{q^2} \qquad (2.3)$$

From equation (2.3), we can calculate the D_{it} if we can obtain the φ_s-V relationship from the capacitance measurement[2].

There are basically three different capacitance methods to determine D_{it}, high-frequency method, low-frequency method and high-low frequency method.

The high-frequency method was first developed by Terman[16]. As shown in Figure 1.3(d), the advantage of high-frequency method is it does not contain the interface trap associated capacitance C_{it} in the equivalent circuit. As the capacitance C_{HF} is measured, we can determine depletion-layer capacitance C_D by[2]

$$C_{HF} = \frac{C_{ox}C_D}{C_{ox}+C_D} \qquad (2.4)$$

φ_s can be calculated by theory once we know the C_D and the φ_s-V relationship can be obtained. The D_{it} can be determined from equation (2.3).

The low-frequency method or so-called quasi-static method was first use by Berglund [17] to obtain the φ_s-V relationship. The D_{it} can be obtained from the φ_s-V relationship by using equation (2.2), which is based on the low-frequency equivalent circuit in Figure 1.3(c),

$$\frac{d\varphi_s}{dV} = \frac{C_{ox}}{C_{ox} + C_D + C_{it}}$$

$$= 1 - \frac{C_D + C_{it}}{C_{ox} + C_D + C_{it}}$$

$$= 1 - \frac{C_{LF}}{C_{ox}} \qquad \textbf{(2.5)}$$

Integrating equation (2.5) by two applied voltage we get

$$\varphi_s(V_2) - \varphi_s(V_1) = \int_{V_1}^{V_2} \left(1 - \frac{C_{LF}}{C_{ox}}\right) dV + c_1 \quad \textbf{(2.6)}$$

where the C_{LF} represent the capacitance under low-frequency and c_1 is a constant. The surface potential can be determined at any applied voltage in equation (2.6). The constant

in equation (2.6) can be the starting point at accumulation or strong inversion where φ_s is known to have weak dependence on the apply voltage [2]. Once we know the value of φ_s, we can calculate the depletion-layer capacitance C_D from equation (2.3). One of the disadvantages associated with the low-frequency method is the measurement difficulty due to the higher leakage current for thinner oxide layer.

Castagne and Vapaille [18] developed a method that combines both high-frequency and low-frequency method, which so-called the high-low frequency method. For the high-low frequency method, the theoretical calculation is no longer needed for comparison, besides such theoretical calculation is highly complicated for a non-uniform doping profile. For low frequency,

$$C_{LF} = \frac{C_{ox}(C_D + C_{it})}{C_{ox} + C_D + C_{it}} \qquad (2.7)$$

With equation (2.4), we can express

$$C_{it} = \left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right)^{-1} - C_D$$

$$= \left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right)^{-1} \qquad (2.8)$$

The difference in capacitance between high-frequency and low-frequency is defined as $\Delta C \equiv C_{LF} - C_{HF}$, and using the relationship $D_{it}=C_{it}/q^2$, we can obtain the interface trap density D_{it} directly[2]

$$D_{it} = \frac{C_{ox}}{q^2}\left[\left(\frac{1}{\Delta C/C_{ox} + C_{HF}/C_{ox}} - 1\right)^{-1} - \left(\frac{1}{C_{HF}/C_{ox}} - 1\right)^{-1}\right]$$

$$= \frac{\Delta C}{q^2}\left(1 - \frac{C_{HF}+\Delta C}{C_{ox}}\right)^{-1}\left(1 - \frac{C_{HF}}{C_{ox}}\right)^{-1} \quad \textbf{(2.9)}$$

for each bias point. The first order of equation (2.9) is proportional to ΔC. To determine the energy spectrum of D_{it}, either the low-frequency integration approach or the high-frequency method can be use to determine the surface potential φ_s.

2.2 Conductance Method

In 1967, Nicollian and Goetzberger proposed one of the most sensitive methods to evaluate the interface trap density D_{it}, and were known as the conductance method [19]. This method can be used to measure interface trap densities of the order of $10^9 cm^{-2}eV^{-1}$ and even lower. This method is also one of the most complete methods. The conductance method can extract D_{it} in both the depletion and weak inversion portion of the bandgap,

the cross-section of majority carriers, and also the fluctuation of the surface potential φ_s. The conductance method is based on measuring the equivalent parallel conductance G_P of an MOS capacitor as a function of bias voltage and frequency. This conductance represents the loss mechanism caused by capture and emission of carriers from the interface traps, and can be used to extract the interface state density.

Figure 2.1(a) is the equivalent circuit of a MOS capacitor for the conductance method. In the equivalent circuit, C_{ox} is the oxide capacitance, C_S is the semiconductor capacitance, and C_{it} is the interface trap capacitance. Resistance R_{it} represent the loss mechanism during the capture and emission of carriers from the interface traps. Figure 2.1(a) can be replaced by circuit of Figure 2.1(b), where C_P and G_P are given by

$$C_P = C_S + \frac{C_{it}}{1+(\omega\tau_{it})^2} \tag{2.10}$$

$$\frac{G_P}{\omega} = \frac{q\omega\tau_{it}D_{it}}{1+(\omega\tau_{it})^2} \tag{2.11}$$

where $C_{it}=q^2D_{it}$, $\tau_{it}=R_{it}C_{it}$ and $\omega= 2\pi f$ (f is the measurement frequency), τ_{it} is the interface state time constant, given by $\tau_{it}=[\upsilon_{th}\sigma_p N_A \exp(-q\varphi_s/kT)]^{-1}$. In equation (2.10) and (2.11), the interface traps have a single energy level in the energy bandgap. However, the distribution of interface traps at the semiconductor/oxide interface is continuous in energy within the semiconductor energy bandgap. The capture and the emission happens

primarily at the interface traps located within a few kT/q above or below the Fermi level E_F, leading to a time constant dispersion and normalized conductance given by [19]

$$\frac{G_P}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} \ln\left[1 + (\omega\tau_{it})^2\right] \qquad (2.12)$$

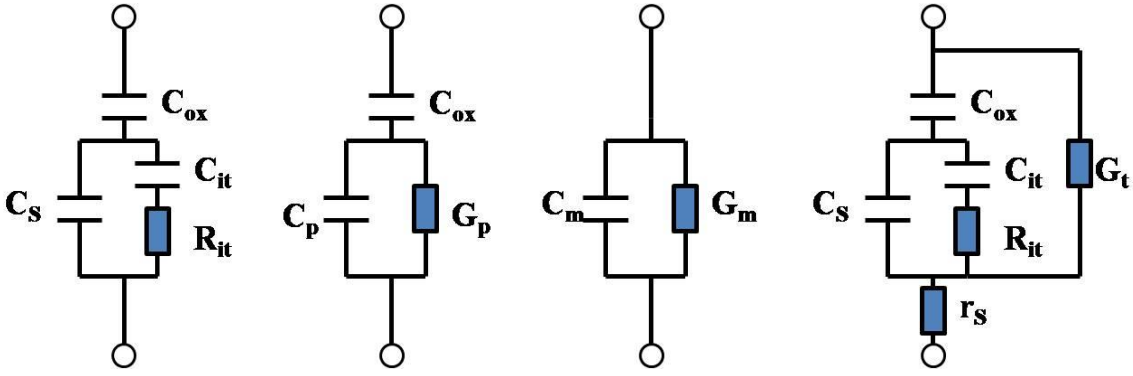


Figure 2.1 Equivalent circuits for conductance method; (a) MOS capacitor with interface trap time constant $\tau_{it}=R_{it}C_{it}$, (b) simplified circuit of (a), (c) measured circuit, (d) including series resistance r_s and tunnel conductance G_t.

It is easier to use the conductance method than using the capacitance method, because for equation (2.11) and (2.12), there is no semiconductor capacitance C_S in the equations. The conductance G_P is measured as a function of frequency and plotted as G_P/ω versus ω[20]. In equation (2.11), at $\omega=1/\tau_{it}$, G_P has a maximum and $D_{it}=2G_P/q\omega$. For equation (2.12), when G_P the maximum, $\omega=2/\tau_{it}$ and $D_{it}=2.5G_P/q\omega$. Now we can determine D_{it} and τ_{it} from the maximum G_P and ω at the location of the peak conductance. The G_P/ω versus ω plot shown in Figure 2.2 is calculated using equation (2.11) and (2.12). An

experimental data from a Si/SiO_2 interface is also shown in Figure 2.2, the experimental peak is much broader than the two calculated curve[21].

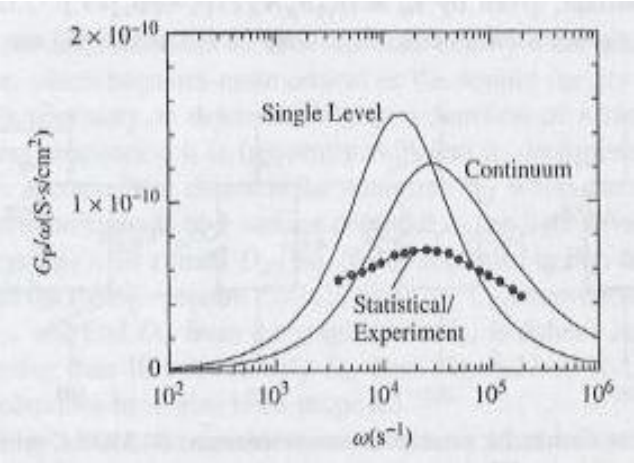


Figure 2.2 G_P/ω versus ω for singal level [equation(2.2)], a continuum [equation(2.3)], and experimental data. For all curves: $D_{it}=1.9\times10^{9}cm^{-2}eV^{-1}$, $\tau_{it}=7\times10^{-5}s$[20].

According the Figure 2.2, the experimental G_P/ω versus ω curve is broader than the continuum curve calculate from equation (2.12), this is because of the interface trap time constant dispersion caused by the fluctuation of the surface potential $\Delta\varphi_s$ due to non-uniformities in oxide charge and interface traps as well as the doping density[20]. Because of the surface potential fluctuations, the analysis of the experimental data becomes more complicated. Considering surface potential fluctuation effect, equation (2.12) becomes

$$\frac{G_P}{\omega}=\frac{q}{2}\int_{-\infty}^{\infty}\frac{D_{it}}{\omega\tau_{it}}\ln\left[1+(\omega\tau_{it})^2\right]P(U_s)dU_s \quad (2.13)$$

where $P(U_s)$ is the probability distribution of the surface potential fluctuations, $P(U_s)$ is given by

$$\boldsymbol{P(U_s) = \frac{1}{\sqrt{2\pi\sigma^2}} exp\left(-\frac{(U_s-\overline{U}_s)^2}{2\sigma^2}\right)} \qquad \textbf{(2.14)}$$

with $\overline{U}_s$ normalized mean surface potential and σ standard deviation.

In Figure 2.2, the curve calculated from equation (2.13) matches the experimental data, this means that when the surface potential fluctuations is considered, there is a good agreement between theory and experiment. An approximate expression giving the interface trap density D_{it} in terms of the maximum conductance is [19]

$$\boldsymbol{D_{it} \approx \frac{2.5}{q}\left(\frac{G_P}{\omega}\right)_{max}} \qquad \textbf{(2.15)}$$

Capacitance meters generally assume that the device consists of a parallel C_m-G_m combination in Figure 2.1(c)[20]. C_m is the measured capacitance and G_m is the measured conductance. Comparing the two circuits in Figure 2.1(b) and 2.1(c), G_P/ω can be expressed in terms of C_m, C_{ox} and G_m as

$$\boldsymbol{\frac{G_P}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2+\omega^2(C_{ox}-C_m)^2}} \qquad \textbf{(2.16)}$$

Here, the series resistance is assumed to be negligible.

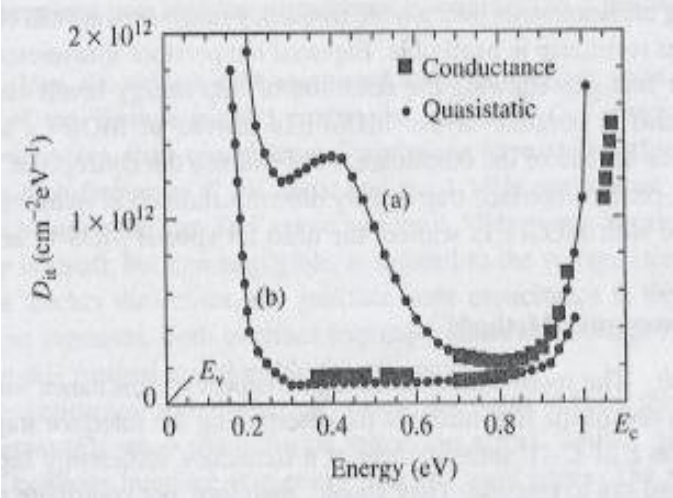


Figure 2.2 Interface trap density D_{it} versus energy for quasi-static and conductance method on (a) (111) n-Si and (b) (100) n-Si. [20]

A wide range of frequency must be used for the conductance measurement. Figure 2.2 is a comparison of the interface trap density D_{it} determined by the quaasi-static and conductance method on (111) and (100) n-type Silicon[22][23]. As in Figure 2.2, the quasi-static method yields D_{it} over a broader energy range, whereas the conductance method yields D_{it} over a narrower energy range, but the two methods agree well with each over. The conductance method measures the D_{it} from flatband to weak inversion in the bandgap. In order to prevent the rise of spurious conductance from the harmonics of signal frequency, the frequency has to be accurately determined and signal amplitude has to be kept around 50mV or lower. For a given D_{it}, the conductance only depends on the device area. For a capacitor with thin oxide layer, the capacitance is much higher relative to the conductance, especially when the D_{it} is low, and also the capacitance meter's

resolution will be dominated by the out-of-phase capacitive current component. In order to prevent this problem, we have to reduce the oxide capacitance C_{ox} by increasing the oxide thickness of the capacitor.

For thin oxide capacitors, the oxide leakage current will be higher, and also the series resistance will no longer be negligible. We need a more complete circuit for the thin oxide capacitor, in Figure 2.1(d), G_t represents the tunnel conductance and r_s represent the series resistance. Equation (2.16) now becomes[24][25]

$$\frac{G_P}{\omega} = \frac{\omega(G_c - G_t)C_{ox}^2}{G_c^2 + \omega^2(C_{ox} - C_c)^2} \qquad \textbf{(2.17)}$$

Where

$$C_c = \frac{C_m}{(1 - r_s G_m)^2 + (\omega r_s C_m)^2} \qquad \textbf{(2.18)}$$

and

$$G_c = \frac{\omega^2 r_s C_m C_c - G_m}{r_s G_m - 1} \qquad \textbf{(2.19)}$$

C_m is the measured capacitance and G_m is the measured conductance. By biasing the device into the accumulation mode, we can determine the series resistance r_s according to[26]

$$r_s = \frac{G_{ma}}{G_{ma}^2 + \omega^2 C_{ma}^2} \qquad (2.20)$$

where G_{ma} and C_{ma} are the measured conductance and capacitance in accumulation mode. As $\omega \rightarrow 0$ in equation (2.19), we can determine the tunnel conductance. When $r_s = G_t = 0$, equation (2.17) will reverts to equation (2.16)

2.3 Extracted D_{it} profile from C-V, G-V measurement

The split C-V measurement of the MOSFET inversion capacitance is a common method to extracting the effective channel mobility of MOSFETs, this method directly estimate the mobile inversion charge density N_{inv} by the gate to channel capacitance C_{gc} as a function of the gate to source voltage V_g as given by

$$Q_{inv} = \int_{-\infty}^{V_g} C_{gc}(V) dV \qquad (2.21)$$

For most of the silicon based MOSFETs including Si MOSFETs with high-κ/metal-gate, this method is highly accurate and reliable. But for III-V based MOSFETs, this method is not that straight forward. In III-V based MOSFETs, the high value of interface states density D_{it} at the semiconductor-dielectric interface due to the native defects of the

semiconductor can exhibit a capacitance C_{it}, this capacitance contributes significantly to the measured C_{gs} that results in an overestimation of the extracted N_{inv}. This can lead to incorrect evaluation of the effective channel mobility [27]. Recently, many groups have reported split C-V measurement and the resultant mobility extracted from the measurement of III-V MOSFETs [28][29][30]. The frequency dispersion capacitance due to the D_{it} and the resistance effects in the inversion regime strongly affected the C-V curves leading to incorrect mobility estimations.

Recently, a novel technique has been reported in [27], this technique can self consistently solve the capacitance-voltage (C-V) and conductance-voltage (G-V) measurement data as a function of gate bias and small signal AC frequency to uniquely determine the D_{it} response as well as the true inversion carrier response for a given voltage. There is a key difference between this method and the conductance method, in this method, the information about the peak position in the measured conductance G/ω versus frequency is not needed, it solves the conductance and the capacitance contribution of D_{it} in a self consistent manner over the entire frequency and voltage range [27]. This will allow us to extract the D_{it} distribution over wider range of energy than the conductance method.

In [27], the measurement was done on $In_{0.53}Ga_{0.47}As$ MOSFETs with $LaAlO_3$ gate dielectric for measuring the capacitance and conductance as a function of frequency and voltage for a range of temperature from 300K low to 35K. An equivalent circuit model

for this measurement in inversion including the effects of channel resistance, gate leakage and interface states is shown in Figure 2.3.

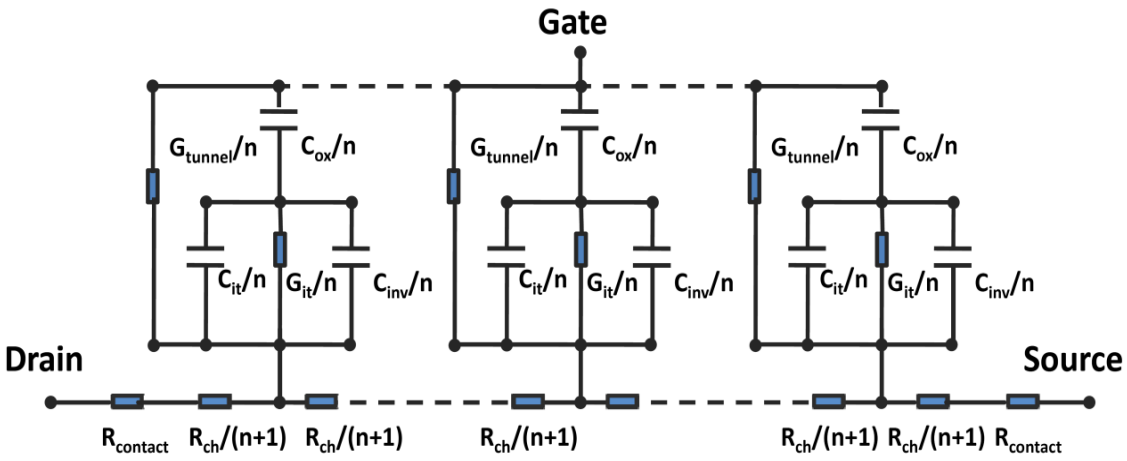


Figure 2.3 Equivalent circuit model of MOSFET in weak and strong inversion. [31]

In this model, $R_{contact}$ is the series resistance associated with implanted source/drain region, contacts and metal pads at the two ends of the channel. R_{ch} is the gate dependent inversion channel resistance, G_{tunnel} in the tunnel conductance of the oxide arising from the gate leakage. C_{ox} is the maximum oxide capacitance measured in accumulation mode on a MOS capacitor. C_{it}, G_{it} and C_{inv} represents the interface trap capacitance, interface trap conductance and the semiconductor inversion capacitance.

By solving the equivalent circuit in Figure 2.3, we can extract the interface state density D_{it}, interface trap response time τ and the true inversion carrier density N_{it} as a function of the gate voltage. The energy voltage relationship of D_{it} can be evaluate from the relationship between N_{it} and the gate voltage V_g. In other words, we can extract the

interface states density and its position in the energy band diagram. Figure 2.4 shows the extracted D_{it} and τ at the III-V/oxide on $In_{0.53}Ga_{0.47}As$ MOSFETs with $LaAlO_3$ gate dielectric in [27].

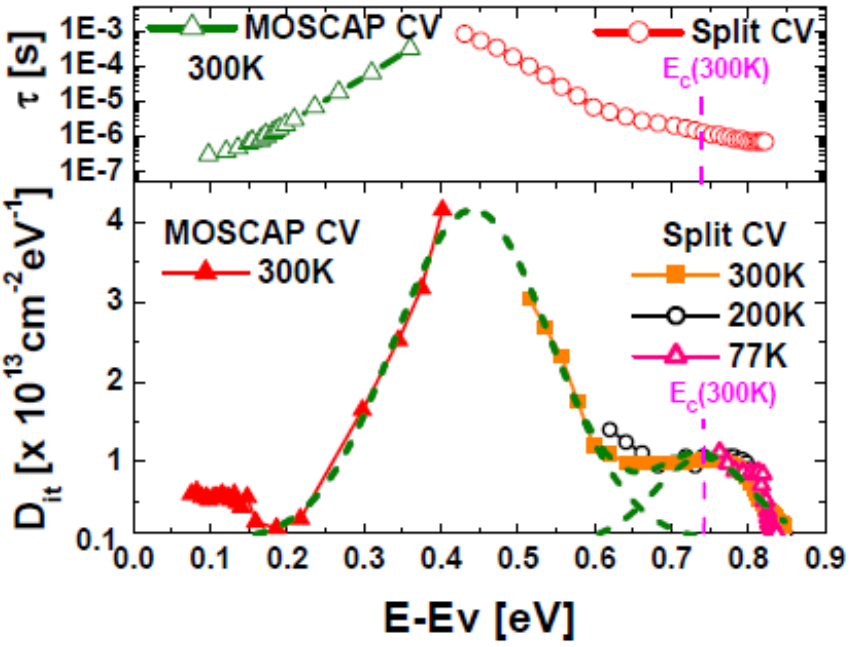


Figure 2.4 Extracted interface state density versus energy and the corresponding trap response time at the III-V/oxide on $In_{0.53}Ga_{0.47}As$ MOSFETs with $LaAlO_3$ gate dielectric. [27]

The D_{it} profile in Figure 2.4 is extracted independently from the C-V and G-V measurement data measured at three different temperatures and are consistent with each other. This D_{it} profile can be approximated by two Gaussian distributions with different peak values as shown as the green dot line in Figure 2.4. The Gaussian distribution with the higher peak value spans across the mid-gap of the $In_{0.53}Ga_{0.47}As$. The other Gaussian distribution with lower peak value extends into the conduction band of the $In_{0.53}Ga_{0.47}As$.

The impact of such $In_{0.53}Ga_{0.47}As$/oxide interface D_{it} distribution on transport characteristics of various III-V based field effect transistors will be discussed in the next chapter.

3. EFFECT OF INTERFACE STATE ON III-V MOSFET, MOS HEMT AND TUNNEL FET: SIMULATION STUDY

3.1 Introduction

Over the last four decades, logic transistor scaling following Moore's Law has resulted in unprecedented increase in logic performance. However, the exponentially rising transistor count has also led to increased energy consumption in modern VLSI devices. In order to aggressively scale the supply voltage V_{cc} for logic transistors, high mobility channel transistors (such as III-V based transistors) [32,33] and steep sub-threshold slope transistors [34] will be needed. It has already been demonstrated that ultra-high mobility compound semiconductor-based MOSFETs and quantum well FETs QWFETs (such as $In_{0.7}Ga_{0.3}As$ and InSb) [32,33] operate at low V_{cc} with high performance InGaAs MOSHEMTs with InP composite barrier stack has been demonstrated with 3.5 times higher effective carrier velocity than strained Si n-MOSFETs [35]. In this chapter, we will discuss the device performance in the sub-threshold region of three different types of III-V based transistor architectures using Sentaurus, a drift-diffusion based numerical simulator. We use the interface state density D_{it} profile mentioned in the last chapter [27] and analyze the impact of such D_{it} distribution present at the high-k dielectric and $In_{0.53}Ga_{0.47}As$ interface on the sub-threshold response of each III-V based transistor design, and discuss the advantages and disadvantages of each of the three architectures. In the next few sections, we will discuss

the physics model which is included in the simulation, the device architectures and discuss the effect of the D_{it} on the performance characteristics of each device.

3.2 Simulation Physics Model

Sentaurus is a numerical simulatior which simulates the electrical behavior of semiconductor devices numerically. A flow chart of the simulation setup for Sentaurus simulator is shown in Figure 3.1.

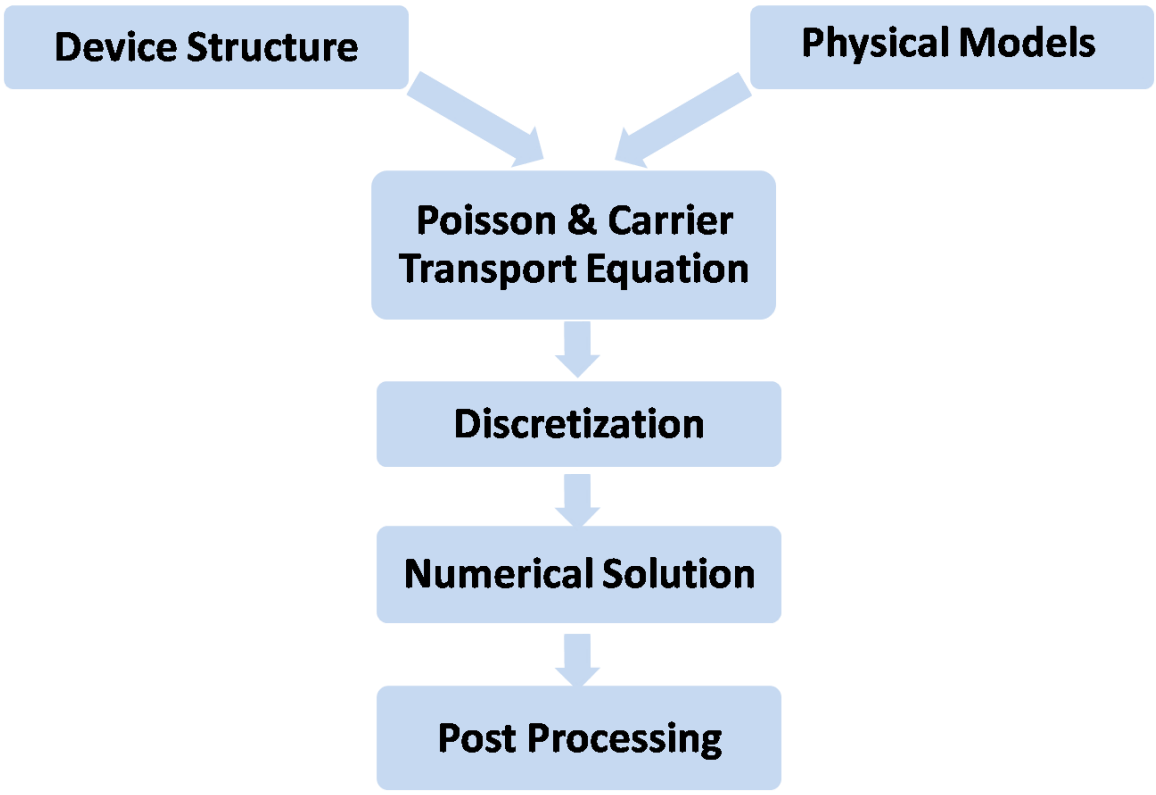


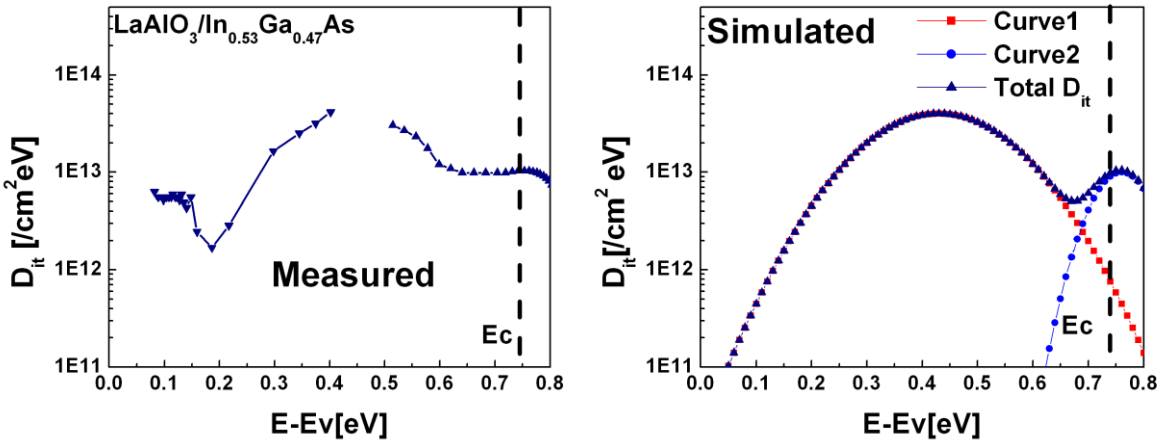
Figure 3.1 Flow chart of the simulation setup.

As shown in Figure 3.1, the device structures should be first designed. In this work, the device structures have been designed in 2 dimensions by using the Sentaurus Structure Editor including all the information of the device structure, these information include the boundaries and material types of the regions, the locations of any electrical contact, the doping conditions of the device and also the grid (the locations of all the discrete nodes and their connectivity) is included. The details of the device architectures will be introduced in the next section.

A set of physics models also should be defined and applied in the device simulation. The physics models included in this work are Fermi statistics, Caughey–Thomas velocity saturation, Masetti mobility model, nonlocal tunneling model, Shockley–Read–Hall generation-recombination and interface trap model. More details of the physics model will be discussed later. After defining the device structure and the physics model, the simulator will solve the Poisson and carrier transport equations by using discretization at each grid point which is defined in the structure and get the numerical solution, these solutions can be displayed by the post processing.

In the Physics model, the Fermi (also called Fermi–Dirac) distribution function has been included in order to calculate the distribution of electrons and holes, Fermi statistics is important for high values of carrier densities. When the carrier is under high electric fields, the carrier drift velocity is no longer proportional to the electric field, instead, the velocity saturates to a finite value, Caughey–Thomas velocity saturation mode is used for the description of this effect [36]. In a doped semiconductor, the carrier mobility will be

degraded due to the scattering of the carriers by charged impurity ions. The Masetti mobility model [37] has been used to describe the behavior of such doping-dependent mobility. Tunneling is a nonlocal process in the simulation, the nonlocal tunneling model is used to simulate the carrier transport equation and the Poisson equation at the nonlocal mesh point which we defined earlier. The Shockley–Read–Hall generation-recombination model is the description of the all the generation-recombination process in the simulation.



(a) **(b)**

Figure 3.2 (a) Extracted D_{it} distribution from experiential measurement. (b) D_{it} distribution used in simulations

The interface trap mode is the model to describe the behavior of the interface states in the simulation. Figure 3.2(a) shows the experimentally measured Dit profile at the interface of an in-situ deposited $LaAlO_3$ high-k dielectric and $In_{0.53}Ga_{0.47}As$ interface after reference [27]. For our simulation purpose, we approximate the interface state density D_{it} by superposition of two Gaussian trap distributions, as shown in Figure 3.2(b).

The left Gaussian trap distribution with a higher peak value spans across a large portion of the bandgap, and the right distribution with a lower peak value extend into the conduction band. In this study, the interface states are considered to be either donor states or acceptor states.

In Figure 3.2(b), the first Gaussian trap distribution with a higher peak value is represented by the equation

$$D_{it} = \left(4 \times 10^{13}\right) exp\left(-\frac{\left(E_{trap} - 0.43\right)^2}{0.0242}\right) \quad (3.1)$$

and the second Gaussian trap distribution with a lower peak value

$$D_{it} = 10^{13} exp\left(-\frac{\left(E_{trap} - 0.75\right)^2}{0.00405}\right) \quad (3.1)$$

where E_{trap} is the trap energy level position respect to the valence band E_V.

3.3 Device Structure

Three different III-V based device architectures have been simulated and analyzed in this study. In this section, the two-dimensional (2D) layout of each III-V based transistor will be introduced. These include an inversion mode surface channel $In_{0.53}Ga_{0.47}As$ MOSFET, an accumulation mode buried channel InAs MOS HEMT, and an $In_{0.53}Ga_{0.47}As$-based inter-band tunnel FET.

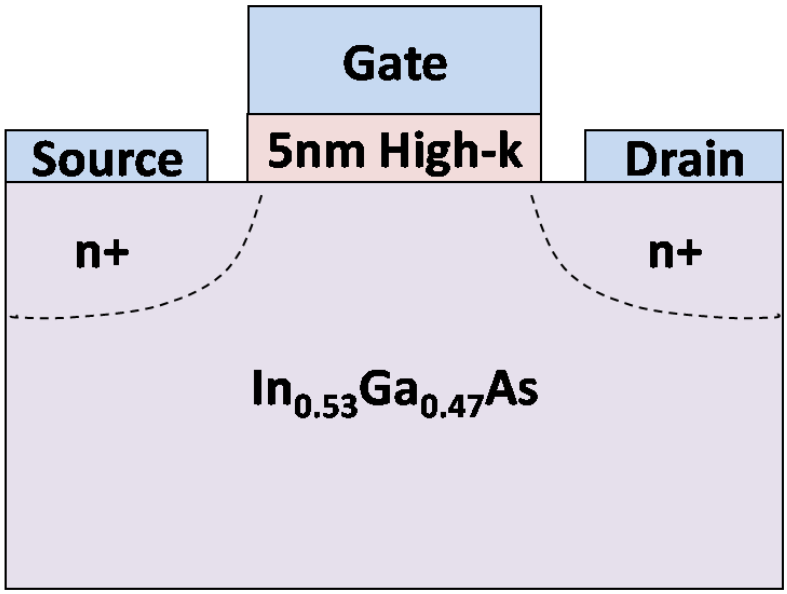


Figure 3.3 Cross-section of 65nm gate length inversion mode surface channel $In_{0.53}Ga_{0.47}As$ MOSFET.

A. Inversion mode surface channel $In_{0.53}Ga_{0.47}As$ MOSFET

A cross section of the inversion mode surface channel $In_{0.53}Ga_{0.47}As$ MOSFET is illustrated in Figure 3.3. This is a traditional bulk MOSFET device design with 65nm

gate length. The simulated device consists of an $In_{0.53}Ga_{0.47}As$ substrate with the background p-type doping of $\mathbf{N_a = 10^{18}cm^{-3}}$. On the top of the channel sits a 5nm thick high-κ oxide layer with 2nm equivalent oxide thickness, which separates the surface channel from the metal gate. The metal gate work function used is 4.55eV. The highly doped n-type source and drain regions are simulated using a Gaussian-type distribution with a peak doping dose of $\mathbf{N_d = 10^{20}cm^{-3}}$ and junction depth of 20nm. The interface state trap model is set at the interface between the high-κ oxide layer and the $In_{0.53}Ga_{0.47}As$ substrate layer.

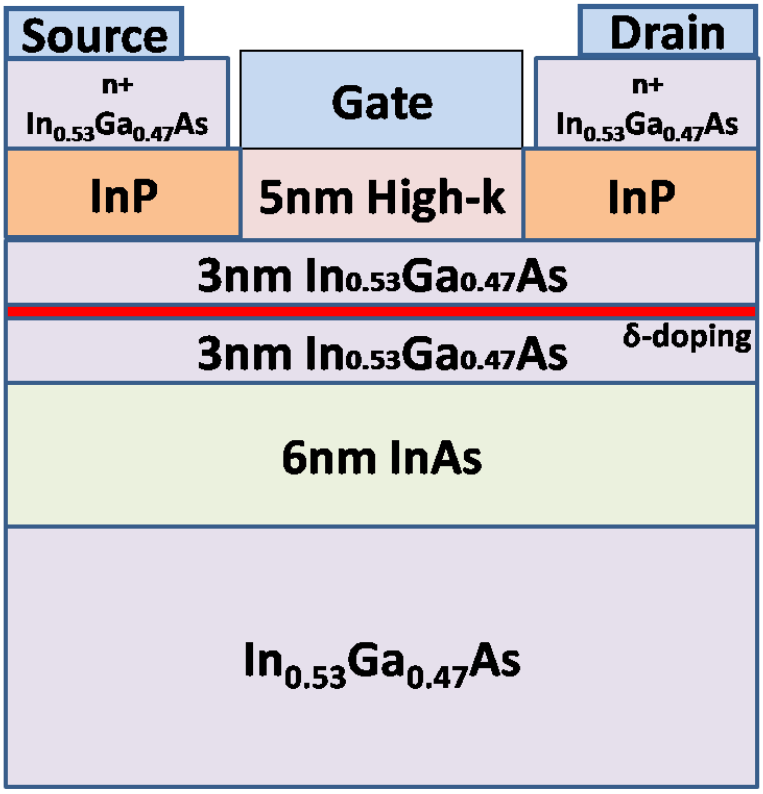


Figure 3.4 Cross-section of 65nm gate length accumulation mode buried channel InAs MOS HEMT.

B. Accumulation mode buried channel InAs MOS HEMT

A cross section of the accumulation mode buried channel InAs MOS HEMT with $In_{0.53}Ga_{0.47}As$ burrier layer is illustrated in Figure 3.4. Same as the MOSFET, the gate length of this device is also 65nm. The simulated device consists of an $In_{0.53}Ga_{0.47}As$ substrate, a 7nm $In_{0.53}Ga_{0.47}As$ barrier layer, and a 6nm InAs channel in between. On the top of the barrier layer sits a 5nm thick high-κ oxide layer with 2nm equivalent oxide thickness, which separates the barrier layer from the metal gate. The metal gate work function used is 4.55eV. The region between the source/drain $In_{0.53}Ga_{0.47}As$ contact and the $In_{0.53}Ga_{0.47}As$ barrier layer are InP cap layers. The substrate, channel and barrier layers are undoped and remain intrinsic, the n-type source/drain region are uniformly doped at $\boldsymbol{N_d = 10^{20} cm^{-3}}$. Finally, a 1nm δ-doping layer ($\boldsymbol{N_d = 5 \times 10^{19} cm^{-3}}$) is used at the middle of the $In_{0.53}Ga_{0.47}As$ barrier layer. The interface state trap model is set at the interface between the high-κ oxide layer and the $In_{0.53}Ga_{0.47}As$ barrier layer.

C. $In_{0.53}Ga_{0.47}As$-based inter-band tunnel FET

A cross section of $In_{0.53}Ga_{0.47}As$-based inter-band tunnel FET is illustrated in Figure 3.5. Same as the two device above, the gate length of this device is also 65nm. The simulated device consists of a $In_{0.53}Ga_{0.47}As$ substrate, p-type substrate is uniformly doped at $\boldsymbol{N_a = 10^{15} cm^{-3}}$, the p^+ region at the source side is uniformly doped at $\boldsymbol{N_a = 10^{19} cm^{-3}}$, and n^+ region at the drain side is uniformly doped at $\boldsymbol{N_d = 5 \times}$

$\mathbf{10^{19}cm^{-3}}$. Similar to the inversion mode surface channel $In_{0.53}Ga_{0.47}As$ MOSFET, between the metal gate and the substrate sits a 5nm thick high-κ oxide layer with 2nm equivalent oxide thickness. The metal gate work function is modeled as 4.55eV. Tunneling happens under the high-κ oxide layer between the p^+ region and the majority p-type substrate. The interface state trap model is set at the interface between the high-κ oxide layer and the $In_{0.53}Ga_{0.47}As$ substrate layer.

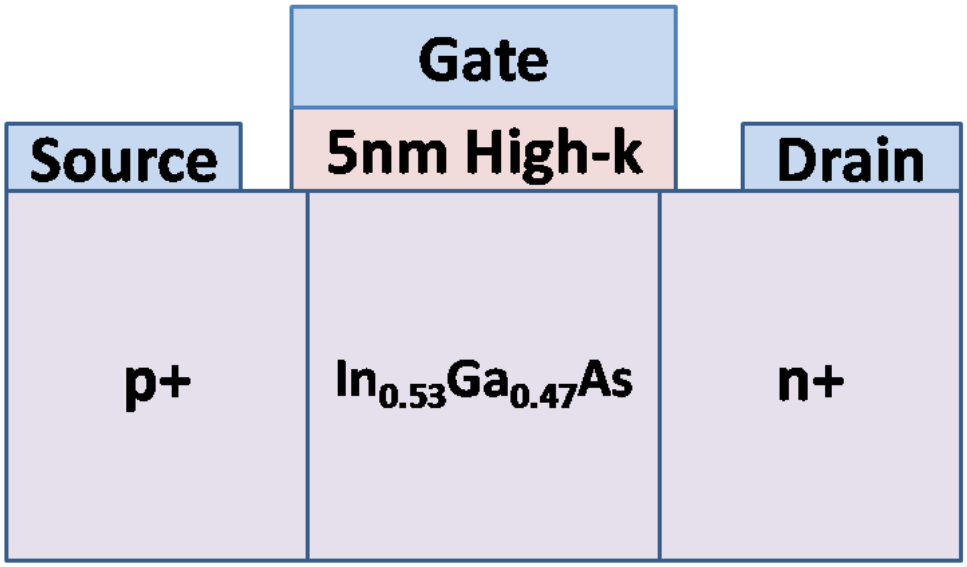


Figure. 3.5 Cross-section of 65nm gate length $In_{0.53}Ga_{0.47}As$-based inter-band tunnel FET.

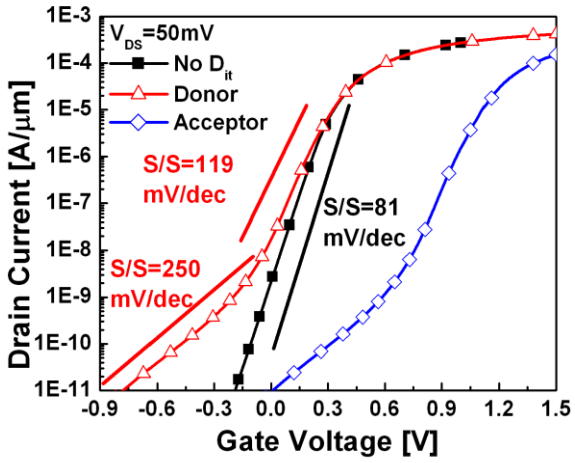
3.4 Current-Voltage Characteristics

In this section, we analyze the effect of D_{it} distribution at the high-κ dielectric and $In_{0.53}Ga_{0.47}As$ interface present in two situations: when the interface states were donor states and the interface states were acceptor states. We compare these two situations to the ideal case (no D_{it} included) of the sub-threshold response for each of the three different types of transistor architecture. Figure 3.6, 3.7 and 3.8 show the simulated transfer characteristics at V_D=50mV for MOSFETs, MOS HEMTs and Tunnel FETs along with their Fermi level movement within the band diagrams as the device turns on.

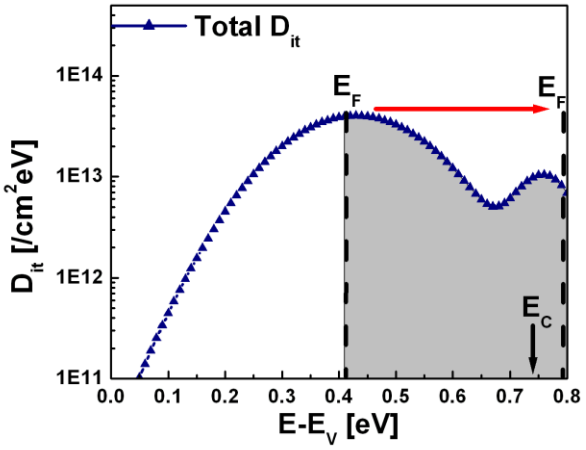
A. Inversion mode surface channel $In_{0.53}Ga_{0.47}As$ MOSFET

Figure 3.6(a) shows the simulated transfer characteristics of MOSFET, the sub-threshold slope of the ideal case is 81mV/dec. When the drain current $\boldsymbol{I_{DS} = 10^{-11}\ A/\mu m}$, the Fermi-level sweeps the highest part of the D_{it} distribution within the bandgap, if the interface states were donor states, a significant portion of donor states stay positively charged as shown by the shaded region in Figure 3.6(b), resulting in severe degradation in sub-threshold slope (250mV/dec). As the drain current increases, the Fermi-level will sweep though much smaller magnitude of D_{it}, the degradation in sub-threshold slope becomes less (119mV/dec). As I_{DS} increases to $\boldsymbol{10^{-5}\ A/\mu m}$, the Fermi-level enters the conduction band and the donor states stay neutralized, and there is

almost no effect of the D_{it}. If the interface states were acceptor states, the acceptor states become negatively charged and resulting in a shift in threshold voltage V_T.



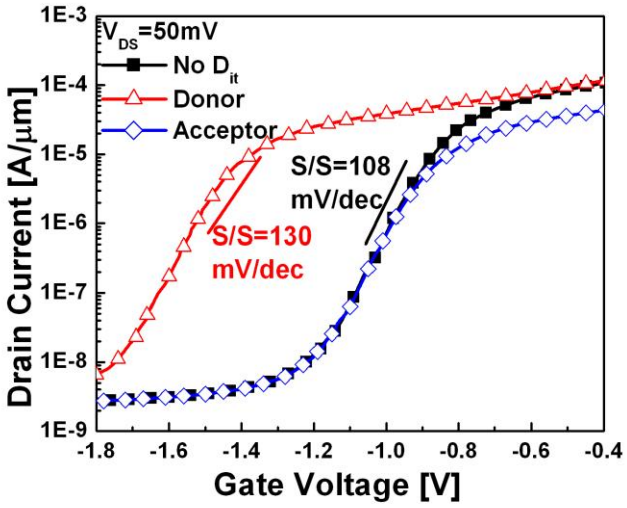
(a)



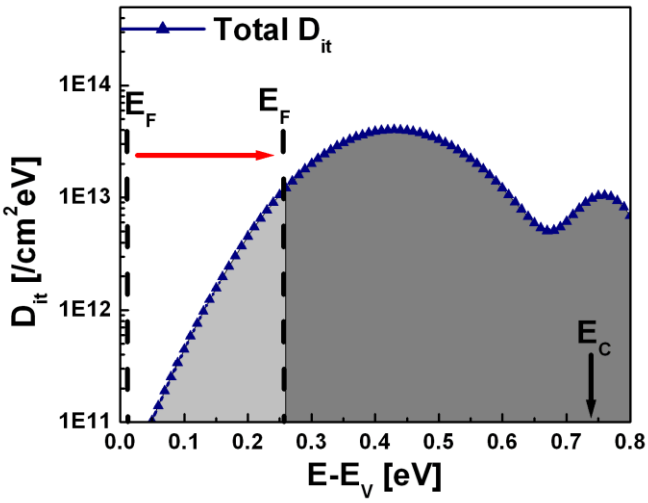
(b)

Figure 3.6 (a) I_D-V_G characteristics at low drain bias (V_D=50mV) for inversion mode surface channel $In_{0.53}Ga_{0.47}As$ MOSFET. (b) The Fermi-level position and movement from $I_{DS} = 10^{-11}\ A/\mu m$ to $I_{DS} = 10^{-5}\ A/\mu m$.

B. Accumulation mode buried channel InAs MOS HEMT



(a)



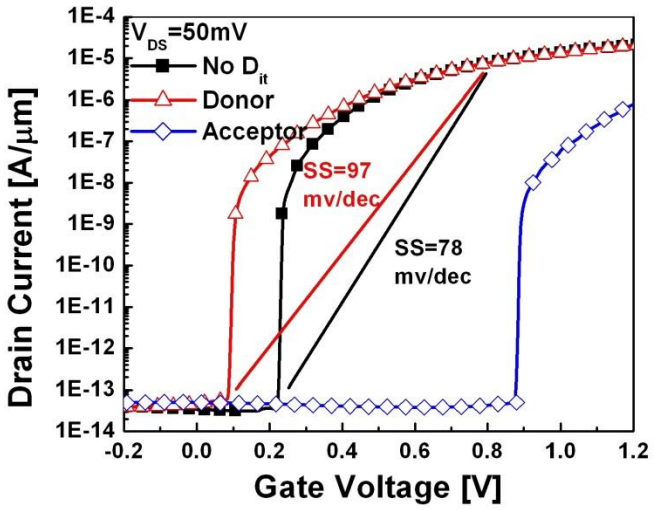
(b)

Figure 3.7 (a) I_D-V_G characteristics at low drain bias (V_D=50mV) for accumulation mode buried channel InAs MOS HEMT. (b) The Fermi-level position and movement from $I_{DS} = 10^{-8}\ A/\mu m$ to $I_{DS} = 10^{-5}\ A/\mu m$.

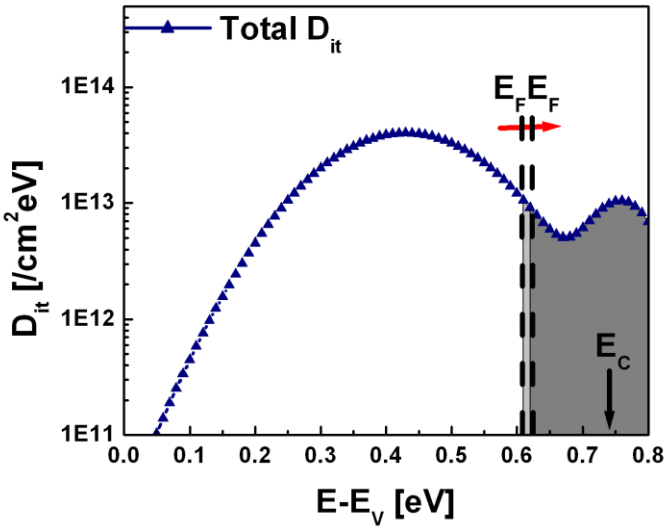
The effect of the D_{it} distribution in MOS HEMTs also leads to a degradation in the sub-threshold slope but less than MOSFETs as shown in Figure 3.7(a). The higher off-state current for this device compared to the InGaAs MOSFET is due to the generation-recombination of the InAs channel. For this architecture, when $\boldsymbol{I_{DS} = 10^{-8}\ A/\mu m}$, Fermi-level is very close to the valence band, if the interface states were donor states, all donor states stay positively charged. As I_{DS} increases to $\boldsymbol{10^{-5}\ A/\mu m}$, as show in Figure 3.7(b), the Fermi-level sweeps in the lower bandgap, which is the lower D_{it} portion of the distribution, part of the donor states are neutralized. The V_T shift is due to significant amount of positively charged donor states.

C. $In_{0.53}Ga_{0.47}As$-based inter-band tunnel FET

Tunnel FETs turns on abruptly when the valence band edge in the p+ source region is raised above the conduction band edge in the channel which is already weakly inverted in the off-state, this gives rise to steep (<kT/q) sub-threshold slope. Figure 3.8(b) shows that, when I_{DS} increase from $\boldsymbol{6 \times 10^{-14}\ A/\mu m}$ to $\boldsymbol{10^{-8}\ A/\mu m}$, the Fermi-level sweeps the interface by only a small amount (~0.01eV), the steep sub-threshold behavior is retained as shown in Figure 3.8(a). Also, The V_T shift is due to the positively charged donor states and negatively charged acceptor states.



(a)



(b)

Figure 3.8 (a) I_D-V_G characteristics at low drain bias (V_D=50mV) for $In_{0.53}Ga_{0.47}As$-based inter-band tunnel FET. (b) The Fermi-level position and movement from $6 \times 10^{-14}\ A/\mu m$ to $10^{-8}\ A/\mu m$.

3.5 Conclusion

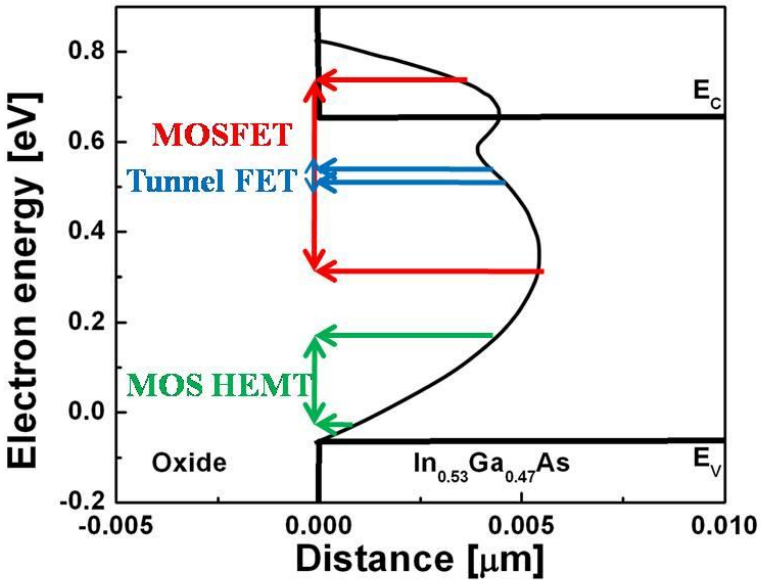


Figure 3.9 Fermi-level movement for MOSFET, MOS HEMT and Tunnel FET

In this chapter, we have introduced the physics based models and the three device structure which we used in the simulation, and investigated how the same exact Interface state density D_{it} distribution at non-ideal $In_{0.53}Ga_{0.47}As$ and high-κ dielectric can affect the sub-threshold response of III-V MOSFETs, MOS HEMTs and Tunnel FETs though a drift-diffusion simulations. It was demonstrated that according to the range and position of the Fermi-level movement at the oxide/semiconductor interface of each the three device architecture in Figure 3.9. For MOSFETs, the Fermi-level sweeps from mid-gap which is the highest part of the D_{it} distribution into the conduction band as it moves from off-state to on-state. For MOS HEMTs, Fermi-level sweeps in the lower half of the

bandgap, which is the lower D_{it} portion of the distribution. For Tunnel FETs, the Fermi-level sweeps the interface by only a small amount. According to the range and position of the Fermi-level movement at the oxide/semiconductor interface, the same exact D_{it} distribution will affect the sub-threshold response of each transistor architecture in a different way.

4. FUTURE WORK

4.1 Deep Depletion in MOS HEMT

The interface trapped charge Q_{it} will change with respect to the position of the Fermi level. When in deep depletion, the quasi-Fermi level will split into Electron Fermi level E_{Fn} and hole Fermi level E_{Fp}. Under this quasi–equilibrium condition, the interface occupancies are now determined by the dynamics of the carrier capture and emission and not directly determined by either E_{Fp} or E_{Fn} [38]. E_{Fn} governs the interface state occupancy in the upper half of the bandgap at the interface and E_{Fp} governs the interface state occupancy in the lower half of the bandgap at the interface.

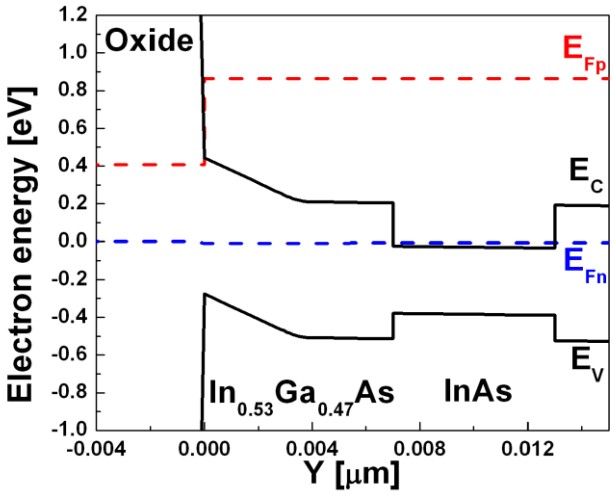


Figure 4.1 Energy-band diagram of the MOS HEMT in deep depletion at $10^{-5}\,A/\mu m$.

Figure 4.1 shows the energy-band diagram of a MOS HEMT. In Figure 4.1, the Fermi level is split into E_{Fp} and E_{Fn} under quasi–equilibrium, E_{Fp} is higher than the conduction band edge E_C and E_{Fn} is in the lower half of the bandgap. Figure 4.2 shows the simulated transfer characteristics of MOS HEMT under deep depletion.

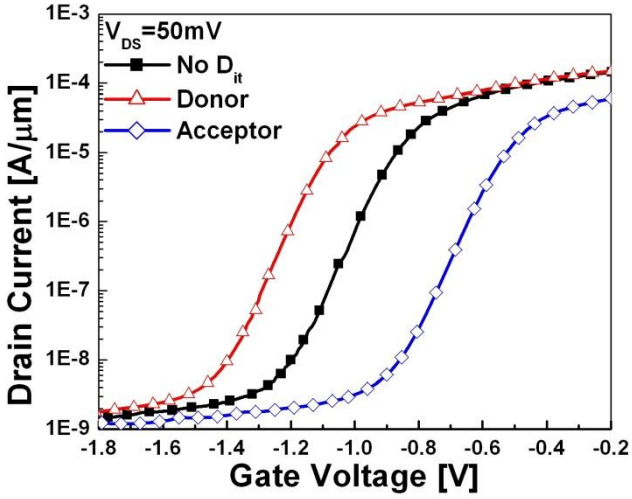


Figure 4.2 I_D-V_G characteristics at low drain bias (V_D=50mV) for accumulation mode buried channel InAs MOS HEMT under deep depletion.

In Figure 4.2, the device shows almost no degradation of the sub-threshold slope both when the interface states are donor type or acceptor type. The shift in threshold voltage V_T in the case of donor state is caused by the positively charged donor states in the upper half of the bandgap due to the position of E_{Fn}. The shift in threshold voltage V_T in the case of the acceptor states is caused by the negatively charged acceptor states in the lower bandgap due to the position of E_{Fp}.

The interface state response in the deep depletion and how to force a MOS HEMT to operate in quasi–equilibrium condition is still under investigation. Figure 4.3 shows the benchmarking of the sub-threshold slope value in InGaAs based MOSFETs and MOS HEMT with the former typically showing higher values than the latter [39].

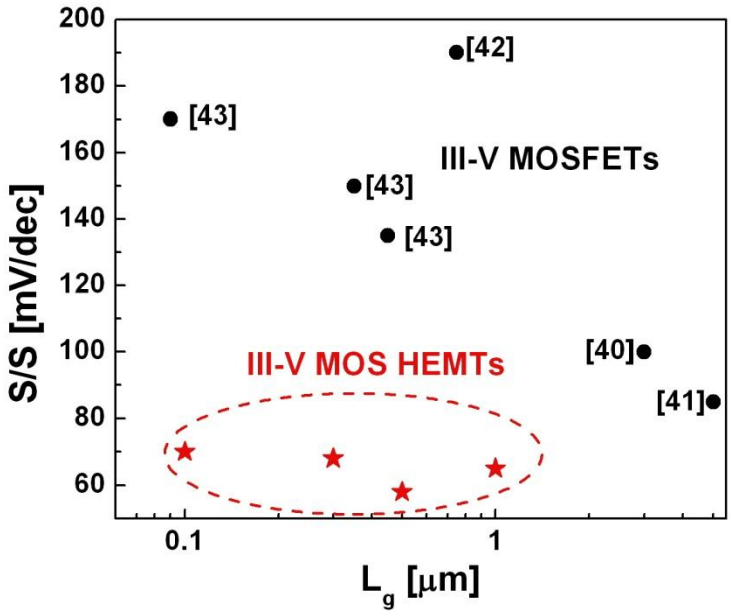


Figure 4.3 Benchmarking of the sub-threshold slope in III-V MOSFET and MOS HEMT[44]

4.2 Trap Assisted Tunneling in Tunnel FET

Tunnel FETs as discussed in the last chapter show a steep sub-threshold slope and is not degraded by the effect of the interface states. This steep sub-threshold slope in tunnel

FET result in higher I_{on}-I_{off} ratio compared to MOSFETs where the sub-threshold slope is limited to kT/q and is degraded more due to the presence of interface states. Recently, it was reported that the average sub-threshold slope is not sub-kT/q or sub-60 mV/dec but much higher and has a temperature dependence [45]. This arises because besides the direct band to band tunneling from the valence band in the p+ source region to the conduction band in the channel at the oxide-semiconductor interface, there is also a significant trap assisted tunneling component, especially at low gate voltages.

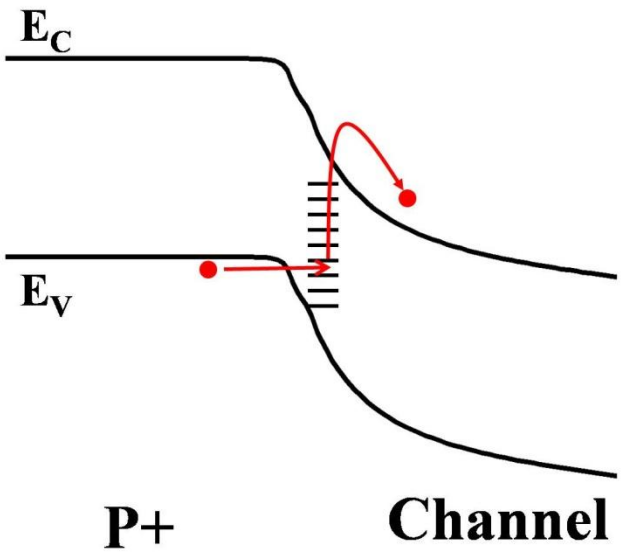


Figure 4.4 The trap assisted tunneling process at the oxide-semiconductor interface [45]

As shown in Figure 4.4, the trap assisted tunneling and its strong temperature dependence [45], arises because of carriers tunneling from the valence band in the p+ $In_{0.53}Ga_{0.47}As$ source region into the mid-gap traps and a subsequent thermal emission

into the conduction band in the channel region. This thermal emission gives rise of a strong temperature dependence and causes the degradation of the sub-threshold slope.

To further understand the impact of interface states on the sub-threshold response of tunnel FETs, trap assisted tunneling should be considered in detail and included in the simulation, also the effect of interface states at various temperature should be investigated.

APPENDIX I: MESHING THE DEVICE STRUCTURE

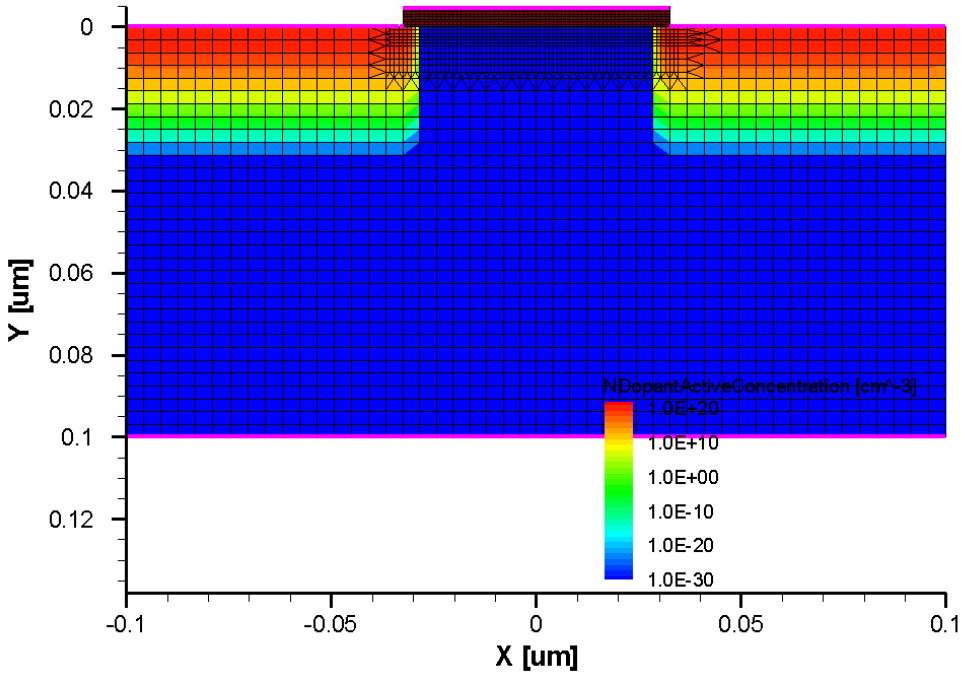


Figure A1 Two-dimensional inversion mode surface channel $In_{0.53}Ga_{0.47}As$ MOSFET with its current meshing and doping conditions

Figure A1 shows the meshing setup of the inversion mode surface channel $In_{0.53}Ga_{0.47}As$ MOSFET in the simulation. The mesh size in the $In_{0.53}Ga_{0.47}As$ substrate region is 3nm in both X and Y direction. In the oxide region, the mesh size is 2nm in the X direction and 0.5nm in the Y direction. A refinement window is also defined at the channel region under the oxide, in this refinement window, the mesh size is 2nm in the X direction and 1nm to in the Y direction.

APPENDIX II: CURRENT FLOW IN MOS HEMT

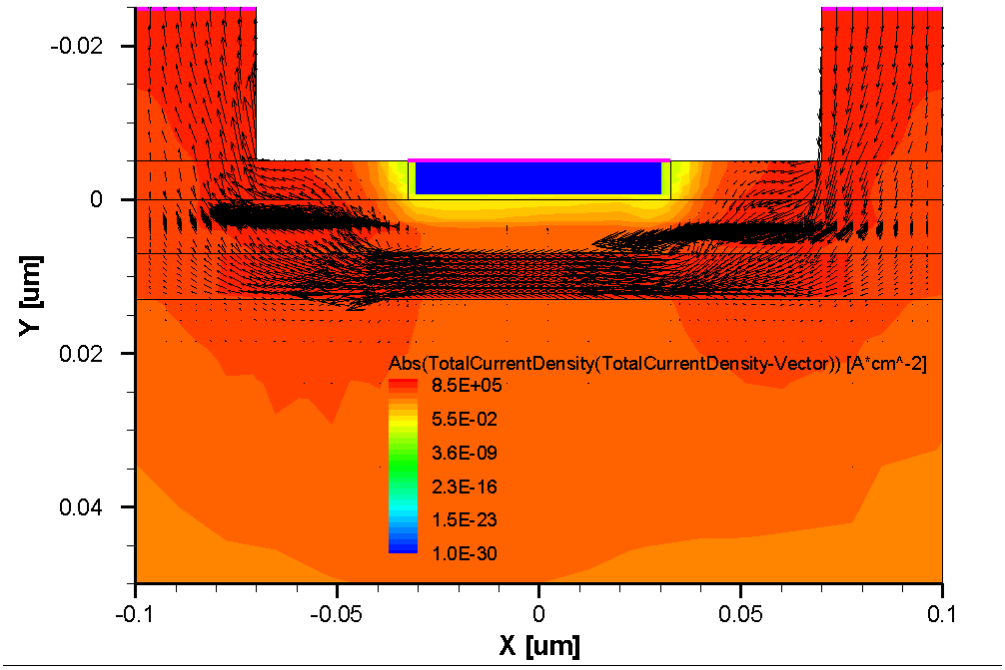


Figure A2 Two-dimensional accumulation mode buried channel InAs MOS HEMT with its current density at on-state

Figure A2 shows the current flow of the accumulation mode buried channel InAs MOS HEMT at on-state. In Figure A2, most of the current tunneled from the InP cap layer to the $In_{0.53}Ga_{0.47}As$ barrier layer and flows laterally alone the barrier layer then tunnel down to the InAs channel layer. The tunneling current is described by the barrier tunneling model.

REFERENCES

1. Yuan Taur, Tak H. Ning: "Fundamental of Mordern VLSI Devices", 1998
2. S. M. Sze and K. K. Ng: "Physics of Semiconductor Devices" 3rd ed., 2007
3. Harald Ibach, Hans Lüth: "Solid-state Physics: An Introduction to Principles of Materials Science" 3rd ed., 2003
4. J. Robertson and B. Falabretti, *J. Appl. Phys*. **100**, 014111, 2006
5. E. H. Nicollian and A. Goetzberger: "MOS Conductance Technique for MeasuringSurface State Parameters," *Appl. Phys. Lett* **7**, 216, 1965
6. E. H. Poindexter, G. J. Gerardi, M.-E. Rueckel, P. J. Caplan, N. M. Johnson, D. K. Biegelsen: "Electronic traps and P_b centers at the Si/SiO_2 interface: Band-gap energy distribution," *J. Appl. Phys.* **56**, 2844, 1984
7. P. D. Ye: "Main determinants for III-V metal-oxide-semiconductor field-effect-transistors," *J. Vac. Sci. Technol.* A **26**,697, 2008
8. Y. Xuan, P.D. Ye, and T. Shen: "Substrate engineering for high-performance surface-channel III-V metal-oxide-semiconductor field-effect transistors," *Appl. Phys. Lett.* **91**, 232107, 2007
9. J. Robertson: "Model of interface states at III-V oxide interfaces," *Appl. Phys. Lett.* **94**, 152104, 2009
10. J. R. Chelikowsky and M. L. Cohen: "Self-consistent pseudopotential calculation for the relaxed (110) surface of GaAs," *Phys. Rev. B* **20**, 4150, 1979

11. W. E. Spicer, I. Lindau, P. Skeath, C. Y. Su, and Patrick Chye: "Unified Mechanism for Schottky-Barrier Formation and III-V Oxide Interface States," *Phys. Rev. Lett.* **44**, 420, 1980
12. W. Walukiewicz: "Mechanism of Fermi-level stabilization in semiconductors," *Phys. Rev. B* **37**, 4760, 1988
13. J. Robertson: "Interface states model for III-V oxide interfaces," *Microelectronic Engineering* **86**, 1558-1560, 2009
14. S. B. Zhang, Su-Huai Wei, and Alex Zunger: "A phenomenological model for systematization and prediction of doping limits in II–VI and I–III–VI_2 compounds" *J. Appl. Phys.* **83**, 3192, 1998
15. E. P. O'Reilly and J. Robertson: "Electronic structure of amorphous III-V and II-VI compound semiconductors and their defects," *Phys. Rev. B* **34**, 8684, 1984
16. L.M. Terman: "An investigation of surface states at a silicon/silicon oxide interface employing metal-oxide-silicon Diode," *Solid-State electron*. **5**, 285, 1962
17. C.N. Berglund: "Surface states at steam-grown silicon-silicon dioxide interfaces," *IEEE Trans. Electron Dev.*, **13**, 701, 1966
18. R. Castagne and A. Vapaille: "Description of the SiO_2---Si interface properties by means of very low frequency MOS capacitance Measurements," *Suface Sci.*, **28**, 157, 1971
19. E. H. Nicollian and A. Goetzberger: "The Si-SiO_2 Interface – Electrical Properties as Determined by the Metal-Insulator-Silicon Conductance Technique," *Bell Syst. Tech. J.* 46, 1055-1133, 1967

20. Dieter K. Schroder: “Semiconductor Material and Device Characterization,” 3rd ed., 2006
21. G. DeClerck: “Characterization of Surface States at the Si-SiO_2 Interface,” in Nondestructive Evaluation of Semiconductor Materials and Devices (J.N. Zemel ed.), *Plenum Press*, 105-148, 1979
22. M. Schulz: “Interface States at the SiO_2-Si Interface,” Surf. Sci. **132**, 422-455, 1983
23. A.K. Aggarwal and M.H. White: “On the nonequilibrium statistics and small signal admittance of Si-SiO_2 interface traps in the deep-depleted gated-diode Structure,” *J. Appl. Phys.* **55**, 3682-3694, 1984
24. Eric M. Vogel, W. Kirklen Henson, Curt A. Richter and John S. Suehle: “Limitations of Conductance to the Measurement of the Interface State Density of MOS Capacitors with Tunneling Gate Dielectrics,” *IEEE Trans. Electron Dev*. **47**, 601-608, 2000
25. T. P. Ma and R. C. Barker: “Surface-state Spectra from thick-oxide MOS Tunnel Junctions,” *Solid-State electron*. **17**, 913-929
26. E. H. Nicollian and J.R. Brewes: “MOS Physics and Technology,” 1982
27. A.Ali , H. Madan, S. Koveshnikov, S. Oktyabrsky, R. Kambhampati, T. Heeg, D. Schlom and S. Datta: “Small Signal Response of Inversion Layers in High Mobility $In_{0.53}Ga_{0.47}As$ MOSFETs Made with Thin High-k Dielectrics," *IEEE Trans. Electron Dev*. **25**, 271-284, 2010

28. Y. Xuan, Y. Wu, and P. Ye: "High-performance inversion-type enhancement-mode InGaAs MOSFET with maximum drain current exceeding 1 A/mm," *IEEE Electron Device Lett.*, **29**, 294, 2008
29. S. Koveshnikov, N. Goel, P. Majhi, C. K. Gaspe M. B. Santos, S. Oktyabrsky, V. Tokranov, M. Yakimov, R. Kambhampati, H. Bakhru, F. Zhu, J. Lee, W. Tsai: "High Electron Mobility (2270 cm_2/Vsec) In0.53Ga0.47As Inversion Channel N-MOSFETs with ALD ZrO2 Gate Oxide Providing 1 nm EOT," *66th Device Research Conf. Digest*, 43-44, 2008
30. H. Zhao, Y. Chen, J. H. Yum, Y. Wang, N. Goel, and J. C. Lee: "High performance In0.7Ga0.3As metal-oxide-semiconductor transistors with mobility > 4400 cm2/Vs using InP barrier layer," *Appl. Phys. Lett.*, **94**, 193502, 2009
31. A. Ali , H. Madan, S. Koveshnikov, S. Oktyabrsky, R. Kambhampati, T. Heeg, D. Schlom and S. Datta: "Small Signal Response of Inversion Layers in High Mobility $In_{0.53}Ga_{0.47}As$ MOSFETs Made with Thin High-k Dielectrics," *ECS Transactions*, **25**, 271-284, 2009
32. Suman Datta, G. Dewey, J. M. Fastenau, M. K. Hudait, D. Loubychev, W. K. Liu, M. Radosavljevic, W. Rachmady, and R. Chau: "Ultrahigh-Speed 0.5 V Supply Voltage $In_{0.7}Ga_{0.3}As$ Quantum-Well Transistors on Silicon Substrate," *Electron Device Letters*, **28**, 685, 2007
33. S. Datta, T. Ashley, J. Brask, L. Buckle, M. Doczy, M. Emeny, D. Hayes, K. Hilton, R. Jefferies, T. Martin, T. J. Phillips, D. Wallis, P. Wilding and R. Chau: "85nm gate length enhancement and depletion mode InSb quantum well

transistors for ultra high speed and very low power digital logic applications," *Electron Devices Meeting, IEEE IEDM Technical Digest*, 763-766, 2005

34. S. Mookerjea, S. Datta: "Comparative Study of Si, Ge and InAs based Steep SubThreshold Slope Tunnel Transistors for 0.25V Supply Voltage Logic Applications," *Device Research Conference*, 47-48, 2008
35. Radosavljevic, B. Chu-Kung, S. Corcoran, G. Dewey, M. K. Hudait, J. M. Fastenau, J. Kavalieros, W. K. Liu, D. Lubyshev, M. Metz, K. Millard, N. Mukherjee, W. Rachmady, U. Shah and R. Chau: "Advanced High-K Gate Dielectric for High-Performance Short-Channel In0.7Ga0.3As Quantum Well Field Effect Transistors on Silicon Substrate for Low Power Logic Applications," *IEEE IEDM Technical Digest*, 13.1.1-13.1.4, 2009
36. D. M. Caughey and R. E. Thomas: "Carrier Mobilities in Silicon Empirically Related to Doping and Field," *Proceedings of the IEEE*, **55**, 2192–2193, 1967
37. G. Masetti, M. Severi, and S. Solmi: "Modeling of Carrier Mobility Against Carrier Concentration in Arsenic-, Phosphorus- and Boron-Doped Silicon," *IEEE Transactions on Electron Devices*, **ED-30**, 764–769, 1983
38. E L Heasell: "A technique for the observation of interface trap densities in MOSFET devices," Semicond. Sci. Technol., **3**, 35-39, 1988
39. R. J.W. Hill, X. Li, H.Zhou, D.S. Macintyre, S. Thoms, M.C. Holland, P. Longo, D.A.J. Moran, A.J. Craven, C.R. Stanley, A. Asenov, R.Droopad, M. Passlack and I.G. Thayne: "Deep sub-micron and self-aligned flatband III–V MOSFETs," *Device Research Conference*, 251, 2009

40. S. Koveshnikovl, N. Goell, P. Majhit, C. K. Gaspe, M. B. Santos, S. Oktyabrsky, V. Tokranov, M. Yakimov, R. Kambhampati, H. Bakhru, F. Zhu, J. Lee, and W. Tsai: "High Electron Mobility (2270 cm^2/Vsec) In0.53Ga0.47As Inversion Channel N-MOSFETs with ALD ZrO2 Gate Oxide Providing 1 nm EOT," *Device Research Conference*, 43, 2008
41. H. Zhao, D. Shahrjerdi, F. Zhu, H. Kim, I. OK, M. Zhang J.H. Yum, S.K. Banerjee and J. C. Lee" "Inversion-type indium phosphide metal-oxide-semiconductor field-effect transistors with equivalent oxide thickness of 12 angstrom using stacked HfAlOx/HfO2 gate dielectric," *Appl Phys Lett* **92** 253506, 2008
42. Y. Xuan, T. Shen, M. Xu, Y.Q. Wu and P.D. Ye: "High Performance Surface Channel In-rich $In_{0.75}Ga_{0.25}As$ MOSFETs with ALD High-k as Gate Dielectric," *IEEE IEDM Technical Digest*. 371-374, 2008
43. N. Goel, D. Heh, S. Koveshnikov, I. Ok, S. Oktyabrsky, V. Tokranov R. Kambhampati, M. Yakimov, Y. Sun, P. Pianetta, C.K. Gaspe, M.B. Santos, J. Lee, S. Datta, P. Majhi, and W. Tsai: "Addressing the gate stack challenge for high mobility InxGa1-xAs channels for NFETs," *IEEE IEDM Technical Digest* 367, 2008
44. W.C. Kao, A. Ali, E. Hwang, S. Mookerjea and S. Datta: Impact of Interface States on Sub-threshold Response of III-V MOSFETs, MOS HEMTs and Tunnel FETs," *IEEE Semiconductor Interface Specialists Conference*, 2009

45. S. Mookerjea, D. Mohata, T. Mayer, V. Narayanan and S. Datta: “Temperature Dependent I-V Characteristics of a Vertical $In_{0.53}Ga_{0.47}As$ Tunnel FET (TFET),” *IEEE Electron Device Letters*, 2010