Suman Datta
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Education

PhD, Electrical and Computer Engineering Dept., University of Cincinnati, OH, September 1999

BS, Electrical Engineering Dept., Indian Institute of Technology, Kanpur, India, June 1995

Experience

Professor (2011-present)

Department of Electrical Engineering, Penn State University, PA

Monkowski Associate Professor (2007-present)

Department of Electrical Engineering, Penn State University, PA

Principal Engineer (2005-2007)

Logic Technology Development, Intel Corporation, Hillsboro, OR

Senior Staff Engineer (2003-2005)

Logic Technology Development, Intel Corporation, Hillsboro, OR

Staff Engineer (2002-2003)

Logic Technology Development, Intel Corporation, Hillsboro, OR

Senior Process Engineer (1999-2002)

Logic Technology Development, Intel Corporation, Hillsboro, OR

Technology CAD (TCAD) Engineer (1999)

Avanti Corporation (now Synopsis), Fremont, CA

Research Highlights

Funding to date (Candidate's share = $2,858,927 out of $5,952,666):

– The Midwest Institute for Nanoelectronics Discovery: Energy Efficient Transistor and Architecture Center (2007-2012)

– 4 NSF grants

– 1 DARPA, 1 NSA and 1ONR grants

– 7 Industry grants

Total number of publications to date: 38 journal, 58 conference (96 total; h-index: 20)

Total number of graduate students to date: Postdoctoral: 1 completed, 1 current;

PhD: 2 graduated, 9 current (including 2 IBM Ph.D. Fellows); MS: 4 graduated (with thesis option), 3 current

Total number of issued United States patents: 126

Main Research Interests

Solid-state Device Physics

Energy efficient Nanoelectronic Transistors for CMOS ULSI applications

Quantum Electronics for post-CMOS ULSI applications

Terahertz Electronics

Co-Integration of Multiferroics with CMOS for Functional Diversification

Correlated Electron Devices

Co-Design of Emerging Devices, Circuits and System Architecture

Accomplishments

- At Penn State, Datta's group has successfully integrated an advanced high-k dielectric gate stack with the mixed arsenide-antimonide quantum-well to demonstrate, for the first time, high-k gated InAsSb QWFETs operating with high drive current under 500 millivolt supply voltage. The research results, which will be presented in the 2010 International Electron Device Meeting Conference (IEDM), showcase the possibility of a new generation of mixed arsenide-antimonide based "green" transistors that may form the building blocks of future ULSI systems consuming 10 times less energy that today's state-of-the-art silicon MOSFETs.

- At Penn State, Datta's group demonstrated the world's first vertical inter-band tunnel transistor in the compound semiconductor system. The tunnel transistor with 100 nm channel length, fabricated at the Penn State Nanofabrication facility, exhibited gated negative differential resistance in its output characteristics and achieved the highest on-current for any tunnel FET in any material system till date. The experimental and modeling results were presented as a late news paper at the 2009 IEEE International Electron Device Meeting (IEDM) and was selected by the IEDM technical program committee as a publicity paper. Tunnel transistor logic is being pursued as an energy efficient alternate transistor architecture in the post CMOS era.

- Datta has made significant technical contributions in the research on using III-V compound semiconductor as a high-mobility channel material and also integrating III-V devices on silicon substrate for future high-speed and low-power logic applications. He and his team from Intel and QinetiQ demonstrated the world's FIRST enhancement mode and depletion mode indium antimonide based quantum-well transistors operating at room temperature with record low energy-delay product. This work, which Datta presented at the 2005 International Electron Device Meeting (IEDM),sparked world-wide interest in pursuing high-mobility modulation doped compound semiconductor heterostructures for future ultra low-power and high-speed digital logic applications. Subsequently, in 2007, Datta and his team from Intel and IQE demonstrated the world's first indium gallium arsenide based n-channel quantum-well transistors ON SILICON SUBSTRATE operating under 500 mV supply voltage resulting in two orders of magnitude improvement in energy-delay product performance over state-of-the-art silicon transistors. Datta's ground breaking experimental work in demonstrating the logic suitability of arsenide and antimonide based quantum-well transistors and their successful heterogeneous integration on silicon substrate has resulted in vigorous global research activity in III-V transistors for logic computation today in both industry and academia.

- At Intel, Datta was the first researcher to demonstrate advanced high performance NMOS and PMOS transistors which successfully integrated high-k dielectric, metal gate electrode and strained transistor channel. Specifically, he demonstrated that a tensile strained silicon channel to enhance electron mobility and a compressively strained silicon germanium channel to boost hole mobility PMOS, could be employed in conjunction with high-k/metal gate stack to significantly improve CMOS transistor performance. This

ground breaking experimental research which Datta presented at the 2003 International Electron Device Meeting (IEDM) was the first experimental demonstration of using the screening effect of metal gate plasmons and channel strain engineering to recover completely the otherwise degraded channel mobility in CMOS transistors from the remote soft optical phonon scattering from the high-k dielectric. This work also showed that the benefits of high-K/metal-gate and strained channels (Si and SiGe channels) are indeed additive. Datta's IEDM presentation sparked much excitement in both industry and academia. In 2004 Datta was recognized with the Intel Achievement Award (the highest technical award given at Intel) for his outstanding technical contributions to high-K/metal-gate transistors.

- Datta has made significant contributions to the research on non-planar Si transistor architecture. He co-invented a novel fully-depleted, non-planar Tri-gate CMOS transistor structure (see multiple granted U.S. patents) which exhibited near-ideal short-channel performance at highly scaled gate dimensions. Subsequently, he led the device physics, modeling and characterization effort to experimentally demonstrate NMOS and PMOS multi-gate transistors combining the excellent short channel behavior with record drive current performance. This work uniquely demonstrated, for the first time, that high levels of channel strain could be incorporated in the three-dimensional non-planar transistor configuration to benefit both top surface and sidewall channel conduction. This work was subsequently presented at the 2006 VLSI Technology Symposium and sparked vigorous interest in fully depleted, multiple gate non-planar transistor structures. Datta's research on characterization and analysis of high performance multi-gate transistors made a significant impact to the silicon industry as i)the results in the seminal 2006 VLSI paper showed, for the FIRST time, non-planar multigate CMOS architecture can simultaneously achieve both excellent electrostatics at reduced gate dimensions and high drive current performance and ii) this work has inspired many subsequent excellent work and technical presentations on similar topic from other researchers world-wide.

Funded Projects

MIND Center

- Energy Efficient Transistor and Architectures, (06/08-05/11), **Nanoelectronics Research Institute/Semiconductor Research Corporation (NRI/SRC)**, $525,920 (Total: $873,920 including PSU match of $348,000), (PI with T. Mayer, V. Narayanan, D. Schlom)(40% share)
- Midwest Institute for Nanoelectronics Discovery Project 1.5 (MIND 1.5) (04/11-12/31/12), **Nanoelectronics Research Institute/Semiconductor Research Corporation (NRI/SRC)**, $280,000 (PI with T. Mayer, V. Narayanan,)(50% share)

NSF

- Ultra-sensitive Magnetic Sensors Integrating the Giant Magnetoelectric Effect with MEMs and Advanced Microelectronics, (10/08-9/11), **National Science Foundation/Division of Electrical, Communications and Cyber Systems (NSF/ECCS)**, $352,273 (Co-PI with Q. Zhang (PI), EE, PSU and Q. Yang, Radiology, PSU Hershey Medical Center)(50% share)
- EMT/NANO:Co-Exploration of Device and System Architecture for Quantum NanoElectronics," (09/08-08/11), **National Science Foundation/Division of Computing and Communication Foundation (NSF/CCF)**, $200,020 (Co-PI with V. Narayanan (PI), EE, PSU)(50% share)

- Collaborative: Mixed Anion and Cation Based Transistor Architecture for Ultra-Low Power Complementary Logic Applications, (10/10-09/13), **National Science Foundation/ Division of Electrical, Communications and Cyber Systems (NSF/ECCS)**, $472,753 (PI with M. Hudait, EE, Virginia Tech)(50% share)
- MRSEC: Center for Nanoscale Science Supplement titled "Very Low Energy Dissipation Computing using Inter-band Tunneling Injected Non-equilibrium Ballistic Carriers," (10/10-09/13), **National Science Foundation/Nanotechnology Research** Institute (NSF/NRI), $300,000, (Co-PI with T. Mayer(PI), EE, PSU)(50% share)

DARPA and NSA

- Mixed Anion Arsenide-antimonide Channel Transistors with High-k Gate Stack, (11/09-10/12) **Semiconductor Research Corporation and Defense Advanced Research Projects Agency (SRC/DARPA),** $226,000 (PI)
- Architecture-Device Co-Design for Ultra-Low Power High Performance Design, (10/09-09/11), **National Security Agency (NSA),** $600,000 (Co-PI with V. Narayanan, EE, PSU)(50% share)

ONR

- Correlated Electron Switching Based Tunnel Transistors, (07/12-06/15) **Office of Naval Research (ONR),** $1,923,700 (PI with R. Engel-Herbert, Mat Sc., PSU, V. Gopalan, Mat Sc, PSU, D. Schlom, Mat. Sc. Cornell, and K. Rabe, Rutgers)(30%)

Industry

- Compound Semiconductor Based Heterojunction Tunnel Transistors for Ultra Low Power Logic Applications-Phase 2, (09/01/09-08/31/11), **Intel Corporation**, $170,000 (PI)
- Ultra-Low Resistance Ohmic Contacts for III-V Digital Logic, (04/01/09-05/01/11), **Intel Corporation**, $250,000 (Co-PI with S. Mohney, Mat. Sc., PSU)(50% share)
- Post CMOS circuits and architecture, (10/01/10-09/30/11), **External research Office (ERO), Intel Corporation**, $50,000 (PI)(100%)
- Sub-0.4V Logic Circuits with Steep Sub-threshold Slope Inter-band Tunnel FETs-Phase 2, (06/09-06/11) **Intel Corporation**, $70,000, (PI)(100%)
- Vcc scalability of III-V based heterojunction tunnel transistors -Phase 1, (09/08-08/09), **Intel Corporation**, $85,000 (sole PI)(100%)
- Sub-0.4V Logic Circuits with Steep Sub-threshold Slope Inter-band Tunnel FETs-Phase 1, (06/08-05/09) **Intel Corporation**, $35,000 (PI)(100%)
- Strained Ge and III-V Quantum-Well Device Characterization, (04/11 – 03/13), **Applied Materials**, $120,000(100%)
- Multi-Gate III-V QWFET, (04/11 – 03/14), **Global Foundries**, $165,000 (100%)

Awards and Honors

- Joseph Monkowsky Professorship for Faculty Early Career Development, The Pennsylvania State University (2007)
- Senior Member of IEEE Electron Devices Society (2006)
- Intel Achievement Award (the highest technical honor at Intel) for "developing the world's first high-K/metal gate CMOS transistors with record-setting performance" (2003)
- Divisional Achievement Award from the Intel Logic Technology Development Group for "invention and successful demonstration of high performance Tri-gate CMOS transistors" (2002)
- All India Rank of 124 (Eastern Zone Rank: 18) among 300,000 students who appeared for Indian Institute of Technology Joint Entrance Examination (IIT-JEE) (1995)

Research Supervision

Postdoctoral Researcher

- Donna Shen (Postdoctoral Associate 2009 University of South Florida, Tampa, FL; PhD 2008 Auburn University, AL): 08/10-Present (co-supervised with Prof. S. Mohney)

Doctoral Students

1. Zhao Feng: Ultra Sensitive Magnetic Sensors Integrating the Giant Magnetoelectric Effect with MEMS and Advanced Microelectronics (Post-comprehensive, 03/2009)
2. Ashkar Ali: Design and Fabrication of Ultra-low power and High Performance Quantum-well Transistors (Post-comprehensive, 07/2010)
3. Feng Li: Ultra-sensitive Chip-Scale Magnetometers (Post-comprehensive, 07/2010)
4. Srinidhi Kestur: Accelerating computationally intensive applications using Reconfigurable systems (Post-comprehensive, 09/2010)
5. Vinay Saripalli: Energy-delay estimation of emerging CMOS and non CMOS –based devices and Circuits (Post-comprehensive, 09/2010)
6. Euichul Hwang: Multi-gate III-V Metal Oxide Semiconductor FETs (Post-comprehensive, 08/2010)
7. Dheeraj Mohata: Vertical Nanopillar Tunnel FETs (Doctoral candidate)
8. Liu Lu: Quantum Transistor Based Logic Circuits (Doctoral candidate)
9. Bijesh R.: Nonequilibrium Transport in Tunnel Transistors (Start date: 09/2010)

MS Students

1. Himanshu Madan: Admittance Spectroscopy of III-V and Dielectric Interfaces from KHz to GHz frequencies (Thesis option)

2. Salil Mujumdar: Strain Engineering in Nanoscale Transistors (Thesis option)

3. Ashish Agrawal: Noise measurement and modeling of nanoscale devices (Thesis option)

Graduated Students (including Postdoctoral Researchers)

1. Tanmoy Maiti (Postdoctoral Associate) (08/09-08/10) (Currently, Assistant Professor at Indian Institute of Technology, Kanpur, India)

2. Ramakrishnan Krishnan, PhD, 12/2009: Reliability Effects Of Soft Errors and NBTI in Current and Emerging Digital Circuits (Currently, Senior Staff Engineer, Advanced Technology Platforms Group, Taiwan Semiconductor and Manufacturing Corp (TSMC), Hsinchu, Taiwan)

3. Saurabh Mookerjea, PhD, 08/2010: Simulation, Design and Fabrication of Tunnel Transistors with steep sub-threshold slopes (Currently, Senior Device Engineer, Logic Technology Development, Intel Corporation, Hillsboro, Oregon)

4. Wei-Chieh Kao, MS (Thesis), 05/2010: Impact of Non-ideal Interfaces on Transistor Performance (Currently, PhD student at Arizona State University)

5. Vikram Sampat Kumar, MS (Thesis), 04/15/2010: An FPGA-based Real Time Tracking For Indoor Environment

6. Srijith Rajamohan, MS (Thesis), 04/2010: A Neural Network based Classifier on the Cell Broadband Engine

7. Ashkar Ali, MS (Thesis), 03/2009: Transport in Silicon Quantum Dots Embedded in a Rare Earth Oxide (Currently, PhD student at Penn State)

8. Chad Ostrowski, BS (Honor's Thesis) 12/2009: Analytical Modeling of Tunnel Diodes

Publications

Book Chapters

[1] V. Saripalli, V. Narayanan and S. Datta, "Ultra Low Energy Binary Diagram Circuits Using Few Electron Transistors", *Lecture Notes of the Institute for Computer Sciences, Social Informatics and Telecommunications Engineering*, Springer Berlin Heidelberg, October 2009

[2] V. Eachempati, R. Das, V. Narayanan, Y. Xie, S. Datta and C. Das, "HeTERO: Hybrid Topology Exploration for RF based On Chip Networks", *Communication Architectures for System-on-Chip (SoC)*, CRC Press, September 2010

[3] S. Datta, D. Schlom, "Gate Oxides beyond SiO2", *Multifunctional Oxide Heterostructures*, Oxford University Press, September 2010

[4] S. Datta and A. Ali, “III-V MOSFETs”, *Future Intelligent Integrated Systems: New Paths to Augmented Silicon CMOS Technologies* , WSPC-Pan Stanford (Singapore), (to be published October 2011)

Journal Articles

[37] D. Mohata*, S. Mookerjea*, A. Agrawal*, Y. Li, T. Mayer, V. Narayanan, A. Liu and S. Datta, "Experimental Staggered-Source and N+ Pocket-Doped Channel III-V Tunnel Field-Effect Transistors and Their Scalabilities," Applied Physics Express, vol 4, pp. 024105, February 2011 (first, second and third authors are supervised by the candidate)

[36] A. Ali*, B. Bennett, B. Boos, H. Madan, A. Agrawal, P. Schiffer, R. Misra and S. Datta, , "Experimental Determination of Quantum and Centroid Capacitance in Arsenide-Antimonide Quantum-Well MOSFETs Incorporating Non-Parabolicity Effect," accepted for publication in IEEE Transactions on Electron Devices , vol. 58 , no. 5, pp. 1397, May 2011 (first author supervised by the candidate)

[35] L. Liu* and S. Datta, “A Generalized Scaling Length Theory for Double Gate Inter-band Tunnel FETs,” submitted to *IEEE Transactions on Electron Devices*, number of pages: 6, July 2010 (first author supervised by the candidate)

[34] E. Hwang*, S. Mookerjea*, M. K. Hudait and S. Datta “Scalability of In0.7Ga0.3As Quantum Well Field Effect Transistor Architecture for Logic Applications,” accepted for publication in *Solid-State Electronics*, number of pages: 6, Aug 2010 (first and second authors supervised by the candidate)

[33] W.C. Kao*, A. Ali*, E. Hwang*, S. Mookerjea* and S. Datta "Effect of interface states on sub-threshold response of III–V MOSFETs, MOS HEMTs and tunnel FETs", accepted for publication in *Solid-State Electronics*, August 2010 (First, second, third and fourth authors supervised by the candidate)

[32] A. Ali*, H. S. Madan*, A. P. Kirk, R. M. Wallace, D. A. Zhao, D. A. Mourey, M. K. Hudait, T. N. Jackson, B. R. Bennett, J. B. Boos, and S. Datta, “Fermi Level Unpinning of GaSb (100) using Plasma Enhanced Atomic Layer Deposition of Al2O3 Dielectric,” accepted for publication in *Applied Physics Letters*, number of pages: 3, August 2010 (First and second authors supervised by the candidate)

[31] V. Saripalli*, L. Liu*, S. Datta and V. Narayanan “Energy-Delay Analysis of Single Electron Transistor Based BDD Logic,” to appear in *Journal of Low Power Electronics*, Vol, 6, No. 3, pp. , October 2010 (First and second authors supervised by the candidate)(This paper will feature on the cover page of the journal)

[30] F. Li*, F. Zhao*, Q. M. Zhang, and S. Datta, "Low Frequency Voltage Mode Sensing of Magnetoelectric Sensor in Package," to appear in *Electronics Letters*, Vol. 46, No. 16, pp. August 2010 (First and second authors supervised by the candidate)

[29] S. Mookerjea*, D. Mohata*, T. Mayer, V. Narayanan, S. Datta, "Temperature-Dependent "Characteristics of a Vertical In0.53Ga0.47As Tunnel FET," *IEEE Electron Device Letters*, Vol. 31, No. 6, pp. 564-567, June 2010. (First and second authors supervised by the candidate)

[28] A. Ali*, H. Madan*, S. Koveshnikov, S. Oktyabrsky, R. Kambhampati, T. Heeg, D. Schlom, and S. Datta, "Small signal response of inversion layers in high mobility In0.53Ga0.47As MOSFETs made with thin high-k dielectrics," *IEEE Transactions on Electron Devices*, Vol. 57, No. 4, p. 742-748, April 2010. (First and second authors supervised by the candidate)

[27] B. Downey, S. Datta and S. Mohney, "Numerical study of reduced contact resistance via nanoscale topography at metal/semiconductor interfaces," *Semiconductor Science and Technology*, Vol. 25, No. 1, pp 1-4, January 2010. (Equal contributions by all authors)

[26] F. Li*, S. H. Lee, Z. Fang*, P. Majhi, Q. Zhang, S. K. Banerjee, and S. Datta, "Flicker Noise Improvement in 100 nm Lg Si0.50Ge0.50 Strained Quantum-Well Transistors using Ultra-Thin Si Cap Layer," *IEEE Electron Device Letters*, vol. 31, No. 1, pp. 47-49, January 2010. (First author supervised and third author co-supervised by the candidate)

[25] S. Mookerjea*, R. Krishnan*, S. Datta, and V. Narayanan, "On Enhanced Miller Capacitance in Inter-Band Tunnel Transistors," *IEEE Electron Device Letters*, Vol. 30, No. 10, pp. 1102-1104, October 2009. (First author supervised and second author co-supervised by candidate)

[24] A. Ali*, H. Madan*, S. Koveshnikov and S. Datta," Small Signal Response of Inversion Layers in High Mobility In0.53Ga0.47As MOSFETs Made with Thin High-k Dielectrics", *Electrochemical Society (ECS) Transactions*, Vol. 25, No. 6, pp. 271-284, Physics and Technology of High-k Gate Dielectrics, October 2009. (First and second authors supervised by the candidate)(Based on candidate's invited talk)

[23] S. Mookerjea*, R. Krishnan*, S. Datta, and V. Narayanan, "Effective Capacitance and Drive Current for Tunnel-FET (TFET) CV/I Estimation," *IEEE Transactions on Electron Devices*, Vol. 56, No. 9, pp. 2092-2098, September 2009. (First author supervised and second author co-supervised by candidate)

[22] Z. Fang*, S. G. Lu, F. Li*, S. Datta, and Q. M. Zhang, "Enhancing the Magnetoelectric Response of Metglas/Polyvinylidene fluoride Laminates by Exploiting the Flux Concentration Effect," *Applied*

Physics Letters, Vol. 95, No. 11, pp. 112903_1-112903_3, September 2009. (First author co-supervised and third author supervised by the candidate)

[21] S. Mookerjea*, R. Krishnan*, A. Vallett, T. Mayer and S. Datta, "Inter-band Tunnel Transistor Architecture using Narrow Gap Semiconductors", *ECS Transactions*, Vol 19, No. 5, Ge and III-V MOSFETs, pp. 287-292, May 2009. (First author co-supervised and third author supervised by the candidate) (Based on Invited Talk by the candidate)

[20] D. Schlom, S. Guha, and S. Datta, "Gate Oxides Beyond SiO2," *MRS Bulletin*, pp. 1017-1025, November 2008. (Equal contributions by all authors)

[19] S. H. Lee, P. Majhi, J. Oh, B. Sassman, C. Young, A. Bowonder, W. Y. Loh, J. J. Choi, B. J. Cho, H. D. Lee, P. Kirsch, H. R. Harris, W. Tsai, S. Datta, H. H. Tseng, S. K. Banerjee, and R. Jammy, "Demonstration of Lg 55 nm pMOSFETs With Si Si0.25Ge0.75 Si Channels, High Ion Ioff (5 × 104), and Controlled Short Channel Effects (SCEs)," *IEEE Electron Device Letters*, Vol. 29, No 9, pp. 1017-1020, September 2008. (Equal contribution by all authors)

[18] C. I. Kuo; H. T. Hsu, E. Y Chang, C. Y. Chang; Y. Miyamoto, S. Datta; M. Radosavljevic, G-W. Huang, and C. T. Lee, "RF and Logic Performance Improvement of In0.7Ga0.3As}/InAs/In0.7Ga0.3As Composite-Channel HEMT Using Gate-Sinking Technology," *IEEE Electron Device Letters*, Vol. 29, Issue 4, pp. 290-293, 2008. (Equal contribution by all authors)

[17] R. Chau, B. Doyle, S. Datta, K. Kavalieros, and K. Zhang, "Integrated nanoelectronics for the future," *Nature Materials*, Vol. 6, pp. 810-812, 2007. (Equal contribution by all authors

[16] S. Datta, G. Dewey, J. M. Fastenau, M. K. Hudait, D. Loubychev, W. K. Liu, M. Radosavljevic, W. Rachmady, and R. Chau, "Ultrahigh-Speed 0.5 V Supply Voltage In0.7Ga0.3As Quantum-Well Transistors on Silicon Substrate," *IEEE Electron Device Letters*, Vol. 28, No. 8, pp. 685, 2007. (Nominated for the George E. Smith award for the best 2007 EDL paper by IEEE Electron Devices Society)

[15] S. Datta, "III-V field-effect transistors for low power digital logic applications," *Journal of Microelectronic Engineering*, Vol. 84, No. 9-10, pp. 2133-2137, 2007. (Invited paper) (This paper is cited several times in the Emerging Research Devices section of the 2007 edition of the International Technology Roadmap for Semiconductors (ITRS). ITRS is a vital reference for the semiconductor industry and addresses the technology challenges and possible solutions for the industry over the next 15 years)

[14] C. Y. Chang, H. T. Hsu, E. Y. Chang, C. I. Kuo, S. Datta, M. Radosavljevic, M. Miyamoto, and G. W. Y. Huang, "Investigation of Impact Ionization in InAs-Channel HEMT for High-Speed and Low-

Power Applications," *IEEE Electron Device Letters*, Vol. 28, No. 10, pp. 856-858, 2007. (Equal contributions by all authors)

[13] T. Ashley, L. Buckle, S. Datta, M.T. Emeny, D.G. Hayes, K.P. Hilton, R. Jefferies, T. Martin, T.J. Phillips, D.J. Wallis, P.J. Wilding, and R. Chau, "Heterogeneous InSb quantum well transistors on silicon for ultra-high speed, low power logic applications," *Electronics Letters*, Vol. 43, No. 14, 2007. (Equal contribution by all authors)

[12] R. Chau, S. Datta, M. Doczy, B. S. Doyle, B. Jin, J. Kavalieros, A. Majumdar, M. Metz, and M. Radosavljevic, "Benchmarking nanotechnology for high-performance and low-power logic transistor applications," *IEEE Transactions on Nanotechnology*, Vol. 4, No. 2, pp. 153-158, 2005. (Equal contribution by all authors)

[11] R. Chau, J. Brask, S. Datta, G. Dewey, M. Doczy, B. Doyle, J. Kavalieros, B. Jin, M. Metz, A. Majumdar, and M. Radosavljevic, "Application of high-K gate dielectrics and metal gate electrodes to enable silicon and non-silicon logic nanotechnology," *Journal of MicroElectronic Engineering*, Vol. 80, No. 17, pp. 1-6, 2005. (Equal contribution by all authors)

[10] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, and M. Metz, "High-K/Metal-Gate Stack and its MOSFET Characteristics," *IEEE Electron Device Letters*, Vol. 25, No. 6, pp. 408-410, 2004. (Equal contribution by all authors)

[9] R. Chau, B. Boyanov, B. Doyle, M. Doczy, S. Datta, S. Hareland, B. Jin, J. Kavalieros, and M. Metz, "Silicon Nano-transistors for Logic Applications," *Physica E, Low-Dimensional Systems and Nanostructures*, Vol. 19, No. 1-2, pp. 1-5, 2003. (Equal contribution by all authors)

[8] B. S. Doyle, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalieros, T. Linton, A. Murthy, R. Rios, and R. Chau, "High Performance Fully-Depleted Tri-Gate CMOS Transistors," *IEEE Electron Device Letters*, Vol. 24, No. 4, pp. 263-265, 2003. (Equal contribution by all authors)

[7] S. Datta, K. P. Roenker, M. M. Cahay, and L. M. Lunardi, "Analytical Modeling of Pnp InP/InGaAs Heterojunction Bipolar Transistors," *Solid-State Electronics*, Vol. 44, No. 7, pp. 1331-1333, 2000.

[6] S. Datta, K. P. Roenker, and M. M. Cahay, "A Gummel-Poon Model for Pnp Heterojunction Bipolar Transistors with a Compositionally Graded Base," *Solid-State Electronics*, Vol. 44, No. 6, pp. 991-1000, 2000.

[5] S. Datta, K. P. Roenker, and M. M. Cahay, "Emitter Series Resistance Effect of Multiple Heterojunction Contacts for Pnp Heterojunction Bipolar Transistors," *Solid-State Electronics*, Vol. 43, No. 7, pp. 1299-1305, 1999.

[4] S. Datta, K. P. Roenker, and M. M. Cahay, "Hole Transport and Quasi-Fermi Level Splitting at the Emitter-Base Junction in Pnp Heterojunction Bipolar Transistors," *Journal of Applied Physics*, Vol. 85, No. 3, pp. 1949-1955, 1999.

[3] S. Datta, K. P. Roenker, and M. M. Cahay, "Implications of Hole versus Electron Transport Properties for High Speed Pnp Heterojunction Bipolar Transistors," *Solid-State Electronic*s, Vol. 43, No. 1, pp. 73-80, 1999.

[2] S. Datta, S. Shi, K. P. Roenker, and M. M. Cahay and W. E. Stanchina, "Simulation and Design of InAlAs/InGaAs Pnp Heterojunction Bipolar Transistors," *IEEE Transactions on Electron Devices*, Vol. 45, No. 8, pp. 1634-1643, 1998.

[1] S. Datta, K. P. Roenker, and M. M. Cahay, "A Thermionic-Emission-Diffusion Model for a Graded Base Pnp Heterojunction Bipolar Transistors," *Journal of Applied Physics*, Vol. 83, No. 12, pp. 8036-8045, 1998

Conference Proceedings Articles

[58] V. Saripalli*, J. P. Kulkarni, N. Vijaykrishnan and S. Datta, "Variation-Tolerant Ultra Low- Power Heterojunction Tunnel FET SRAM Design", accepted in IEEE/ACM Int. Symp. on Nanoscale Architectures (NANOARCH), San Diego, CA, June 2011 (first author supervised by the candidate)

[57] A. Agrawal, A. Ali, R. Misra, P. E. Schiffer, J. B. Boos, B. R. Bennett and S. Datta, "Low Field Electron Transport in Mixed Arsenide Antimonide Quantum Well Heterostructures", accepted for publication in Electronic Materials Conference (EMC), Univ. of California, Santa Barbara, June 2011 (first, second authors supervised by the candidate)

[56] A. Agrawal*, A. Ali*, R. Misra, P. E. Schiffer, B. R. Bennett, J. B. Boos and S. Datta, "Experimental Determination of Dominant Scattering Mechanisms in Scaled InAsSb Quantum Well", accepted for publication in Device Research Conference (DRC), Univ. of California, Santa Barbara, June 2011 (first, second authors supervised by the candidate)

[55] R.Bijesh*, I. OK, M. Baykan, C. Hobbs, P.Majhi, R.Jammy and S.Datta, "Hole Mobility Enhancement in Uniaxially Strained SiGe FINFETs: Analysis and Prospects", accepted for publication in Device Research Conference (DRC), Univ. of California, Santa Barbara, June 2011 (first author supervised by the candidate)

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Recent Invited Talks

Universities

[1] "Tunnel Transistor Based Energy Efficient Logic", *IEEE EDS Distinguished lecture series in Electronics/Photonics*, Ohio State University, Columbus, OH, 04/2010

[2] "Energy Efficient Logic Transistors using Compound Semiconductors" Cornell University Electron Devices Society Lecture Series, Cornell University, Ithaca, NY, 04/2010

[3] "Logic and Memory Design using Inter-band Tunnel Transistor" Nanoseminar Seminar Series, Arizona State University, 03/2010

[4] "Compound Semiconductor based Logic Elements" IEEE Electron Devices Mini Colloquium, Indian Institute of Technology, Mumbai, 01/2010

[5] "Ushering in the Green Transistor Era", Rochester Institute of Technology, Rochester, New York, 5/2009

[6] “Green Transistors to Green Architectures”, Institut für Materialien und Bauelemente der Elektronik, Leibniz Universität Hannover (University of Hannover), Hannover, Germany, 10/2009

[7] “Green Nanoelectronic Computing Devices”, as part of the annual workshop on Emerging Trends in Photonic and Electronic Device Research held sponsored by The University of Illinois chapters of the Optical Society of America (OSA) and the IEEE Electron Devices Society (EDS) in conjunction with the Micro and Nanotechnology Laboratory (MNTL), University of Illinois, Urbana Champagne, Illinois, 09/2008

[8] “Recent Advances in Silicon and Non-Silicon Nanoelectronic Devices for High-Performance, Energy Efficient Logic Applications”, Penn State University Computer Science and Engineering Colloquia Series, 11/2007

[9] “Emerging Nanoelectronic Devices for High-Speed and Ultra-Low Power Applications”, sponsored by the University of Wisconsin, Madison, Materials Research Science and Engineering Center (MRSEC) in association with Electrical Engineering Department University of Wisconsin, Madison, Wisconsin, 12/2006

[10] “Ultra Low Power Nanoelectronics for the Logic technology”, Taipei Local Chapter of IEEE Electron Devices Society (EDS), National Tchao-tung University (NCTU), Hsinshu, Taiwan:, 12/2006

[11] “Emerging Nanoelectronic Devices for High-Speed and Ultra-Low Power Application”, Electrical Engineering Colloquium, University of Texas, Austin, 3/2006

[12] “Silicon Nano-Transistors and Nanotechnology for High-Performance Logic Applications”, sponsored by the IEEE Phoenix Section Components, Packaging, and Manufacturing Technology Society Chapter, & Waves and Devices Chapter, Arizona State University, Tempe, Arizona, 11/2003

Government/Industry

[13] “Function Stacks for Logic and Memory Devices”, Invited Speaker at the SEMATECH's 7th International Symposium on Advanced Gate Stack Technology, in Albany, New York, 09/29/2010-10/01/ 2010

[14] “Non silicon logic elements for extreme voltage scaling “, Invited Speaker at the IBM MRC Workshop on III/V Devices IBM Research, Zurich, Switzerland, 09/2010

[15] “Binary Decision Diagram Logic for Single Electron Devices and Tunnel FETs”, Invited Speaker at the Nanoelectronics Research Initiative (NRI) sponsored Architecture & Device Benchmarking Workshop, University of Notre Dame, 08/09/2010

[16] “Tunnel Transistors: From Circuits to Architecture”, Invited Speaker at the Nanoelectronics Research Initiative (NRI) sponsored Architecture & Device Benchmarking Workshop, University of Notre Dame, 08/09/2010

[17] “High mobility channel MOSFETs: to include or not to include in the ITRS?”, Panelist at the Sematech/IMEC III-V Workshop for discussion on inclusion high mobility channel MOSFETs in the ITRS, Hilton Hawaiian Village, Honolulu, 06/2010

[18] “Green Transistors to Green Architectures”, Tutorial at the 16th IEEE International Symposium on High-Performance Computer Architecture (HPCA), Bangalore, India, 01/2010

[19] “High Mobility Channel MOSFETs”, Panelist at the Workshop for Future III-V Complementary Metal–Oxide–Semiconductor (CMOS) Technology, Washington DC , December 2009

[20] “Heterojunction Tunnel Transistor Logic,” Intel on-site NRI sponsored PI’s Workshop, Intel Corporation, Portland, Oregon, 8/2009

[21] “Tunnel Transistor Logic”, Intel Microprocessor Research Lab Seminar, Portland, Oregon, 10/09

[22] "Looking Beyond Silicon - A Pipe Dream or the Inevitable Next Step?” Panelist on the IEDM sponsored evening panel called (This panel assembled internationally recognized panelists to discuss the future of Complementary Metal-Oxide Semiconductor (CMOS) and beyond CMOS for leading-edge advanced integrated circuit applications”, 12/2007

[23] "III-V Complementary Metal-Oxide Semiconductor (CMOS) on Si: Technical and Manufacturing Needs” Panelist on the Sematech and Aixtron sponsored workshop on readiness of III-V MOSFET Technology. This workshop received world-wide press coverage under the heading “III-V Compounds Emerging as Prime Materials for Future NMOS Channels, Technologists Indicate at SEMATECH & AIXTRON Workshop,” Washington, D.C., 12/2007

Invention

[110] US Patent # 7825481 “Field effect transistor with narrow bandgap source and drain regions and method of fabrication,” R. Chau, S. Datta, J. Kavalieros, J. Brask, M. Doczy, Nov 02, 2010.

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[107] US Patent # 7820513 "Nonplanar semiconductor device with partially or fully wrapped around gate electrode and methods of fabrication," S. Hareland, R. Chau, B. Doyle, R. Rios, T. Linton, S. Datta, Oct 26, 2010.

[108] US Patent # 7820512 "Spacer patterned augmentation of tri-gate transistor gate length," R. Pillarisetty, S. Datta, J. Kavalieros, B. Doyle, U. Shah, Oct 26, 2010.

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[105] US Patent # 7785958 "Method for making a semiconductor device having a high-k gate dielectric layer and a metal gate electrode," M. Doczy, J. Brask, J. Kavalieros, U. Shah, M. Metz, S. Datta, R. Nagisetty, R. Chau, Aug 31, 2010.

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[103] US Patent # 7736956 "Lateral undercut of metal gate in SOI device," S. Datta, J. Brask, J. Kavalieros, B. Doyle, G. Dewey, M. Doczy, R. Chau, June 15, 2010.

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[100] US Patent # 7713803 "Mechanism for forming a remote delta doping layer of a quantum well structure," B. Jin, J. Kavalieros, S. Datta, A. Majumdar, R. Chau, B. Jin, May 11, 2010

[99] US Patent # 7709909 "Method for making a semiconductor device having a high-k gate dielectric," M. Doczy, G. Dewey, S. Datta, S. Pae, J. Brask, J. Kavalieros, M. Metz, A. Sherrill, M. Kuhn, R. Chau, May 04, 2010.

[98] US Patent # 7704833 "Method of forming abrupt source drain metal gate transistor," N. Lindert, S. Datta, J. Kavalieros, M. Doczy, M. Metz, J. Brask, R. Chau, M. Bohr, A. Murthy, April 27, 2010.

[97] US Patent # 7671471 "Method for making a semiconductor device having a high-k dielectric layer and a metal gate electrode," J. Brask, J. Kavalieros, M. Doczy, U. Shah, C. Barnes, M. Metz, S. Datta, A. Cappellani, R. Chau, March 03, 2010.

[96] US Patent # 7642610 "Transistor gate electrode having conductor material layer," A. Murthy, B. Boyanov, S. Datta, B. Doyle, B. Jin, S. Yu, R. Chau, January 05, 2010.

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[91] US Patent # 7608883 "Transistor for non volatile memory devices having a carbon nanotube channel and electrically floating quantum dots in its gate dielectric" M. Radosavljevic, A. Majumdar, S. Datta, J. Brask, B. Doyle, R. Chau, October 27, 2009

[90] US Patent # 7601980 "Dopant confinement in the delta doped layer using a dopant segregation barrier in quantum well structures" M. Hudait, A. Budrevich, D. Loubychev, J. Kavalieros, S. Datta, J. Fastenau, A. Liu, October 13, 2009

[89] US Patent # 7598560 "Hetero-bimos injection process for non-volatile flash memory," J. Kavalieros, S. Datta, R. Chau, D. Kencke, October 6, 2009.

[88] US Patent # 7592213 "Tensile strained NMOS transistor using group III-N source/drain regions," S. Datta, J. Brask, B. Jin, J. Kavalieros, M. Hudait, September 22, 2009.

[87] US Patent # 7575991 "Removing a high-k gate dielectric," M. Doczy, R. Norman, J. Brask, M. Metz, S. Datta, R. Chau, August 18, 2009.

[86] US Patent # 7569857 "Dual crystal orientation circuit devices on the same substrate," P. Tolchinsky, J. Kavalieros, B. Doyle, S. Datta, August 4, 2009.

[85] US Patent # 7569869 "Transistor having tensile strained channel and system including same," B. Jin, R. Chau, S. Datta, J. Kavalieros, M. Radosavljevic, August 4, 2009.

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[82] US Patent # 7547637 "Methods for patterning a semiconductor film," J. Brask, J. Kavalieros, U. Shah, S. Datta, A. Majumdar, R. Chau, B. Doyle, June 16, 2009.

[81] US Patent # 7531393 "Non-planar MOS structure with a strained channel region," B. Doyle, S. Datta, B. Jin, R. Chau, May 12, 2009.

[80] US Patent # 7531404 "Semiconductor device having a metal gate electrode formed on an annealed high-k gate dielectric layer," S. Pae, J. Maiz, J. Brask, G. Dewey, J. Kavalieros, R. Chau, S. Datta, May 12, 2009.

[79] US Patent # 7524727 "Gate electrode having a capping layer," G. Dewey, M. Doczy, S. Datta, J. Brask, M. Metz, April 28, 2009.

[78] US Patent # 7525160 "Multigate device with recessed strain regions," J. Kavalieros, J. Brask, S. Datta, B. Doyle, R. Chau, April 28, 2009

[77] US Patent # 7514346 "Tri-gate devices and methods of fabrication," R. Chau, B. Doyle, J. Kavalieros, D. Barlage, S. Datta, April 14, 2009.

[76] US Patent # 7518196 "Field effect transistor with narrow bandgap source and drain regions and method of fabrication," R. Chau, S. Datta, J. Kavalieros, J. Brask, M. Metz, April 14, 2009.

[75] US Patent # 7514746 "Floating-body dynamic random access memory and method of fabrication in tri-gate technology," S. Tang, A. Keshavarzi, D. Somasekhar, F. Paillet, M. Khellah, Y. Ye, S. Lu, B. Doyle, S. Datta, V. De, April 7, 2009.

[74] US Patent # 7504678 "Tri-gate devices and methods of fabrication," R. Chau, B. Doyle, J. Kavalieros, D. Barlage, S. Datta, March 17, 2009.

[73] US Patent # 7501336 "Metal gate device with reduced oxidation of a high-k gate dielectric," B. Doyle, J. Kavalieros, J. Brask, M. Metz, M. Doczy, S. Datta, R. Chau, March 10, 2009.

[72] US Patent # 7569443 "Complementary metal oxide semiconductor integrated circuit using raised source drain and replacement metal gate," J. Kavalieros, A. Cappellani, J. Brask, M. Doczy, S. Datta, C. Barnes, R. Chau, January 20, 2009.

[71] US Patent # 7494862 "Methods for uniform doping of non-planar transistor structures," B. Doyle, R. Chau, S. Datta, J. Kavalieros, February 24, 2009.

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[68] US Patent # 7465976 "Tunneling field effect transistor using angled implants for forming asymmetric source/drain regions," J. Kavalieros, M. Metz, G. Dewey, B. Jin, S. Datta, R. Chau, December 16, 2008.

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[64] US Patent # 7449373 "Method of ion implanting for tri-gate devices," B. Doyle, S. Datta, J. Kavalieros, A. Majumdar, November 11, 2008.

[63] US Patent # 7449756 "Semiconductor device with a high-k gate dielectric and a metal gate electrode or fully wrapped around gate electrode and methods of fabrication," M. Metz, S. Datta, M. Doczy, J. Brask, J. Kavalieros, R. Chau, November 11, 2008.

[62] US Patent # 7445980 "Method and apparatus for improving stability of a 6T CMOS SRAM cell," S. Datta, B. Doyle, R. Chau, B. Jin, J. Kavalieros, B. Zheng, S. Hareland, November 4, 2008.

[61] US Patent # 7442983 "Method for making a semiconductor device having a high-k gate dielectric," M. Doczy, G. Dewey, S. Datta, S. Pae, J. Brask, J. Kavalieros, M. Metz, A. Sherrill, M. Kuhn, R. Chau, October 28, 2008.

[60] US Patent # 7439113 "Forming dual metal complementary metal oxide semiconductor integrated circuits," M. Doczy, M. Taylor, J. Brask, J. Kavalieros, S. Datta, M. Metz, R. Chau, J. Hwang, October 21, 2008.

[59] US Patent # 7427794 "Tri-gate devices and methods of fabrication," R. Chau, B. Doyle, J. Kavalieros, D. Barlage, S. Datta, S. Hareland, September 23, 2008.

[58] US Patent # 7429747 "Sb-based CMOS devices," M. Hudait, S. Datta, J. Kavalieros, M. Doczy, R. Chau, September 30, 2008.

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[21] US Patent #7138316 "Semiconductor channel on insulator structure," B. Jin, B. Doyle, S. Hareland, M. Doczy, M. Metz, Matthew, B. Boyanov, S. Datta, J. Kavalieros, R. Chau, November 21, 2006.

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[11] US Patent #7045428 "Method for making a semiconductor device with a high-k gate dielectric and a conductor that facilitates current flow across a P/N junction," J. Brask, J. Kavalieros, M. Doczy, M. Metz, U. Shah, C. Barns, S. Datta, R. Turkot, R. Chau, May 16, 2006.

[10] US Patent #7042009 "High mobility tri-gate devices and methods of fabrication," M. Shaheen, B. Doyle, S. Datta, R. Chau, P. Tolchinsky, May 9, 2006.

[9] US Patent #7005366 "Tri-gate devices and methods of fabrication," R. Chau, B. Doyle, J. Kavalieros, D. Barlage, S. Datta, S. Hareland, February 28, 2006.

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[6] US Patent #6787440 "Method for making a semiconductor device having an ultra-thin high-k gate dielectric," C. Parker, M. Kuhn, Y. Zhou, S. Hareland, S. Datta, N. Lindert, R. Chau, T. Glassman, M. Metz, S. Tyagi, September 7, 2005.

[5] US Patent #6914295 "Tri-gate devices and methods of fabrication," R. Chau, B. Doyle, J. Kavalieros, D. Barlage, S. Datta, S. Hareland, July 5, 2005.

[4] US Patent #6909151 "Nonplanar device with stress incorporation layer and method of fabrication," S. Hareland, R. Chau, B. Doyle, S. Datta, B. Jin, June 21, 2005.

[3] US Patent #6887800 "Method for making a semiconductor device with a high-k gate dielectric and metal layers that meet at a P/N junction," M. Metz, S. Datta, J. Kavalieros, M. Doczy, J. Brask, U. Shah, R. Chau, May 3, 2005.

[2] US Patent #6869889 "Etching metal carbide films," J. Brask, J. Kavalieros, M. Doczy, M. Metz, S. Datta, U. Shah, T. Bacuita, R. Chau, March 22, 2005.

[1] US Patent #6858478 "Tri-gate devices and methods of fabrication," R. Chau, B. Doyle, J. Kavalieros, D. Barlage, S. Datta, S. Hareland, February 22, 2005.

Professional Activities

Senior Member, IEEE

Member, *Executive Committee, Electronics and Photonics Division, the Electrochemical Society (ECS),* September 2009-present

Member, *Executive Committee, Mid-West Institute for Nanoelectronics Discovery (MIND),* 2008-present

Member, *"Front End Processes" Tab and contributor to the 2003 Version of the International Technology Roadmap for Semiconductors (ITRS)*

Member, *American Society for Engineering Education,* 2007 – Present

Associate Editor, *Association for Computing Machinery (ACM) Journal of Emerging Technologies in Computing Systems (JETC),* February 2010 - Present

TPC Vice-Chair, *IEEE Device Research Conference (DRC),* University of California, Santa Barbara, CA, June 2011

Chair, *Quantum, Power, and Compound Semiconductor Devices Sub-Committee, IEEE International Electron Devices Meeting (IEDM '10),* San Francisco, California, December 2010

Organizer and Chair, *Rump Session on Embedded Memory called "Looking for Extra Cache", IEEE Device Research Conference (DRC '10),* Univ. of Notre Dame, June 2010

Organizer and Chair, *Rump Session on Steep Slope Transistors called "Steep Slope or Slippery Slope", IEEE Device Research Conference (DRC '10),* Penn State University, June 2009

TPC Member, *IEEE Device Research Conference (DRC '10),* Univ. of Notre Dame, June 2010

TPC Member, *Electronic Materials Conference (EMC '10),* Univ. of Notre Dame, June 2010

TPC Member, *Semiconductor Interface Specialist Conference (SISC '10)*, San Diego, California, December2010

TPC Member, *European Solid-State Device Research Conference (ESSDERC '09)*, Seville, Spain, September, 2010

TPC Member, *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED '10)*, Austin, Texas, August 2009

TPC Member, *European Solid-State Device Research Conference (ESSDERC '09)*, Athens, Greece, September, 2009

TPC Member, *Quantum, Power, and Compound Semiconductor Devices, IEEE International Electron Devices Meeting (IEDM '09)*, Baltimore, Maryland, December 7– 9, 2009

TPC Member, *IEEE Device Research Conference (DRC '09),* Penn State Univ., June 2009

TPC Member, *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED '09)*, San Francisco, California, August 2009

TPC Member, *European Solid-State Device Research Conference (ESSDERC '09)*, Edinburgh, Scotland, September 2008

TPC Member, *Silicon Nanoelectronics Workshop (SNW '08)*, Honolulu, Hawaii, June 2008

TPC Member, *International Symposium on VLSI Technology, Systems, and Applications (2005 IEEE VLSI-TSA)*, Hinshu, Taiwan, April 25-27, 2005

Arrangements Chair, IEEE *Device Research Conference (DRC)*, Penn State University, June 2009

Panel Chair, *ACM/IEEE International Symposium Low Power Electronics and Design (ISLPED '09)*, San Francisco, California, August 2009

Session Chair, *"Non Volatile Memory" at the High-K Dielectric Materials and Gate Stack Symposium, Electrochemical Society Meeting (ECS '09),* Vienna, Austria, October 2009

Session Chair, *"MOS Devices" at the IEEE Device Research Conference (DRC '09), June 2009*

Session Chair, *"MOS Devices" at the IEEE Device Research Conference (DRC '09), June 2009*

Session Co-Chair, "III-V Logic Transistors with Advanced Gate Stack" at the *IEEE International Electron Devices Meeting (IEDM '09)*, Baltimore, Maryland, December 8, 2009

Session Co-Chair, *"Heterostructure High-Speed Devices"* at the *IEEE International Electron Devices Meeting (IEDM '08),* San Francisco, California, December 2008

Session Chair, *"Materials for Ge and Si devices"* at the *International Conference on Insulating Films on Semiconductors (INFOS '07)*, Athens, Greece, June 2007

NSF Review Panelist- In EPDT, EMT programs in years 2008-2010

Reviewer,

IEEE Transactions on Nanotechnology

IEEE Transactions on Electron Devices

IEEE Electron Device Letters

ACM Journal on Emerging Technologies in Computing Systems

Solid-State Electronics

Applied Physics Letters

Journal of Applied Physics (JAP)

Journal of Vacuum Science and Technology B

Journal of Nanotechnology

Nanotechnology (Journal) from Institute of Physics (IOP)

Journal of Electronic Materials

IEDM, DRC, ESSDERC, VLSI-TSA, ISLPED SISC, EMC, SNW

Doctoral Thesis Committee Membership,

Completed

* Dissertation Committee Member: Niranjan Soundarajan, June 2010, Advisor: V. Narayanan
* Dissertation Committee Member: Soumya Eachempati, June 2010, Advisor: V. Narayanan
* Dissertation Committee Member: Jason Ryan, May 2010, Advisor: P. Lenahan
* Dissertation Committee Member: Nicholas Duarte, July 2009, Advisor: S. Tadigadapa
* Dissertation Committee Member: Insoo Kim, July 2009, Advisor: T. Jackson
* Dissertation Committee Member: Karthik Sarpatwari, June 2009, Advisor: S. Mohney
* Dissertation Committee Member: Sandhya C., February 2010, Indian Institute of Technology, Mumbai, Advisor: S. Mahapatra
* Dissertation Committee Member: Aaron Vallett, Februaray 2011, Advisor: T. Mayer
* Dissertation Committee Member: Prasoon Joshi, December 2010, Advisor: S. Tadigadapa

In Progress

* Dissertation Committee Member: Meng-Wei Kuo, Advisor: T. Mayer

* Dissertation Committee Member: Xiahua Zhong, Advisor: T. Mayer

* Dissertation Committee Member: Jing Liang, Advisor: N. Samarth

* Dissertation Committee Member: Joon Sue Lee, Advisor: N. Samarth

* Dissertation Committee Member: Xin Wang, Advisor: T. Mayer

* Dissertation Committee Member: James Bashan, Advisor: C. Grimes

* Dissertation Committee Member: Xiangyu Dong, Advisor: Y. Xie

* Dissertation Committee Member: Dalong Zhao, Advisor: T. Jackson

* Dissertation Committee Member: Brad Bittel, Advisor: P. Lenahan

Teaching

Student Rating of Teaching Effective Scores for "Overall Quality of Instructor" (out of maximum score of 7) are noted next to the semester the course was taught along with the college of engineering (COE) average

Penn State, EE 597B: Nano Transistors

Semester Taught: Spring 2010 (6.64; COE Avg. ?)

Enrollment: 10

Description: Advanced Graduate level course on ballistic and collision affected quantum transport in nanoscale devices; Developed by Prof. Datta

Penn State, EE 542: Semiconductor Devices

Semester Taught: Fall 2009 (6.45; COE Avg. ?), Fall 2007 (5.50; COE Avg. ?)

Enrollment: 22, 21

Description: Graduate level core course on solid-sate device physics

Penn State, EE 442: Solid-State Devices

Semester Taught: Fall 2008 (6.53; COE Avg. ?)

Enrollment: 17

Description: Senior elective course on solid-state materials, device physics and electronic/photonics devices

Penn State, EE 310: Electronic Circuit Design

Semester Taught: Spring 2009 (6.65; COE Avg. ?), Spring 2008 (6.37; COE Avg. ?)

Enrollment: 113, 125

Description: Junior Level core electronic circuits course emphasizing analog amplifiers and digital logic

University Service

Department Chair Search Committee, EE Department (09/2010-Present)

Graduate Program Committee, EE Department (05/2009-Present)

Undergraduate Program Committee, EE Department (09/2007-05/2009)

Electronic Materials and Devices Area Committee, EE Department (08/2007-Present)

Electronic Materials and Devices Area Coordinator for the Doctoral Candidacy Exam, EE Department (08/2007 – Present)

Complex Oxide Faculty Search Committee, Materials Science and Engineering Department, (08/2008 – 04/2009)