

The Pennsylvania State University
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**BAND-TO-BAND TUNNELING FIELD EFFECT TRANSISTOR FOR LOW POWER
LOGIC AND MEMORY APPLICATIONS: DESIGN, FABRICATION AND
CHARACTERIZATION**

A Dissertation in
Electrical Engineering
by
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ABSTRACT

Over the past decade the microprocessor clock frequency has hit a plateau. The main reason for this has been the inability to follow constant electric field scaling, which requires the transistor supply voltage to be scaled down as the transistor dimensions are reduced. Scaling the supply voltage down reduces the dynamic power quadratically but increases the static leakage power exponentially due to non-scalability of threshold voltage of the transistor, which is required to maintain the same ON state performance. This limitation in supply voltage scaling is directly related to MOSFET's (Metal Oxide Semiconductor Field Effect Transistor) sub-threshold slope (SS) limitation of 60 mV/dec at room temperature. Thus novel device design/materials are required that would allow the transistor to switch with sub-threshold slopes steeper than 60 mV/dec at room temperature, thus facilitating supply voltage scaling.

Recently, a new class of devices known as super-steep slope ($SS < 60$ mV/dec) transistors are under intense research for its potential to replace the ubiquitous MOSFET. The focus of this dissertation is on the design, fabrication and characterization of band-to-band tunneling field effect transistor (TFET) which belongs to the family of steep slope transistors. TFET with a gate modulated zener tunnel junction at the source allows sub- kT/q (sub-60 mV/dec at room temperature) sub-threshold slope (SS) device operation over a certain gate bias range near the off-state. This allows TFET to achieve much higher $I_{ON}-I_{OFF}$ ratio over a specified gate voltage swing compared to MOSFETs, thus enabling aggressive supply voltage scaling for low power logic operation without impacting its ON-OFF current ratio.

This dissertation presents the operating principle of TFET, the material selection strategy and device design for TFET fabrication. This is followed by a novel 6T SRAM design which circumvents the issue of unidirectional conduction in TFET. The switching behavior of TFET is studied through mixed-mode numerical simulations. The significance of correct benchmarking

methodology to estimate the effective drive current and capacitance in TFET is highlighted and compared with MOSFET. This is followed by the fabrication details of homo-junction TFET. Analysis of the electrical characteristics of homo-junction TFET gives key insight into its device operation and identifies the critical factors that impact its performance. In order to boost the ON current, the design and fabrication of hetero-junction TFET is also presented.

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Chapter 1

Introduction

1.1 Power crisis in today's multi-core CPU era

Since the invention of transistor at Bell labs [1] and the Integrated circuit by Jack kilby at TI [2], the semiconductor industry has seen a record growth over the last forty years in terms of revenue and transistor count on a chip with the trend following the well known Moore's law [3]. But, the miniaturization of the transistor and its ever growing density on the chip has paved the way for the seemingly insurmountable barriers of static power dissipation (Gate Leakage, Drain-Substrate Tunneling Leakage), heat removal resulting from high dynamic power dissipation, parasitic resistances and global interconnect delays. It has been suggested that there are certain fundamental impenetrable limits to the scaling of Si nano-electronics [4, 5].

Over the last decade, the transistor architecture has undergone significant changes compared to its primitive cousin [6] with the introduction of strained silicon at 90nm node [7] and HfO₂ gate dielectric (replacing SiO₂) with a metal gate (replacing poly-silicon) at the 45nm node [8] (figure 1-1). Strain in the Si MOSFET channel results in higher carrier mobility, thus significantly boosting its ON state performance while HfO₂ with a higher dielectric constant ($\epsilon \sim 25$ compared to 3.9 for SiO₂) and gate dielectric thickness has allowed stronger gate coupling with the channel and an exponentially reduced gate tunneling leakage. The use of metal gate electrode has increased the channel mobile charge concentration by eliminating the poly-silicon depletion, thereby resulting in higher drive current.

In modern multi-core CPU's the total power dissipation is limited to around 100W due to thermal issues. But, more transistors are required with each generation of scaled technology

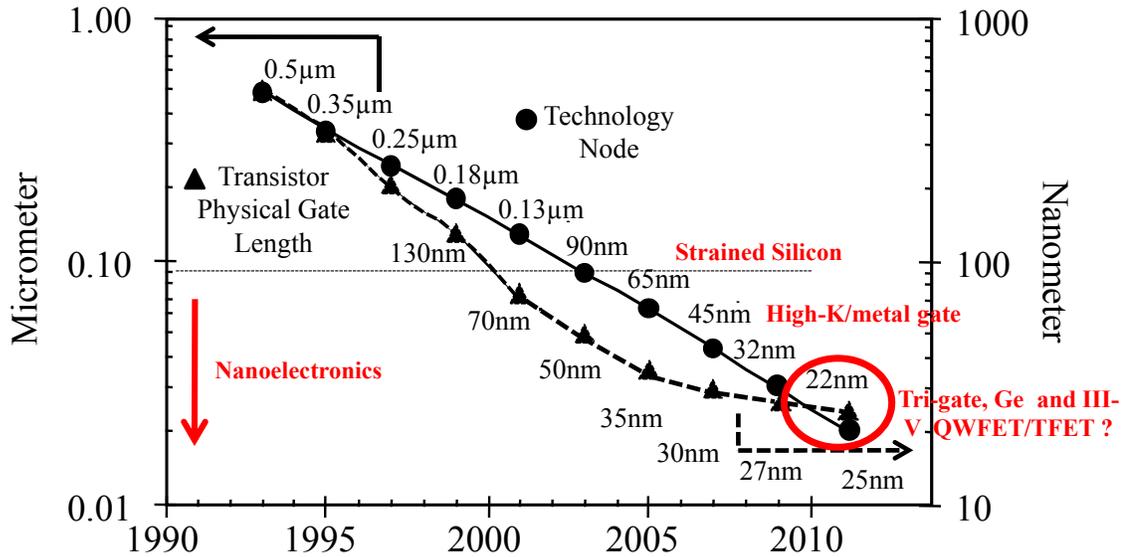


Figure 1-1. Transistor scaling over the years has followed the well known Moore's law resulting in 2X increase in transistor count every two years. With each generation of scaled technology the transistor performance has been improved. But, it's only in the last decade or so that some notable changes have been made to the traditional transistor architecture, like strained Si at 90nm node and High-K/metal gate at 45nm node. Beyond the 22nm node Tri-gate/Multi-gate devices, Ge and III-V MOSFETs/QW-FETs, TFETs and a host of other novel devices are being explored.

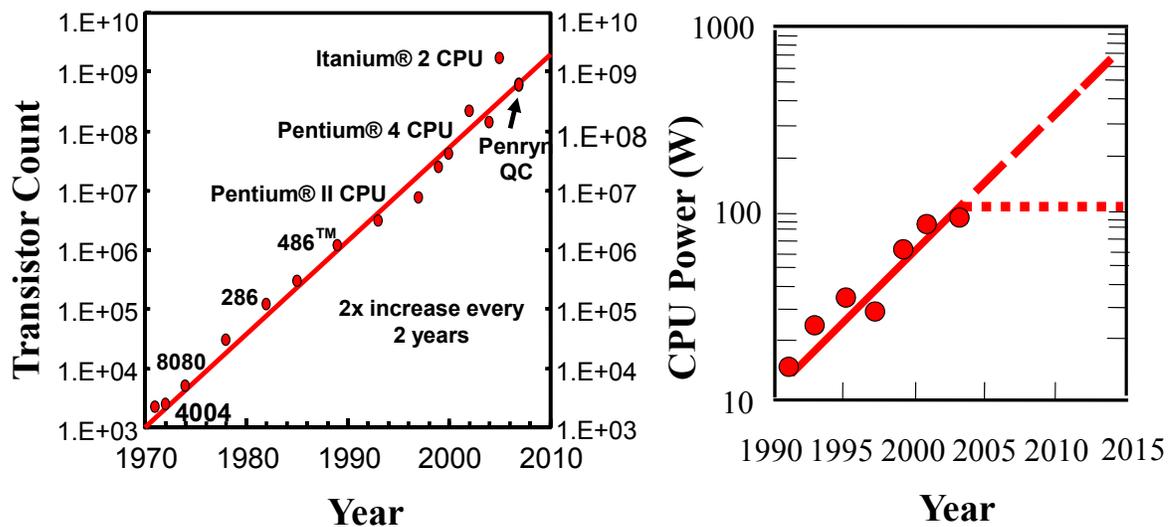


Figure 1-2. (a) Rising transistor count in Intel microprocessor chips (b) The total power dissipation in modern CPU is limited to around 100W [9].

to meet the ever increasing demand for higher functionality (figure 1-2). For the 22 nm node and beyond a host of new devices/materials are being investigated, trying to address this most critical bottleneck to transistor scaling i.e. power dissipation, both static and dynamic.

Some of the alternatives being actively pursued for future technology nodes are the Tri/Multi-Gate device architectures [10], alternate channel materials with multi-gate FETs (III-V and strained Ge quantum wells and FETs) [11], super-steep sub-threshold slope transistors (sub-60mV/dec) [12] [13] [14] [15], carbon-nanotube/graphene based FETs [16] and spin FETs [17]. All of these approaches promise low-power operation.

This dissertation will primarily focus on inter-band tunnel field effect transistor (TFET) [12] which falls in the category of super-steep sub-threshold slope transistors. As will be discussed in the next section unlike metal oxide semiconductor field effect transistors (MOSFET), TFETs can in principle operate at sub-threshold slopes of less than 60 mV/dec at room temperature. This results in higher I_{ON} - I_{OFF} ratio at reduced supply voltages thus enabling aggressive supply voltage scaling. Further due to the presence of the source side tunnel barrier the off current, I_{OFF} can be significantly smaller compared to MOSFET and is limited only by the reverse biased diode leakage current. This can significantly reduce the dynamic (proportional to square of the supply voltage) and static power dissipation in TFET (proportional to supply voltage and off current, I_{OFF}). Due to this unique feature of TFET, Semiconductor Research Corporation's (SRC) National Research Initiative (NRI) has recently created a focus center called the Midwest Institute for Nano-electronics Discovery (MIND) to further understand and fabricate these tunnel devices as part of a bigger charter to develop energy-efficient devices for future high performance and low power computing systems.

At this point it also worth pointing out that there are some other proposals for achieving sub-threshold slopes of less than 60 mV/dec like the impact ionization MOSFET (IMOS) [13],

use of negative capacitance effect with ferroelectric gate dielectrics [14] and suspended gate MOSFET [15] with a cantilever type action but this work will primarily concentrate on TFETs.

1.2 Band-to-Band Tunneling Field Effect Transistor (TFET): Operating Principle

In order to understand the operating principle of TFET it is useful to compare it with MOSFET. Figure 1-3 shows the device structure for MOSFET and TFET. Double gate (DG) structures with a gate length (L_G) of 30 nm, 2.5 nm thick HfO_2 gate dielectric and a thin body thickness of 7 nm shown here are for illustrative purposes only and the physics discussed in this section is fairly general and independent of any particular device architecture.

As shown in figure 1-3 TFET consists of $P^+ - I - N^+$ doped regions as source, channel and drain respectively compared to $N^+ - P - N^+$ doped regions in MOSFETs. Fig. 1-4 depicts the energy band diagram for MOSFET and TFET. In the OFF state ($V_{GS}=0V$, $V_{DS}=1V$), the conduction in MOSFET is limited by the source side p-n junction barrier which prevents the thermionic emission of carriers while in the ON state ($V_{GS}=V_{DS}=1V$) the source barrier is negligible enabling thermionic emission of carriers. For TFETs in OFF state ($V_{GS}=0V$, $V_{DS}=1V$), the transmission probability is low due to the wide source to channel tunnel junction barrier (Low Electric Field) resulting in very low OFF currents. In the ON state ($V_{GS}=V_{DS}=1V$) the tunnel barrier shrinks allowing carriers to tunnel through into the channel.

Figure 1-5 compares the simulated transfer ($I_{DS}-V_{GS}$) characteristics for Si MOSFET and TFET as an illustrative case. Si TFET has a much steeper sub-threshold slope ($SS < 60$ mV/dec) while its ON current, I_{ON} is an order of magnitude lower than Si MOSFET due to the presence of the source side tunnel barrier.

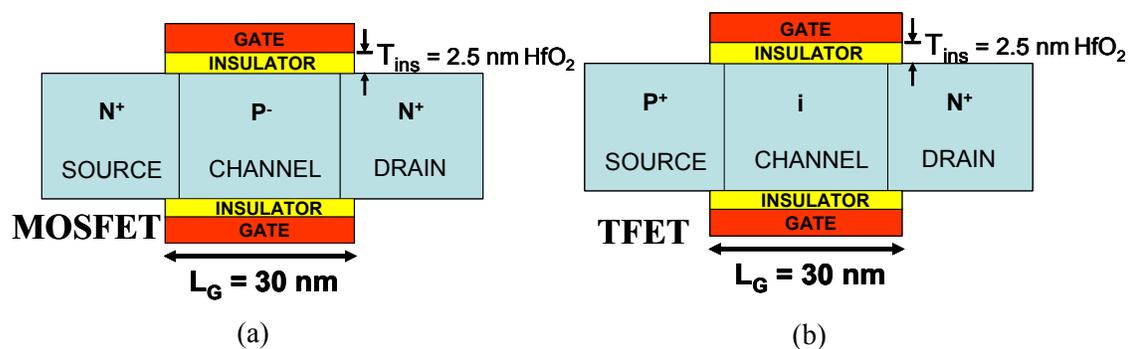


Figure 1-3. Generic device schematic (a) MOSFET (b) TFET

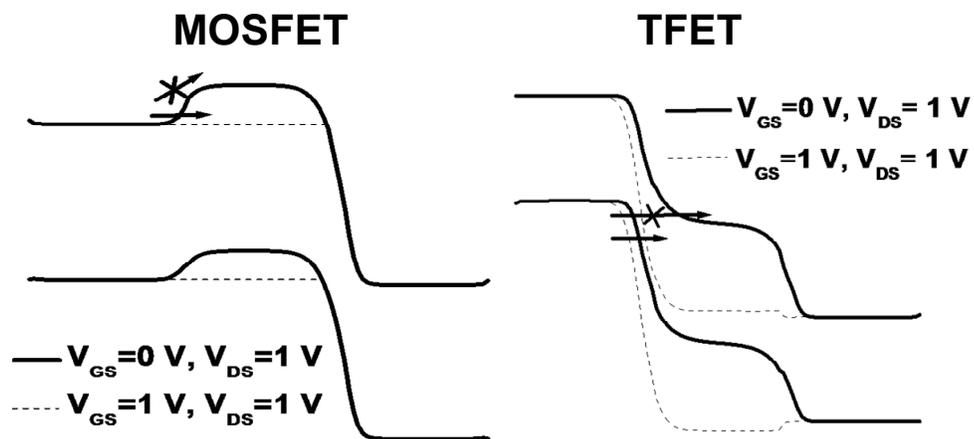


Figure 1-4. Band-diagrams for MOSFET and TFET illustrating its operating principle

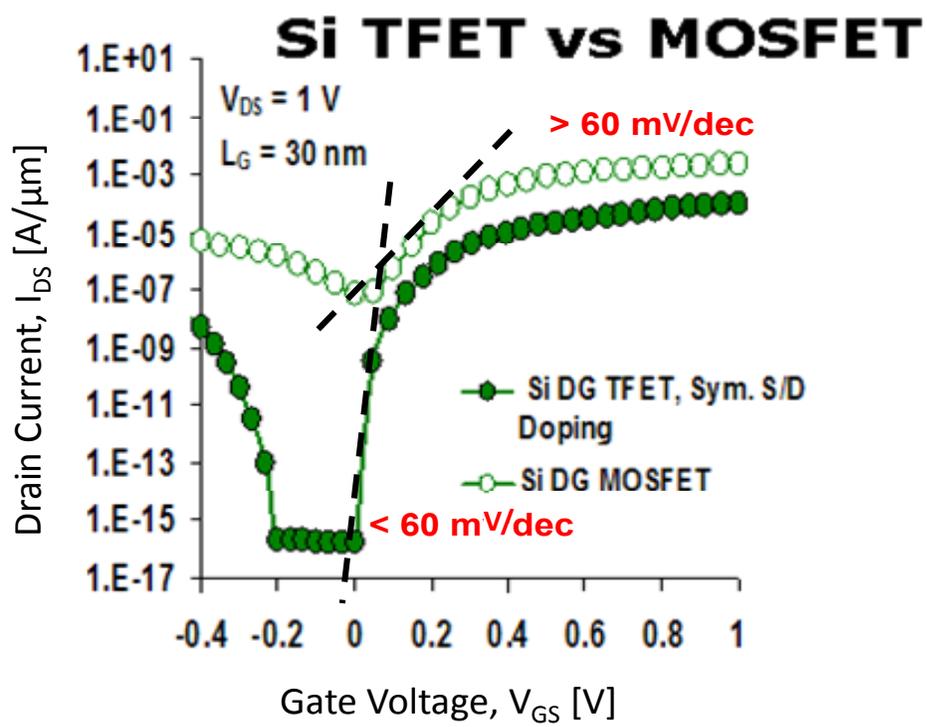


Figure 1-5. Simulated transfer characteristics of Si MOSFET vs. TFET

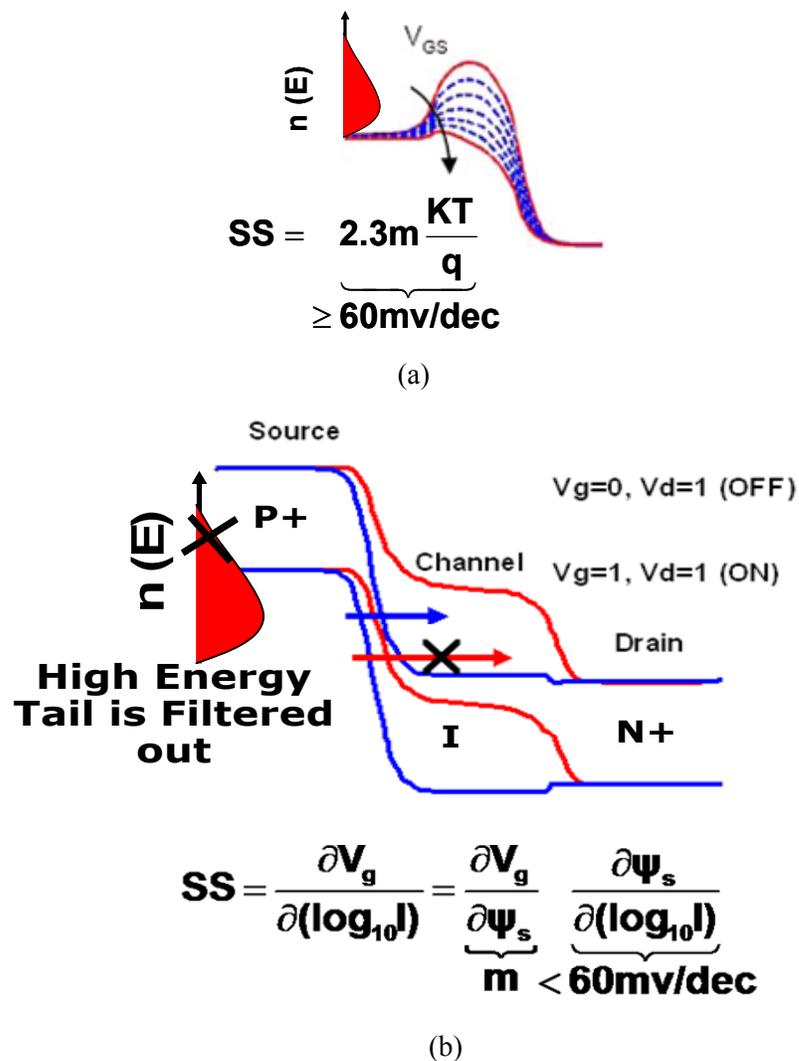


Figure 1-6. (a) Fermi distribution of carriers in the source of a MOSFET. The electrons in the high energy tail of the distribution participate in the transport process resulting in the sub-threshold slope limitation of 60mV/dec (b) Fermi distribution of carriers in the source of a TFET. The electrons in the high energy tail of the distribution are cut-off by the band-gap in the source and thus do not participate in the transport process. It is primarily the cold carriers that participate in the transport process resulting in a sub-threshold slope of less than 60mV/dec. This is similar to a band-pass filter action wherein the high energy carriers are filtered out.

In MOSFETs (Figure 1-6 (a)) the SS is limited by the tail of the Fermi-Dirac distribution of electrons in the N+ source region resulting in $SS=2.3mkT/q$ [18], where $m=1+C_{dep}/C_{ox}$, k is the Boltzmann constant, T is the temperature, C_{dep} – is the semiconductor depletion capacitance and C_{ox} is the oxide capacitance. On the contrary in TFETs (Figure 1-6 (b)) the Fermi tail is cut-off by the band-gap in the source region. Qualitatively this can be understood as cold carriers i.e. carriers participating in the tunneling process are cold (lower T) and hence the SS of less than 60 mV/dec.

The drain current in TFET under high gate and drain bias can be expressed as shown in equation (1), which is similar to the conventional tunnel diode equation [19]. This is possible because the channel quasi-fermi level is in equilibrium with the drain fermi level at high gate and drain bias. In equation (1), $T(E)$ is the tunneling probability, $F_S(E)$ and $F_D(E)$ are the source and drain side Fermi-Dirac distributions and N_S and N_D are the corresponding density of States. The integral range from E_C (Channel) to E_V (Source) represent the range of energies over which tunneling takes place. The WKB expression for tunneling probability (Triangular Barrier Approximation) is shown in Equation (2), E_g represents the barrier height seen by the particle

$$I_T=I_{VC} - I_{CV} = A \int_{E_C}^{E_V} [F_S(E) - F_D(E)]T(E)N_S N_D dE \quad (1)$$

$$T(E) = \exp\left(-\frac{4\sqrt{2m^*}E_g^{3/2}}{3q\hbar\xi}\right) \quad (2)$$

impinging on the tunnel barrier (Band-gap of the material in this case), m^* is the effective mass of the tunneling particle (material dependent) and ξ is the electric field at the tunnel junction. This implies that lower band-gap, low mass materials (Low E_g and m^*) and higher electric fields will result in higher ON currents.

1.3 Brief history

Over the years many attempts have been made to replace the conventional transistor, both the bipolar junction transistor (BJT) and the MOSFET. This section will briefly review all the tunneling transistor based concepts that have been proposed till date.

The first unequivocal demonstration of a true tunneling device was the tunnel diode by L. Esaki [19][20][21]. While studying the internal field emission in a degenerately doped germanium tunnel diode (heavily doped p^+/n^+ junction) he discovered an anomalous current-voltage characteristic (negative resistance region) in the forward biased operation. This was explained using the concept of quantum mechanical tunneling. The operating principle of a tunnel diode is shown in the figure 1-7 (a) below. This device has been widely used for low-power microwave applications such as local oscillators for satellite communication and high speed sampling. A tunnel diode operating in the reverse bias region is known as the zener/backward diode. The operating principle of the zener diode is illustrated in figure 1-7 (b). This phenomenon of zener tunneling is exploited in the TFET discussed in the previous section, which is essentially a gated zener diode.

After this initial work by L. Esaki in heavily doped semiconductor junctions, tunneling phenomenon was shown to play a crucial role even in metal–oxide–metal (MOM) and metal–oxide–semiconductor (MOS) diodes [19]. This concept was utilized in the first proposal for a tunnel transistor by Mead in 1960 [22]. The operating principle is shown in figure 1-8(a). The device is sometimes called the MOMOM (metal-oxide-metal-oxide-metal) transistor. In this case the electrons are injected from the emitter into the base via tunneling. These electrons that enter the base have energies of a few kT above the fermi level of the base metal. This is thus also called a hot electron transistor. The goal was to boost the current gain of the transistor by reducing the

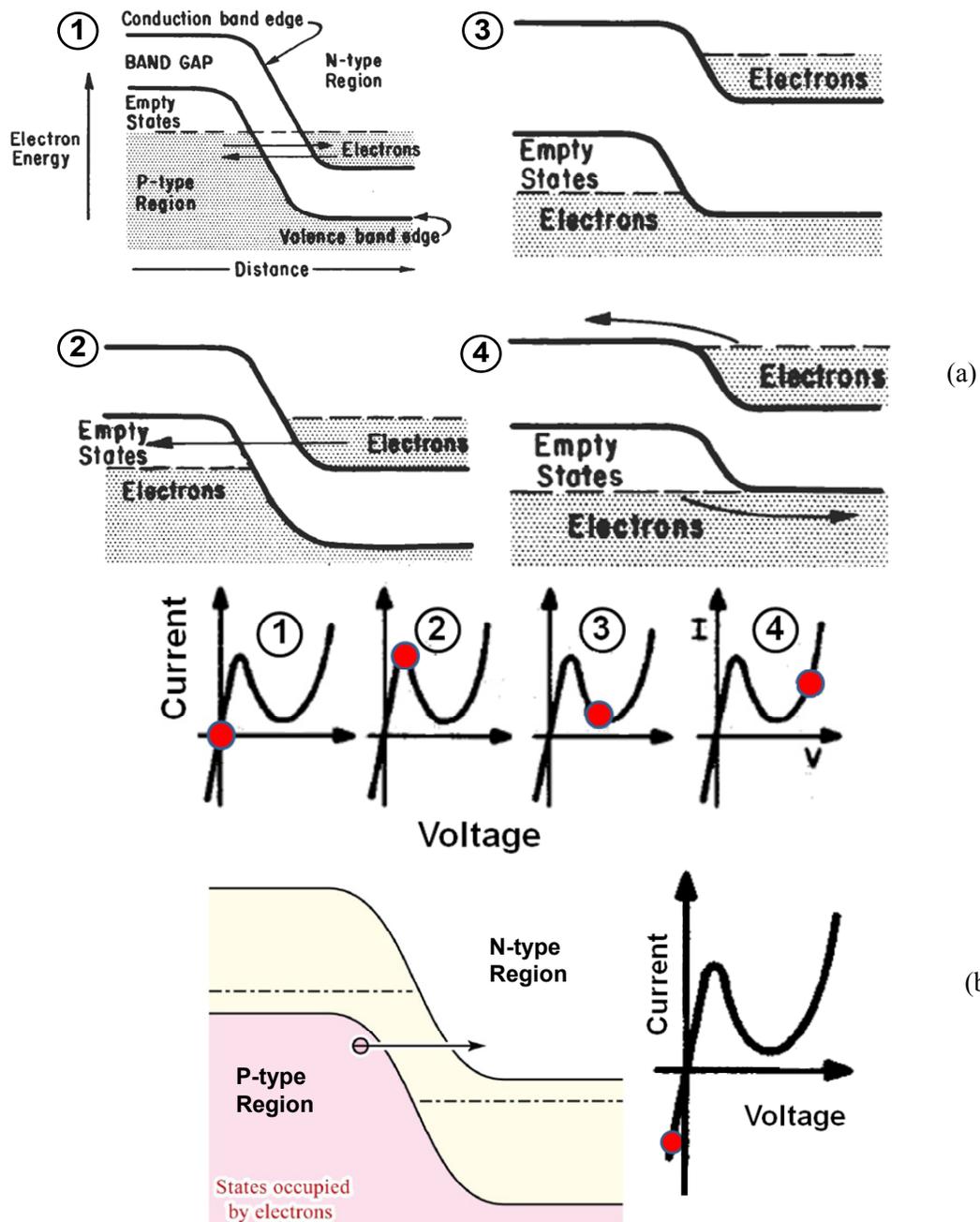


Figure 1-7. (a) Operating principle of a tunnel diode under forward bias (1) Electrons at the same energy level on both sides of the junction. There is no net current (2) Electrons tunnel from the n-type region to the p-type region. A large current flows through the device (3) There are no states available for the electrons on the n-side to tunnel into, the current drops to a very small value (4) The electrons are thermionically emitted over the barrier, current increases again (b) Operating principle of a backward/zener diode. In this case electrons tunnel from the p-type region to the n-type region under reverse bias. This phenomenon is exploited in TFET [19][20][21]

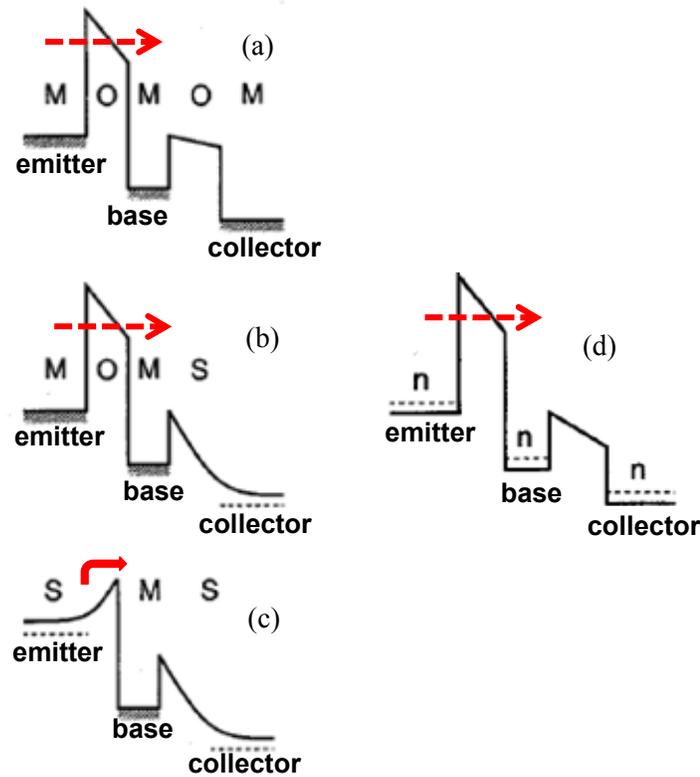


Figure 1-8. Band diagram for different types of hot electron transistor.(a), (b) and (c) are metal base transistors (MBT) while (d) is Heiblum's [24] all semiconductor analog of the MBT. All of these utilize hot electron injection into the base as a means to reduce the base transit time. In (a), (b) and (d) hot electrons are injected via quantum-mechanical tunneling while in (c) it is thermionically emitted over the barrier. M-metal, O-oxide and n refers to n-type semiconductor doping [23]

base transit time. Two other deviations of this device were also proposed. In one case the second MOM layer was replaced with a metal-semiconductor (MS) schottky contact (figure 1-8(b)) and in another a SMS layer (figure 1-8(c)) was used to thermionically (instead of tunneling) inject hot electrons into the metal base. Unfortunately, all these devices showed very poor transfer ratio (α), mainly due to the quantum-mechanical (QM) reflection of electrons at the base-collector interface [23].

Taking advantage of the tremendous progress in MBE (molecular beam epitaxy) growth of semiconductor hetero-junctions, in 1981 Heiblum [24] proposed the first all semiconductor analog of the metal base transistor (MBT). In this case the QM reflections can be largely avoided if the transport occurs at similar brillouin-zone points on both sides of the interface [23]. Unfortunately, the speed limitations of all these proposals involving hot carrier injection via tunneling were very similar to that of the hetero-junction bipolar transistor (HBT) - already a mature technology at that time. We will discuss more on hot carrier injection as a means to boost drive current in TFET in chapter 5.

Recently, there has been a lot of interest in using gated zener diode (TFET) as a digital switch. The operating principle of TFET is already explained in section 1.2, here we will review some of the early work in this area. S. Banerjee [25] in 1987 first reported of a novel three terminal transistor action in a silicon trench capacitor that worked on the principle of zener tunneling. In 1992 T. Baba [26] formally proposed the concept of a surface tunnel transistor (STT) using a gated P^+-I-N^+ diode. Transistor action was demonstrated in GaAs based STTs with $i-Al_{0.6}Ga_{0.4}As$ as the gate dielectric. In 1995 W. M. Reddick [27] experimentally demonstrated STT action in silicon. In 2000, W. Hansch [28] proposed and fabricated a vertical silicon tunnel transistor taking advantage of MBE grown epitaxial layers to create highly abrupt tunnel junctions. This was followed by the work of K. K. Bhuiwala [29] who proposed the use of δp^+ doped SiGe layer next to the source-channel tunnel junction in a vertical device architecture to

improve its drive current and sub-threshold slope. In 2004, J. Appenzeller [30] experimentally demonstrated sub- kT/q sub-threshold slope in a carbon-nanotube based transistor, clearly explaining the band-pass filter like action between the conduction and valence band that gives rise to sub- kT/q sub-threshold slope. This was then followed by other experimental demonstration in Si, strained SiGe and Ge material systems [31][32][33].

Besides, some initial proof of concept work by T. Baba [26] not much work has been done till date using III-V compound semiconductors. III-V compound semiconductors allow band-gap engineering and are ideally suited for TFET application, as will be discussed in greater detail in the following chapters. This dissertation primarily deals with the use of III-V compound semiconductors for TFET application.

1.4 Organization of dissertation

Chapter 2 discusses the material selection strategy, device design and TFET based memory circuits. In particular, we will look at a novel 6T (six transistor) TFET SRAM design to circumvent the unidirectional conduction issue in TFET. Chapter 3 investigates the large signal switching behavior of TFET and compares its performance with MOSFET. TFET has an inherent miller capacitance and its effect on digital switching is discussed at length. Chapter 4 describes the fabrication and characterization of homo-junction and hetero-junction TFET. Chapter 5 presents the conclusion and future work.

Chapter 2

TFET Device Design and Memory Circuits: A Simulation Study

This chapter is organized into five different sections. Section 2.1 presents the material selection strategy for TFET fabrication. A thorough numerical simulation study is presented to identify the appropriate material system for high performance logic application. The physics of non-local tunneling model used for numerical simulation is explained in detail. Section 2.2 discusses the selection of the best device architecture (vertical vs. lateral) for TFET fabrication. This is followed by the design of the ultimate scaled transistor architecture. Section 2.3 describes the unidirectional conduction property of TFET. Section 2.4 discusses the implication of this unidirectional conduction on conventional 6T TFET SRAM design. A novel 6T TFET SRAM design is proposed in section 2.5.

2.1 Material selection strategy: A simulation study

This section discusses the results from a study on double gate (DG) inter-band tunnel FETs (TFET) in 3 different material systems [34], Si, Ge and InAs, for logic circuit applications down to 0.25V supply voltage (V_{DD}). Based on two-dimensional numerical drift-diffusion simulations [35], it is shown that 30nm gate length (L_G) InAs (indium arsenide) based TFETs can achieve I_{ON}/I_{OFF} (ON-OFF current) ratio of $> 4 \times 10^4$ with < 1 ps (pico-second) intrinsic delay at 0.25V V_{DD} . Further it is shown that in the range of 0.5-0.75V $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ is the most promising material system for TFET application.

2.1.1 Device simulation set-up

Before we discuss the results of numerical simulation it is important to understand the various models and framework used for simulation. This is explained schematically in figure 2-1.

The device structure and physical models are fed into the device simulator. The poisson and carrier continuity equation is then solved self-consistently to yield the transfer and output characteristics of the device. Fermi statistics, caughy-thomas velocity saturation model [36], masetti mobility model [37], non-local tunneling model [35][38] and Shockley-Read-Hall (SRH) generation-recombination model [39] are used for numerical simulation. The non-local tunneling model needs a little more discussion. This model is explained below.

In the non-local tunneling model the tunneling probability is calculated using the Wentzel-Kramers-Brillouin (WKB) approximation [40] which is essentially an exponential relationship involving the imaginary wave-vector, κ in the band-gap of the semiconductor (equation 1).

$$\Gamma_{VC} = \exp\left(-2 \int_u^l \kappa(r, \varepsilon) dr\right) \quad (1)$$

$$\kappa(r, \varepsilon) = \frac{\kappa_C \kappa_V}{\sqrt{\kappa_C^2 + \kappa_V^2}} \quad (2)$$

$$\kappa_C = \sqrt{2m_C(r) |E_C(r) - \varepsilon| \Theta[E_C(r) - \varepsilon] / \hbar} \quad (3)$$

$$\kappa_V = \sqrt{2m_V(r) |\varepsilon - E_V(r)| \Theta[\varepsilon - E_V(r)] / \hbar} \quad (4)$$

$$R_{VC}(u, l, \varepsilon) = A_{VC} F T_{VC} T \ln \left[\frac{1 + \exp\left(\frac{\varepsilon - E_{f,p}(u)}{kT}\right)}{1 + \exp\left(\frac{\varepsilon - E_{f,n}(l)}{kT}\right)} \right] \quad (5)$$

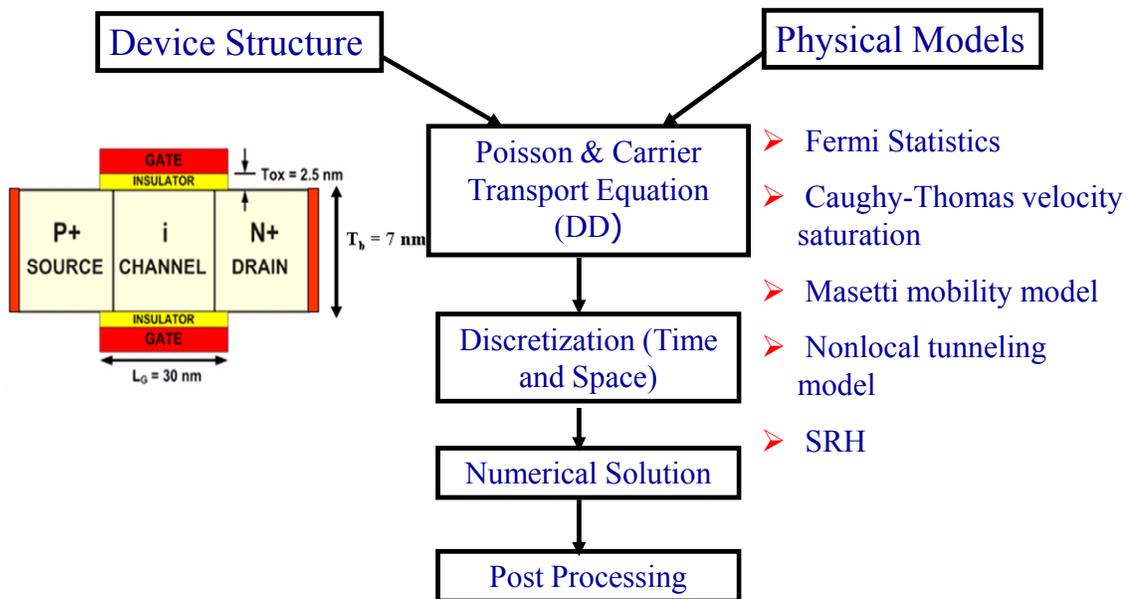


Figure 2-1. Numerical simulation set-up.

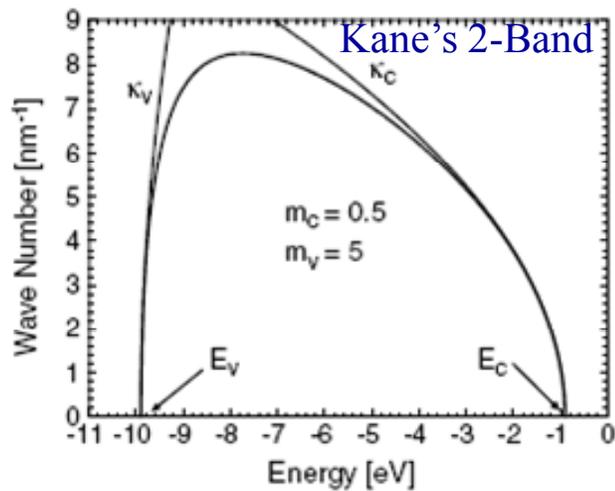


Figure 2-2. Kane's 2-band dispersion relation smoothly connects the band-edge (κ_C and κ_V) wave-vector within the band-gap of the semiconductor.

The imaginary wave-vector, κ is calculated using the Kane's 2-band dispersion relation [41] (equation 2) as shown in figure 2-2. κ_C and κ_V are the band-edge wave vectors in the conduction and valence band respectively. Kane's 2-band dispersion relation smoothly connects the band edge wave vectors along the band-gap. This then forms a part of the generation-recombination term in the carrier-continuity equation (equation 5). A derivation for R_{VC} is shown below.

$$\begin{aligned}
 R_{VC} &= \frac{1}{q} \nabla \cdot J_{Tun} \\
 &= \frac{1}{q} \frac{dJ_{Tun}}{d\psi} \cdot \nabla \psi \\
 &= \frac{dJ_{Tun}}{d\varepsilon} \cdot F
 \end{aligned} \tag{6}$$

Here ψ , $\varepsilon = -q\psi$ and $F = -\nabla \psi$ are the potential, energy level and electric field, respectively.

The total tunnel current can be expressed as shown in (7).

$$J_{Tun} = J_{Tun,p-n} - J_{Tun,n-p} \tag{7}$$

$$J_{Tun,p-n} = A^* T^2 \int_{\varepsilon}^{\infty} T_{VC} \ln \left[\frac{1}{1 + \exp((\varepsilon - E_{fp}) / k_B T)} \right] d\varepsilon \tag{8}$$

$$J_{Tun,n-p} = A^* T^2 \int_{\varepsilon}^{\infty} T_{VC} \ln \left[\frac{1}{1 + \exp((\varepsilon - E_{fn}) / k_B T)} \right] d\varepsilon \tag{9}$$

Here E_{fp} and E_{fn} are the quasi-fermi levels on the left and right side of the tunnel barrier.

After some simple algebraic manipulation equation (1) can be written as;

$$R_{VC} = A_{VC} F T_{VC} T \ln \left[\frac{1 + \exp[(\varepsilon - E_{fp}) / kT]}{1 + \exp[(\varepsilon - E_{fn}) / kT]} \right] \tag{10}$$

The inter-band tunneling current in TFET depends on the potential profile along the entire path between two points connected by tunneling. In contrast to the local tunneling models commonly used [42][43] the non-local tunneling model reflects the real space carrier transport through the barrier taking into account the potential profile along the entire tunneling path.

2.1.2 Simulation result

The n-channel DG TFET and MOSFET used in this study have the same design as in figure 1-3. Gaussian doping profiles with doping gradients of 2nm/decade are used for the source and drain regions. Despite the steep sub-threshold slope and the I_{ON} - I_{OFF} (ON-OFF current) ratio spanning 12 decades over 1V V_{GS} swing (Figure 1-5), Si DG TFET I_{ON} (60 $\mu\text{A}/\mu\text{m}$) is much less than Si DG MOSFET I_{ON} (1.1 $\text{mA}/\mu\text{m}$) due to the poor tunneling rate of source side valence electrons into the channel conduction band. Narrow gap semiconductors can enhance the source side tunneling rate due to the combined effects of both reduced barrier height and shorter tunneling distance in addition to the reduced tunneling mass. Figure 2-3 compares the I_{DS} - V_{GS} characteristics of Ge and InAs based DG TFET with its MOSFET counterparts. Both Ge and InAs DG MOSFET suffer from increased band to band tunneling at the drain end, which forward biases the source to channel junction and significantly degrades the I_{ON} - I_{OFF} ratio. It's clearly seen that the performance difference between the TFET and the MOSFET is reduced with reducing band-gap and supply voltage of operation. In order to suppress the ambipolar characteristics, an asymmetric source and drain doping in InAs DG TFET was utilized which exhibits I_{ON} - I_{OFF} ratio of $>4 \times 10^4$ at 0.25V V_{DD} .

We further analyzed the output characteristics of TFET in great detail. With increasing drain bias in TFETs, the majority of the potential drop occurs in the p+/n+ junction (Figure 1-4)

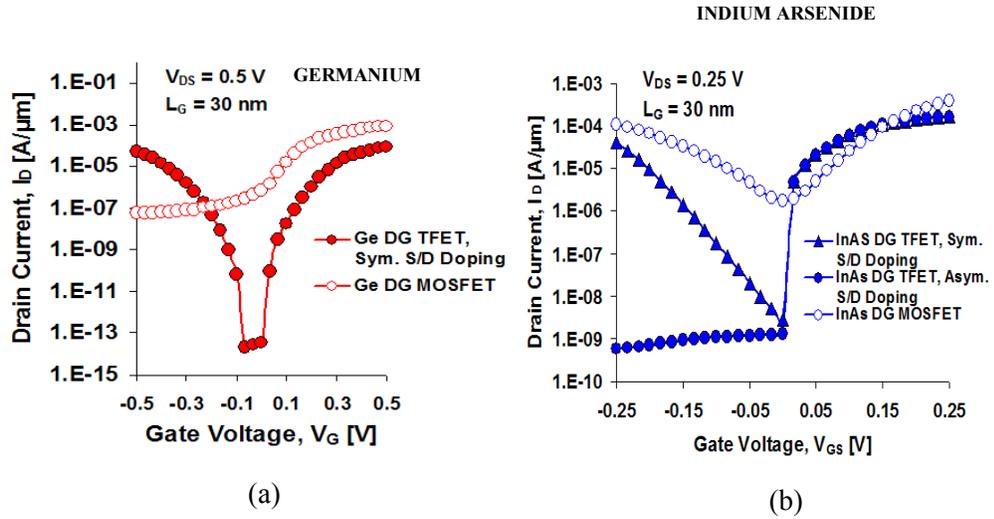


Figure 2-3. (a) I_{DS} - V_{GS} (transfer characteristics) comparison of Ge DG TFET with Ge DG MOSFET (b) I_{DS} - V_{GS} (transfer characteristics) comparison of InAs TFET v/s InAs DG MOSFET

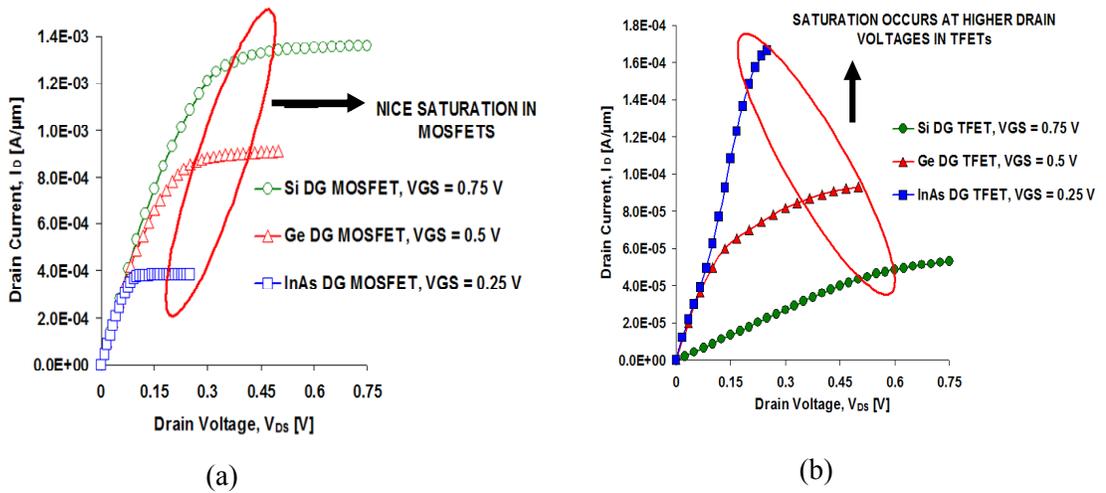


Figure 2-4. (a) I_{DS} - V_{DS} (output characteristics) of MOSFET in three different material systems (b) I_{DS} - V_{DS} (output characteristics) comparison of TFET in three different material systems

near the source end which causes delayed saturation and pinch-off characteristics in TFET compared to its MOSFET counterparts (Figure 2-4).

We further compared the effect of scaling the electrical gate dielectric thickness (SiO_2 vs. HfO_2) on the performance of Si, Ge and InAs based TFET (Figure 2-5). While Si and Ge TFETs show significant percentage increase in drive current with oxide scaling, the InAs TFETs show negligible sensitivity due to the small tunneling barrier and the limited density of states in the channel originating from its low effective mass. This also results in reduced sensitivity of InAs TFETs to supply voltage (and, hence, electric field) scaling for a fixed $I_{\text{ON}}-I_{\text{OFF}}$ ratio of 10^4 (Figure 2-5).

Finally, we compared the device performance of Si, Ge and InAs based TFET for a fixed $I_{\text{ON}}-I_{\text{OFF}}$ ratio of 10^4 using a benchmarking approach presented in [44]. The InAs and Ge based TFET show clear advantage in switching delay, τ (Figure 2-6 (a)), as well as in the energy-delay product, EDP (Figure 2-6 (b)), at fixed $I_{\text{ON}}-I_{\text{OFF}}$ ratio 10^4 , as V_{DD} is progressively scaled. InAs TFETs show the maximum benefit when the supply voltage V_{DD} is scaled aggressively down to 0.25V and this benefit primarily arises from efficient tunneling under low electric field and MOSFETs in this low V_{DD} range do not even meet the $I_{\text{ON}}-I_{\text{OFF}}$ stipulation. Thus, narrow band-gap semiconductor based DG TFETs provide a promising device option for ultra-low standby and dynamic power high-speed logic circuits operating under quarter volt supply voltages. Even though not directly shown in this simulation work hetero-junction TFET designs could be extremely beneficial (Chapter 4 discusses hetero-junction TFET design and fabrication). Hetero-junctions involving SiGe source and δp^+ SiGe source regions with Si channel and drain have been utilized [45][46] to increase the ON current of Si TFET with the same level of OFF current. Further this can also reduce/eliminate the problem of delayed output current saturation by reducing the potential drop across the tunnel junction.

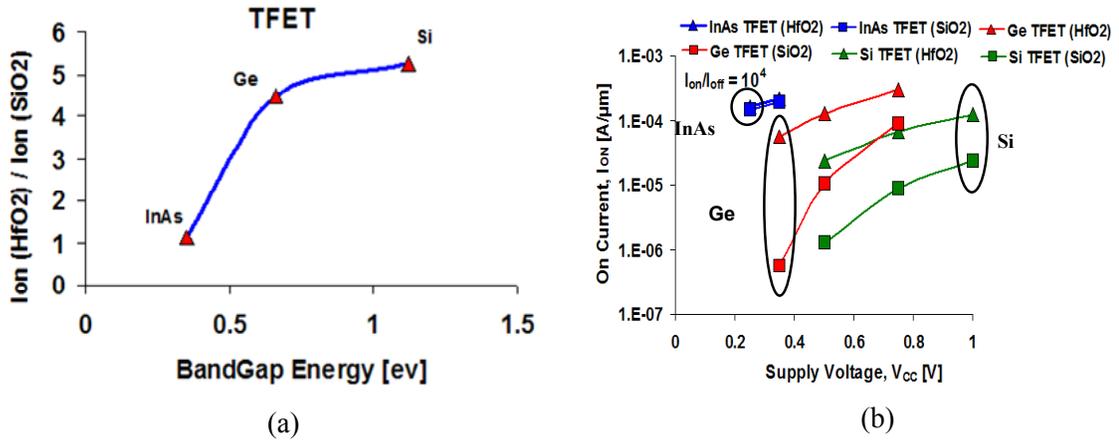


Figure 2-5. (a) Comparison of the effect of oxide scaling on TFET performance for different materials (b) Scaling of ON current with supply voltage for TFETs in different materials

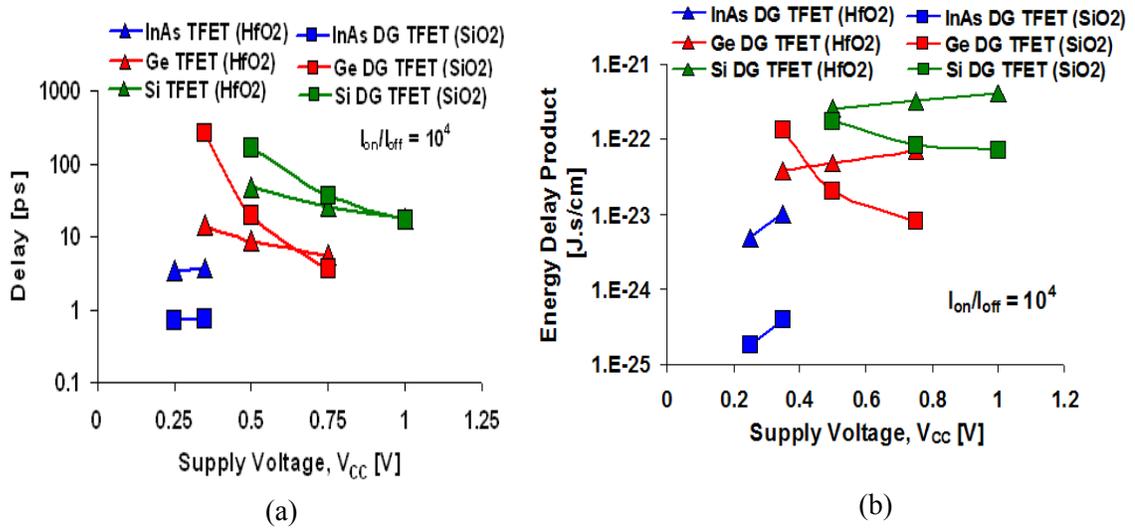


Figure 2-6. (a) Intrinsic Delay v/s Supply Voltage (b) Energy Delay Product v/s Supply Voltage

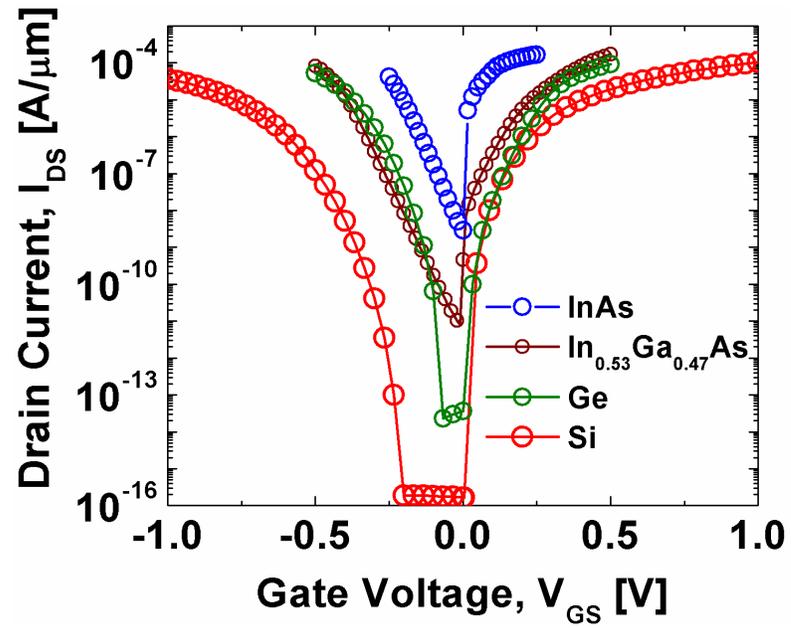


Figure 2-7. Transfer characteristics of InAs, $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, Ge and Si TFET are being compared on the same voltage scale. $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ gives the highest ON current at 0.5V, this material is therefore selected for the fabrication of first generation of tunnel transistors.

We have also looked at ternary compounds for TFET application. Figure 2-7 compares the transfer characteristics of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ TFET with that of Si, Ge and InAs TFET. It is quite evident from figure 2-7 that in the voltage range of 0.5-0.7V $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ TFET delivers the highest ON current and is therefore selected for TFET fabrication.

At this point it is worth pointing out that even though low band-gap and tunneling mass materials provide high ON current, its ambipolar leakage is also higher. But this higher ambipolar leakage can be circumvented by using some innovative device structures like (i) reduced drain side doping (ii) large band-gap drain and (iii) drain side under-lap design.

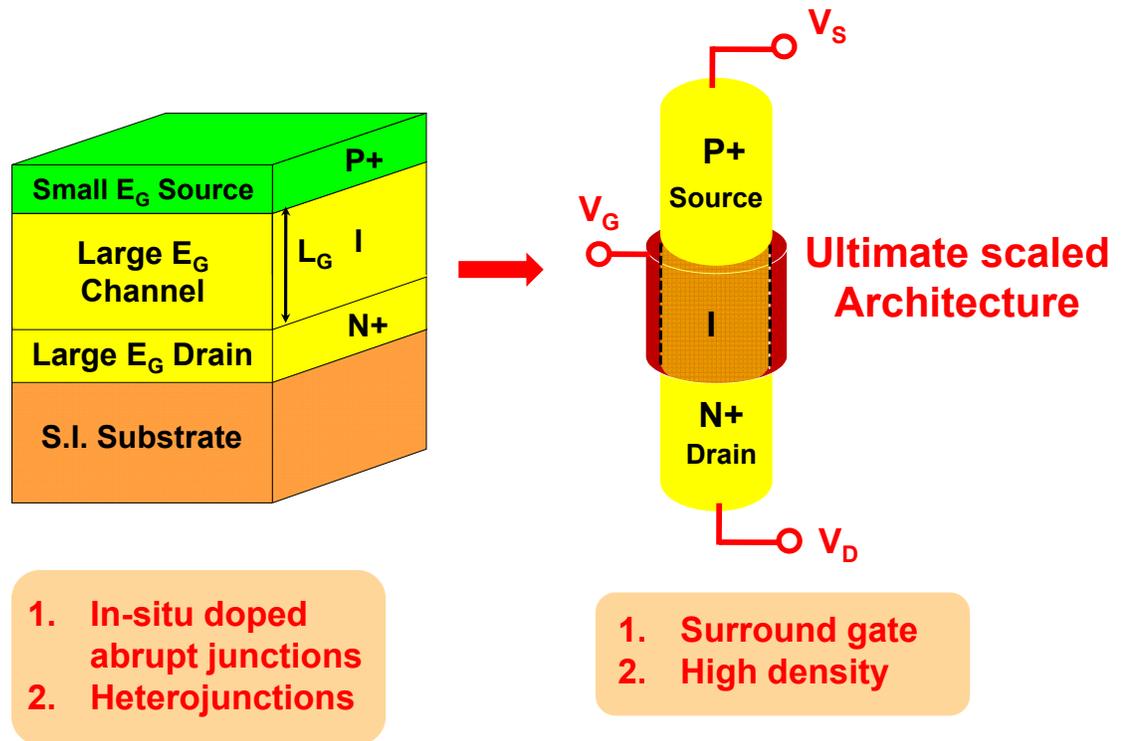


Figure 2-8. Advantages of a vertical TFET architecture. In-situ doped highly abrupt tunnel junctions can be created. Further hetero-junctions can be easily incorporated and such a vertical design can potentially result in the smallest foot-print device.

2.2 Device architecture selection: vertical vs. lateral

Having selected the material system of choice, the next step is to select the appropriate device architecture. For this, we need to realize that tunnel FET is essentially a gated pin diode. So, we need abrupt junctions for excellent gating action. In order to achieve this we decided to go with a MBE grown epitaxial layer structure (Figure 2-8). Here the junctions are in-situ doped and hence abrupt. Hetero-junctions can be easily incorporated in this design. We envision making a vertical transistor out of this which can feature a gate all around architecture. This design will also result in a small device footprint and therefore high density of transistors down the line. Compared to MBE grown vertical junctions ion-implanted lateral junctions are much more diffused and is therefore expected to have poor drive current.

2.3 Unidirectional conduction in TFET

Figure 2-9 shows the $I_{DS}V_{DS}$ (output) characteristics of a n-type Si TFET. The device exhibits expected characteristics due to tunneling during positive V_{DS} (reverse bias conditions) while I_{DS} increases significantly for two conditions when V_{DS} is negative (forward bias). When V_{DS} is $\sim -1V$, there is a significant I_{DS} irrespective of the value of V_{GS} . Significant current conduction is also observed when V_{DS} is slightly negative and V_{GS} is positive. This is due to electrons tunneling from the conduction band of intrinsic 'i' region to the valence band of p^+ source region.

This characteristic is very different from that of MOSFET which is a very symmetric device with current increasing for both positive and negative V_{DS} . This has important implication for the access transistor of an SRAM cell and hence its stability. In the following section we will analyze the performance of different SRAM designs with TFETs. Since analytical models for

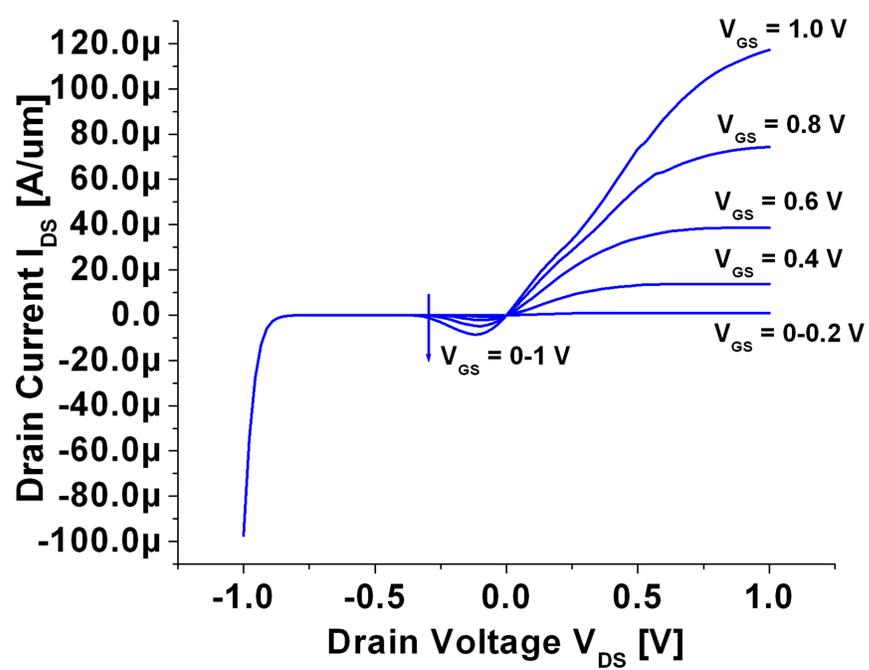


Figure 2-9. Output characteristics of Si NTFET

TFET are not available, we have built a look-up table based model using verilog-A for circuit simulation. The Verilog-A module is then used as instances for circuit simulation in Cadence Spectre. This efficient and accurate way of modeling is well suited for the emerging devices for which compact or SPICE models are not available [47]. In this model, IV and CV characteristics of the TFET devices are extracted using Sentaurus TCAD simulations and stored as two dimension look-up tables. We also observed enhanced miller capacitance (High C_{GD}) values for our devices and their effect was observed to be negligible for circuits with high electrical effort.

2.4 Different SRAM designs with TFET

Figure 2-10 shows various SRAM designs. Figure 2-10 (a) is the standard 6T SRAM cell and (b) and (c) show the 6T TFET SRAM design configuration with inward and outward access transistors. The read noise margin (RNM) of a SRAM design is estimated graphically as the length of a side of the largest square that can be embedded inside the lobes of a butterfly curve. The Write Noise Margin (WNM) is measured through the write trip point defined as the difference between V_{DD} and the minimum bit-line voltage required to flip the data storage nodes Q or QB. Figures 2-11 and 2-12 show an example of RNM measurement, read failure and WNM for a 6T TFET inward access transistor configuration shown in figure 2-10 (b). The 6T TFET SRAM design suffers from severe noise margin deficiencies due to the uni-directionality issue as shown in figure 2-13 and figure 2-14. Figures 2-13 and 2-14 show the read and write noise margins (RNM and WNM) for 6T TFET SRAM with inward and outward access transistor configurations. As mentioned above, we observe in figure 2-13 that the WNM reduces to 0 for cell ratio ($b = WPull-Down/WAccess$) > 0.3 while RNM is 0 for $b < 0.3$.

Similarly, figure 2-14 shows that RNM starts to increase only for Pull-up ratios ($WPull-Up/WAccess$) greater than 2 while WNM reduces to 0 for the same. Thus, a 6T TFET

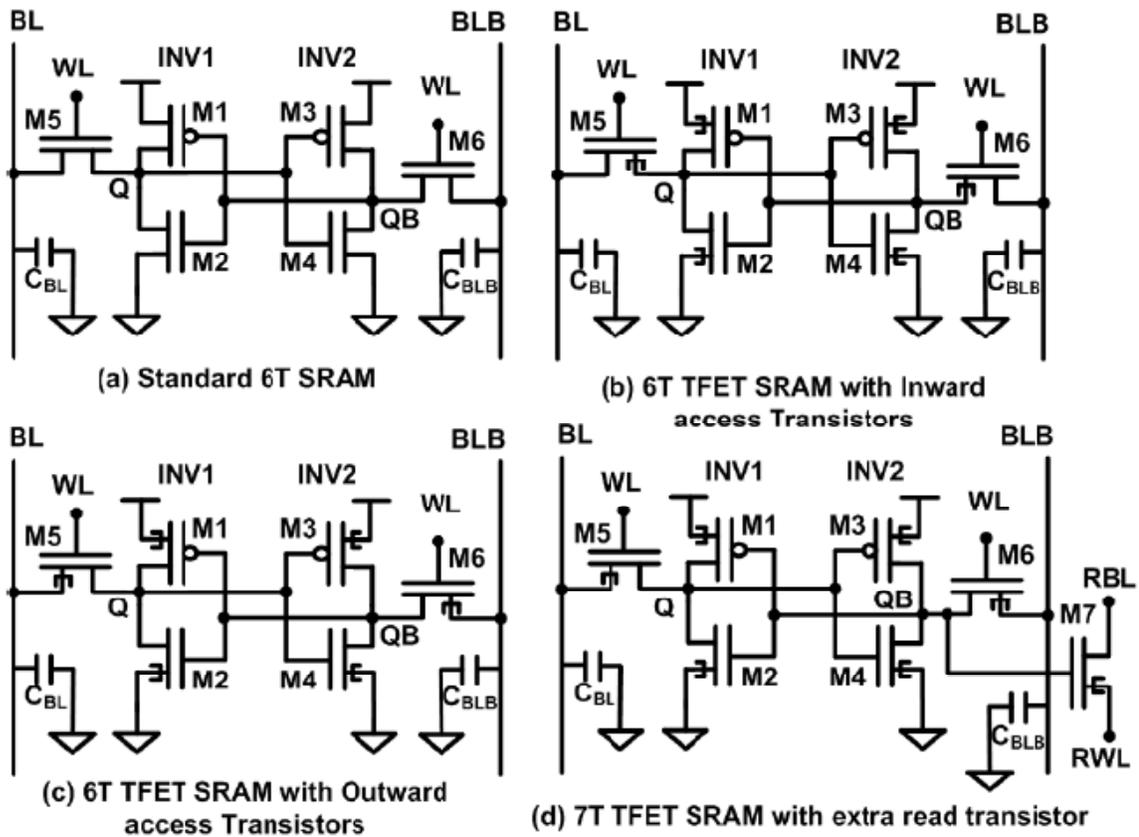


Figure 2-10. Different SRAM designs.

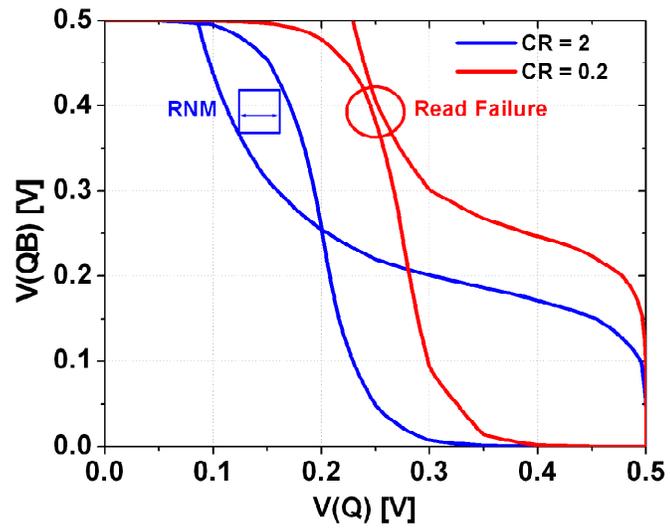


Figure 2-11. Measurement of read noise margin (RNM) and read failure.

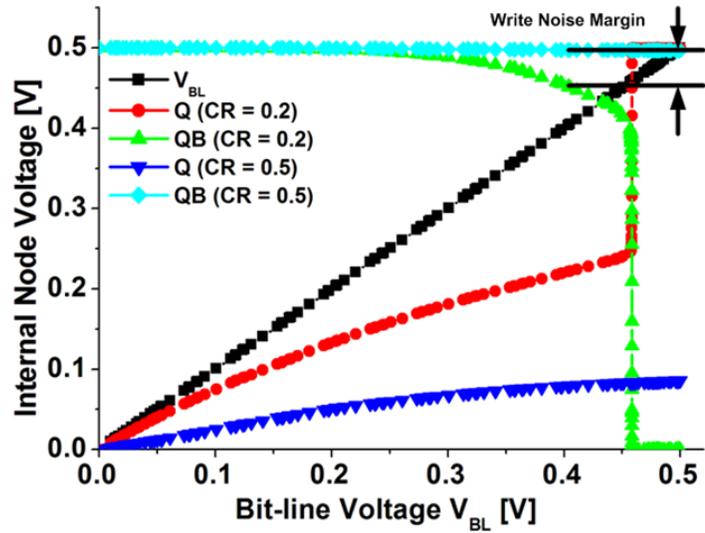


Figure 2-12. Measurement of write trip point (WTP) and write failure.

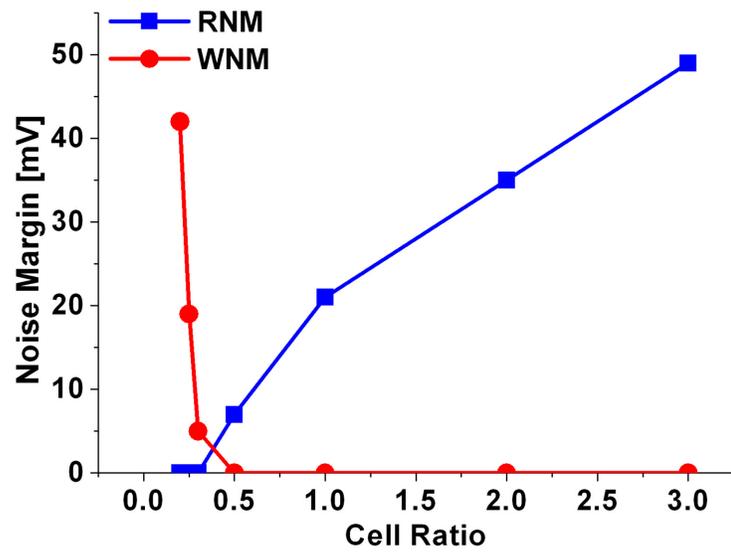


Figure 2-13. Noise margins for 6T TFET SRAM cell with inward access transistors at $V_{DD}=0.5V$.

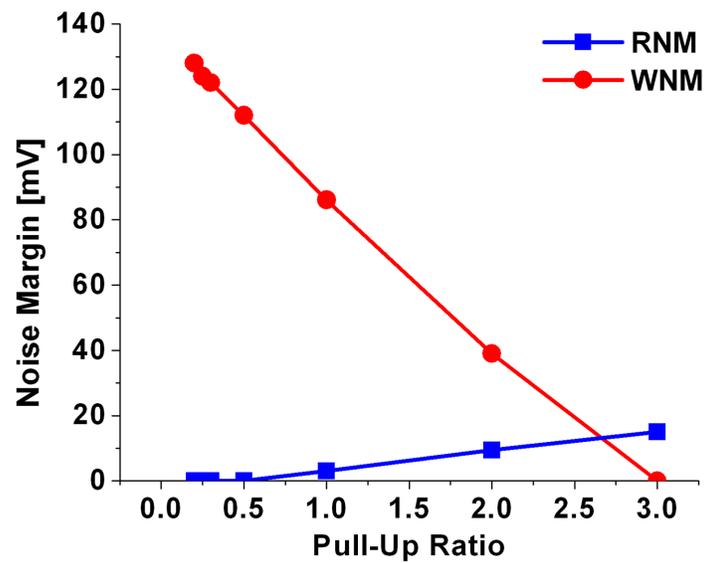


Figure 2-14. Noise margins for 6T TFET SRAM cell with outward access transistors at $V_{DD}=0.5V$

SRAM with acceptable stability margins is not possible. In order to have enough read and write margins, a 7T TFET SRAM configuration with outward access transistors was proposed in [48] as shown in figure 2-10(d). In this design, outward access transistor configuration is used to obtain the adequate write margin while the read margin is improved by providing a read-buffer with an extra transistor and separate read bit-line and word-line.

2.5 Novel 6T TFET SRAM design

As shown in the previous section, a conventional 6T TFET SRAM design is not feasible. We have proposed a novel 6T TFET SRAM, keeping minimum number of devices and preserving the adequate RNM and WNM as shown in figure 2-15. Our proposed design consists of cross coupled inverters (INV1 and INV2) with the bit-lines BL and BLB connected to node Q through the access transistors M5 and M6 (Note that both the access transistors are connected to the same node Q). It is a design strategy to provide a virtual ground to INV1 while writing either '1' or '0' to node Q. This virtual grounding helps in improving the WNM, by decoupling (or weakening of the re-generative action) of the cross-coupled inverters.

A. Read Operation

We use differential read operation in our proposed design. Both the bit-lines (BL and BLB) are pre-charged to V_{DD} and then the WL is asserted to '1'. If the bit stored at node Q is a '0', then BL discharges from V_{DD} and the sense amplifier is triggered. Otherwise, the bit-line BL remains pre-charged at V_{DD} unperturbed. Figure 2-16 (a) shows the current path during a read operation in our proposed design. We have chosen inward access transistor for read operation in our design since this configuration allows us to have a higher RNM than outward access transistor configuration as shown in figure 2-13 and figure 2-14 while our design strategy significantly improves the WNM as explained in the later sections.

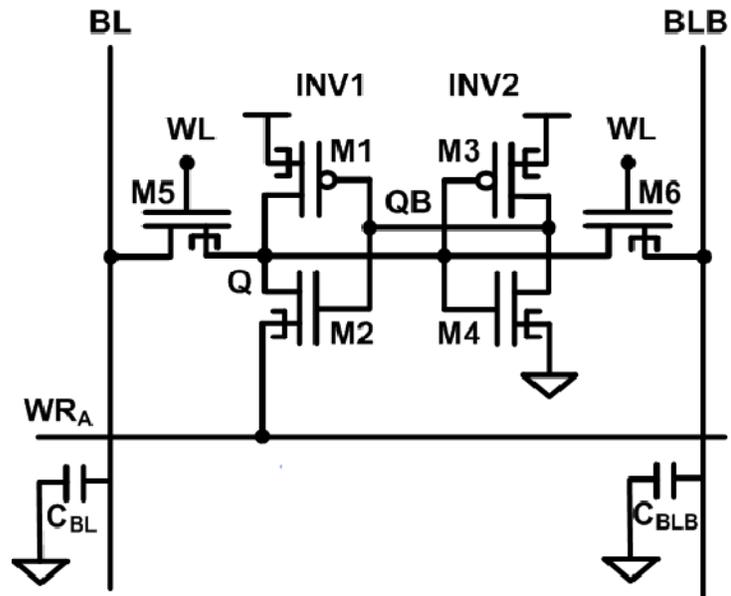


Figure 2-15. Novel 6T TFET SRAM design

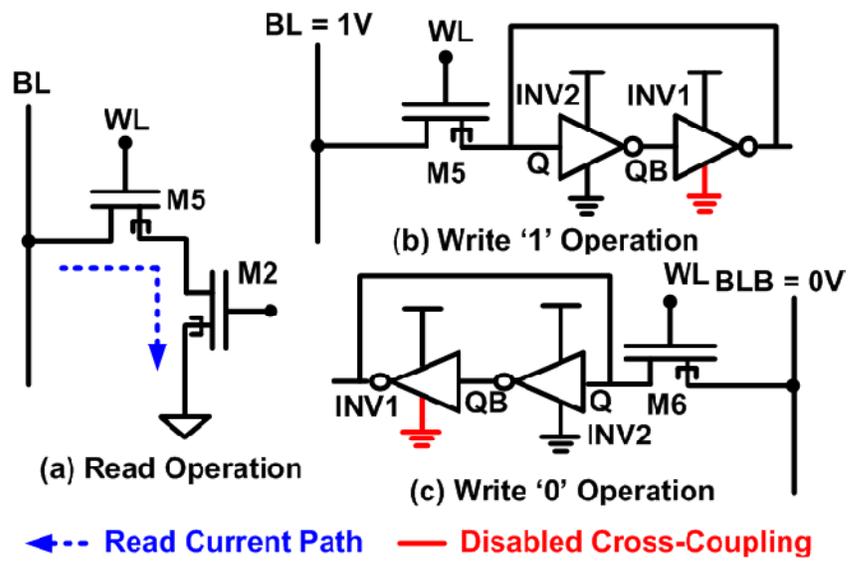


Figure 2-16. Read and write operation of the novel 6T TFET SRAM cell

B. Write Operation

The write operation in our design is done through one of our access transistors depending on the bit to be written onto the SRAM cell. To write a '1' onto Q, we charge the bit-line BL to V_{DD} and line WRA is also raised simultaneously to weaken the inverter INV1 and disable the cross-coupling between the two inverters. Once Q settles to a '1' and QB reaches '0', the WRA line is connected to ground and the cross coupling is enabled. Figure 2-16(b) shows the write '1' operation.

If the node Q stores a '1' and we intend to write a '0', the bit line BLB is pulled low to 0V. Simultaneously, the write enable line WRA is also raised simultaneously to virtual ground and the word line WL is asserted. This breaks the cross-coupling and Q is drained to ground through the access transistor M6. Once the node QB settles to a '1', the cross-coupling is enabled. Figure 2-16(c) shows the write '0' operation.

In order to demonstrate a successful read and write operation, we have simulated the RNM and WNM of the proposed 6T TFET SRAM for different cell ratios (b) at $V_{DD}=0.5V$ when the pull up ratio is kept at minimum. In figure 2-17, the RNM at half pre-charged bitline is much better than fully pre-charged bit-line. For $b > 2$, there is no significant improvement in the RNM while a slight degradation in the WNM is observed, also using the higher cell ratio will increase the cell area. Hence, in all the simulations we have used cell ratio (b) of 2 unless specified. Due to the asymmetric nature of the proposed design, writing a '1' is more difficult than writing '0', hence, we have only measured the WNM for writing a '1'.

2.5.1 Benchmarking

Stability, performance and power of a SRAM cell are the three key design metrics in the nanometer regime. For comparison, we have used the existing 6T CMOS SRAM and 7T TFET

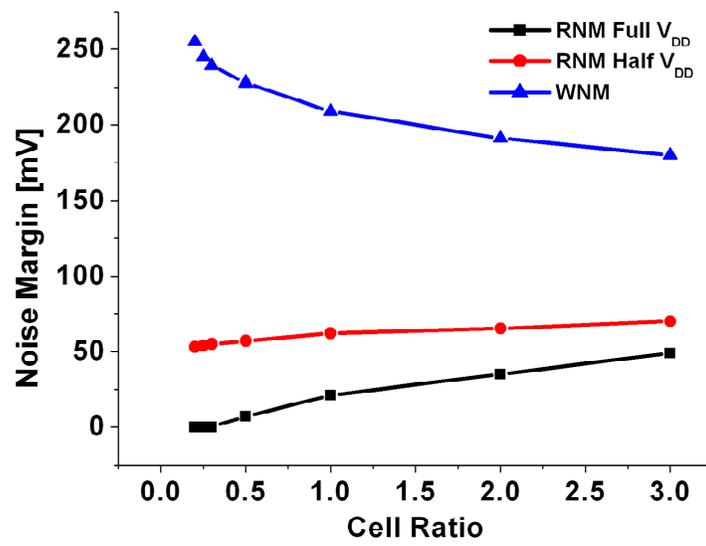


Figure 2-17. Noise margins for modified 6T TFET SRAM cell with inward access transistors at $V_{DD}=0.5V$

SRAM design. We use 32nm Predictive Technology Models (PTM) [49] for 6T CMOS, while the 6T and 7T TFET SRAMs are simulated as discussed earlier.

A. Stability

An adequate read and write stability is highly desirable for a successful realization of a SRAM cell. The RNM and WNM are the widely used metrics for stability analysis of a SRAM cell. Figure 2-18 shows the RNM of different designs. The proposed 6T TFET SRAM and 6T CMOS have bit-lines BL and BLB pre-charged to full V_{DD} and half V_{DD} . The 7T TFET SRAM cell shows the highest RNM, because of the isolated read-buffer which yields the RNM equivalent to Hold Static Noise Margin (SNM). The isolated read buffer concept has been widely explored in CMOS SRAM designs to improve RNMs. However, the proposed 6T TFET with fully pre-charged bit-line has the lowest RNM. This is because of the single access transistor which conducts during the read operation and rises the internal node (Q) voltage to a higher value than a 6T CMOS SRAM (while the other access transistor does not assist because of its unidirectionality). The RNM of the proposed 6T TFET with half-swing is much better than the 6T CMOS with half and full pre-charged bit-lines. In 6T CMOS SRAM, half pre-charged bit-lines are not as effective as 6T TFET SRAM. This is due to the symmetric nature of SRAM where one of the bit-lines connected to a node (Q or QB) via access devices storing a V_{DD} is also pre-charged to half V_{DD} . This scenario is not effective in holding that node at V_{DD} as compared to pre-charging to full V_{DD} due to conduction from the node to bit-line in the former case. However in our proposed 6T TFET design, M6 in figure 2-15 does not conduct in the reverse direction and this contributes to higher RNM at half pre-charged V_{DD} . At $V_{DD}=0.3V$, we observe a 63% improvement in RNM over a 6T CMOS while it is 59% lesser than a 7T TFET. The advantage of 7T TFET purely comes from the extra transistor used as a read port. Figure 2-19 shows the WNM of SRAM cell designs for different V_{DD} . The WNM of the proposed 6T TFET SRAM design is higher than its counterpart designs due to weakening of the inverter which enables a faster write.

At $V_{DD}=0.3V$, we observe a 46% and 32% improvement in WNM over 6T CMOS and 7T TFET respectively.

B. Performance

Read and write delays are the metrics used to compare the performance of different SRAM designs. In 6T CMOS and 6T TFET read delay is defined as the time delay between 50% of word line (WL) activation to 10% of pre-charged voltage difference between the bit lines. In 7T and 8T SRAM designs, bit-line sensing is done using CMOS logic gates and not by using differential sense amps [50] [51]. So, for the 7T TFET design, read delay is measured between 50% of word line (WL) activation to 50% of pre-charged bit line voltage. Figure 2-20 shows the read delay of different SRAM designs. We observe that CMOS performs better than TFETs in the entire voltage range due to its high drive current. At $V_{DD}=0.3V$, 6T CMOS design has a better read delay than 6T TFET and 7T TFET by 40% and 58% respectively. However, this problem can be solved in TFETs by moving to lower band-gap and low effective mass materials such as Indium Arsenide (InAs) which have a higher tunneling rate through the barrier and higher drive current (I_{ON}) of $\sim 85 \mu A/\mu m$ for $V_{DD}=0.25V$ [34].

The write delay is defined as the time between the 50% activation of the word line (WL) to when the internal Q is flipped to 90% of its full swing. At lower voltages, write delay of the proposed 6T TFET SRAM design is significantly less than the 6T CMOS and 7T TFET SRAM designs as shown in figure 2-21. This is due to the simple fact of breaking the cross coupling which enables a faster write speed than other designs. The write delays for 6T CMOS and 7T TFETs are 8.1X and 4.7X times higher than the proposed 6T TFET design at $V_{DD}=0.3V$.

C. Leakage Power

Due to the inherent nature of TFETs, the OFF state leakage current of a TFET is orders of magnitude lower than CMOS. Thus, we see a huge improvement in terms of leakage reduction. Figure 2-22 shows the standby leakage/cell of various SRAM designs. Both 6T and 7T TFET

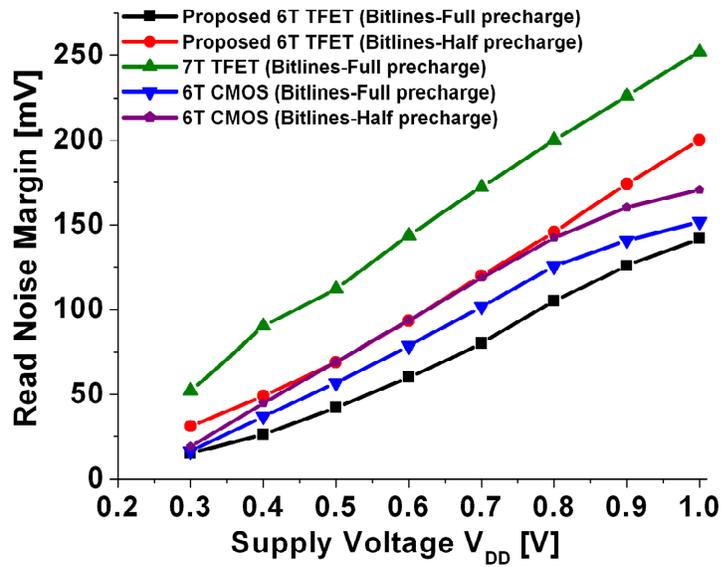


Figure 2-18. Read noise margins for various designs at different supply voltages.

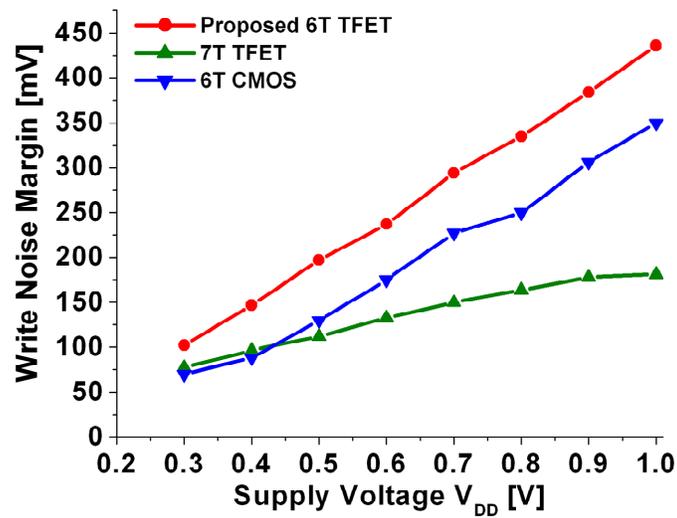


Figure 2-19. Write noise margins for various designs at different supply voltages.

have equal leakage power due to the presence of the same leakage paths. We obtain a 700X and 1600X improvement in leakage reduction over CMOS designs at 0.3V and 0.5V V_{DD} . This shows that TFETs are a potential replacement candidate for CMOS transistors at low voltage and low power applications.

D. Area

The proposed 6T TFET SRAM cell is not expected to have an area increase while a 7T TFET SRAM is bound to have an increase of around 15% [48]. Thus, a design with comparable margins and better performance can be obtained using a 6T instead of 7T.

In conclusion, we have proposed a novel 6T Si-TFET based SRAM design to enable ultra-low voltage and low power operation. We show that our proposed 6T Si-TFET SRAM cell has comparable margins and better performance than the 7T TFET SRAM design. We also obtain a significant improvement in leakage reduction over the entire voltage range and find TFETs to be a suitable candidate for replacement of CMOS in SRAM designs at ultra low voltages such as 0.3V. Our design has superior margins and performance except for read delay than CMOS due to the low drive current. The use of lower band gap materials such as Indium Arsenide (InAs) is expected to further boost the TFET performance.

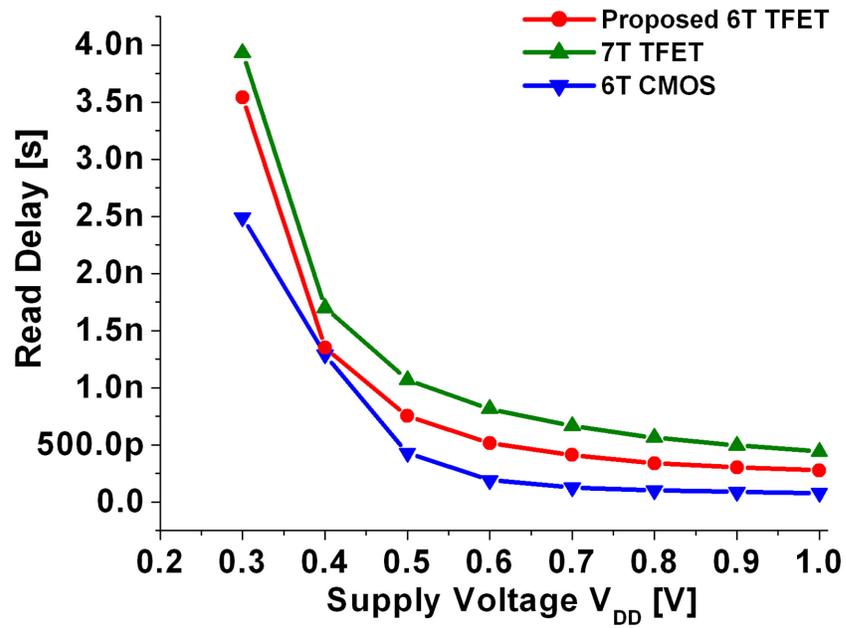


Figure 2-20. Read delay for various supply voltages.

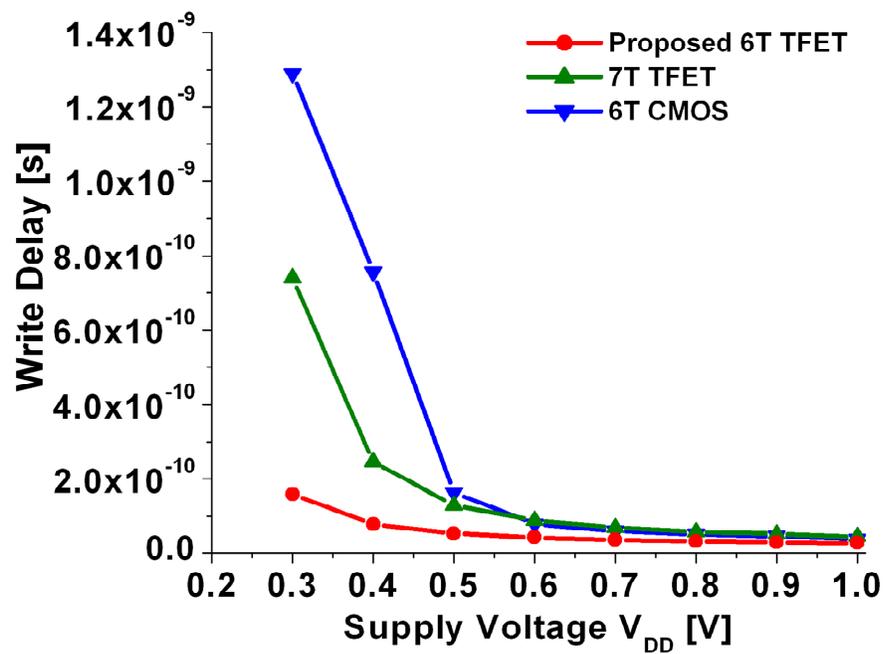


Figure 2-21. Write delay for various supply voltages.

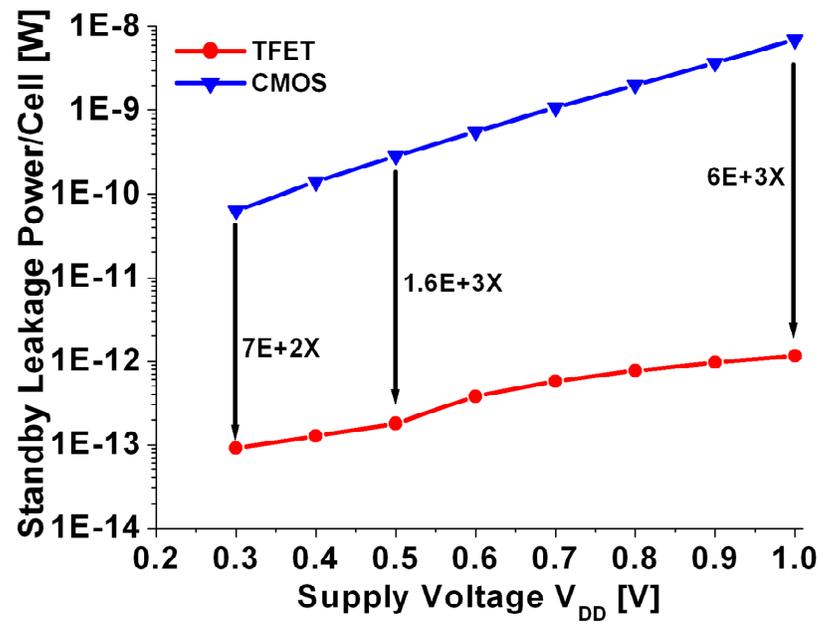


Figure 2-22. Standby leakage/cell for CMOS and TFET SRAM designs.

Chapter 3

Logic Circuits: A simulation study

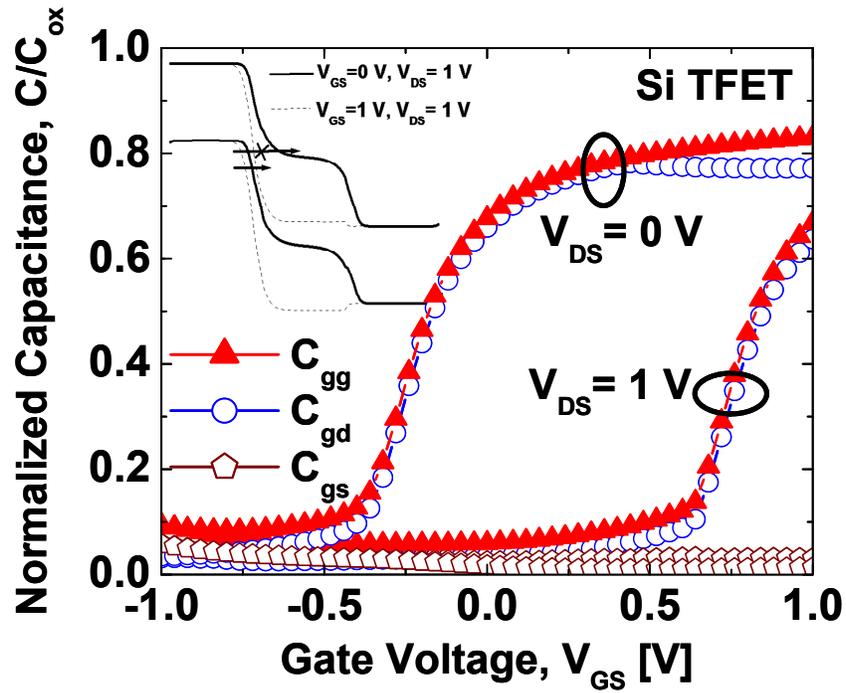
This chapter presents the digital switching behavior of TFET. This chapter is divided into two main sections. Section 3.1 describes the physics of enhanced miller capacitance in TFET and its effect on large signal digital switching. Section 3.2 gives a quantitative estimate of the actual switching capacitance and effective drive current that should be used for calculating the intrinsic delay of TFET, the difference with MOSFET is clearly explained. This chapter further highlights the importance of proper benchmarking of TFET.

Recent work has been done to benchmark the intrinsic delay of the TFETs with MOSFETs. While reference [52] uses $C_{ox}V_{DD}/I_{ON}$ where C_{ox} is the oxide capacitance, reference [53] uses $C_{gg}V_{DD}/I_{ON}$ where C_{gg} is the total gate capacitance of the TFET including the quantum capacitance of the channel. The reference [54] uses the metric $(Q_{on}-Q_{off})/I_{ON}$ where Q_{on} and Q_{off} are the total charge in the ON and OFF states of the transistor, respectively, thereby taking into account the nonlinear charge-voltage relationship in TFETs. It has been shown in [54] that the intrinsic speed of TFETs can be higher than MOSFETs over a certain range of I_{ON}/I_{OFF} ratios because of the smaller charge involved in the entire switching process. However, the intrinsic speed of the transistor could be deceptive in predicting the large signal switching performance of a digital circuit. To the best of our knowledge, no work has been done before to investigate the circuit level switching behavior of TFETs and extract the effective output capacitance and drive current in order to correlate the CV/I device metric to the large signal switching delay ($\tau_f=0.69R_{sw}(C_{EFF} + C_L)$, $R_{sw}=V_{DD}/2I_{EFF}$) at the circuit level. In this chapter we show that the effective load capacitance for TFET based unloaded inverters can be more than double the gate capacitance as a direct manifestation of enhanced miller effect and the effective drive current can be extracted

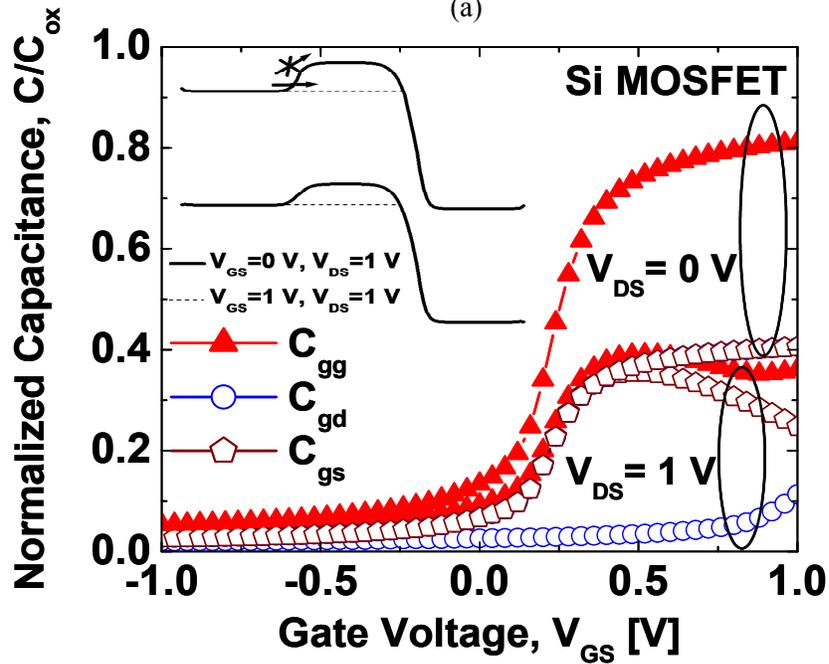
from a simple 3-pt model tracking the actual switching current trajectory in inverters.

3.1 Miller effect in TFET

Both MOSFET and TFET device structure used in this simulation study have a double gate configuration same as in figure 1-3. As before a non-local tunneling model is used for the simulation of tunnel current which accounts for the actual spatial charge transfer across the tunnel barrier by considering the actual potential profile along the entire path connected by tunneling. Figure 3-1(a) and 3-1(b) show the Si TFET and MOSFET capacitance versus voltage characteristics at $V_{DS} = 0$ V and 1.0V, normalized to the gate oxide capacitance, $C_{ox} (= \epsilon_{ox}/t_{ox})$. It is clearly seen that for TFETs the gate-to-drain capacitance (C_{gd} - miller capacitance) reflects the entire gate capacitance (C_{gg}) and the gate-to-source capacitance (C_{gs}) remains very small due to the presence of source side tunnel barrier. C_{gd} increases at positive gate voltages due to the reduction in channel to drain side potential barrier as depicted in the inset of figure 3-1(a). It is worth noting that, even at $V_{GS}=V_{DS}=1$ V the gate capacitance, C_{gg} in Si TFET is dominated by C_{gd} . In TFETs, the pinch-off point is pushed to higher values of V_{DS} for higher V_{GS} 's as observed in the output characteristics later in figure 3-8. The fundamental reason for this is that, at higher V_{GS} , there is higher band bending at the source-channel end in TFETs which implies a larger percentage of the drain to source bias appears on the source side. Thus, for a given gate voltage (e.g. $V_{GS} = 1$ V), the drain voltage continues to impact the source side tunnel barrier till $V_{DS} = 1$ V, beyond which the pinch-off finally starts to set in and C_{gd} starts decreasing. This is clearly seen in figure 3-2(a) which plots the normalized C_{gd} as a function of the drain voltage V_{DS} for different gate voltages, V_{GS} . For $V_{GS}=1$ V, C_{gd} starts decreasing only at drain voltages (V_{DS}) exceeding 1V due to delayed pinch-off. In MOSFETs both C_{gs} and C_{gd} contribute half of the total gate charge in



(a)



(b)

Figure 3-1. Capacitance-voltage characteristics showing the gate (C_{gg}), gate-to-source (C_{gs}) and gate-to-drain (C_{gd}) capacitances as a function of gate to source voltage, V_{GS} , for (a) Si TFET and (b) Si MOSFET.

the linear region and C_{gd} becomes negligible in saturation region due to higher potential barrier between the channel and the drain thus causing the majority of the contribution to the gate capacitance to originate from the source (C_{gs}). In contrast to TFETs, the pinch-off in MOSFETs takes place at V_{DSSAT} given by $V_{GS} - V_T$ and, hence, at $V_{GS}=V_{DS}=1V$ the channel is well pinched off and the gate capacitance C_{gg} is mainly dominated by C_{gs} . This is again more clearly visualized in figure 3-2(b), where C_{gd} in Si MOSFETs for $V_{GS}=1V$ starts decreasing at drain voltage (V_{DS}) of 0.6V which is an indication of early saturation.

This high gate to drain capacitance (C_{gd}) inherent to the TFET device operation has strong implications for its transient response [55]. Figure 3-3(a) shows the transient response for Si TFET and MOSFET inverter for an input step voltage with peak to peak voltage of 1V and 5 picosecond rise time. Si TFETs can be seen to suffer from an output voltage overshoot of 0.9V (90% of peak input voltage) due to the large miller feed through capacitance originating from its fundamental device operation coupled with its low drive current compared to the MOSFETs. Figure 3-3 (b) compares the normalized values of the input to output capacitance or the miller capacitance (C_M) for MOSFET and TFET inverters as a function of its input voltage. The contribution to the total miller capacitance comes from the gate-to-drain capacitance (C_{gd}) of both the n and p type transistor and is tabulated in Table 3-1. For MOSFET inverters in region A, B, D and E one of the transistors remains in the linear region resulting in $C_M=C_{gd}=0.5C_{gg}$. The dip seen in the miller capacitance (Region C) is due to both the transistors entering the saturation region during the input ramp from 0-1 V. In contrast, in the TFET inverter, both the pull-up and pull-down transistors barely enter saturation (due to delayed pinch-off behavior) and, thus, the overall miller capacitance between the input and output nodes maintains a value of $C_M=C_{gd}=1.1 C_{gg}$ throughout the entire transition of the input ramp signal. In Si TFET inverter, where the pull-down device has a very large on resistance due to poor transmission through the source to channel

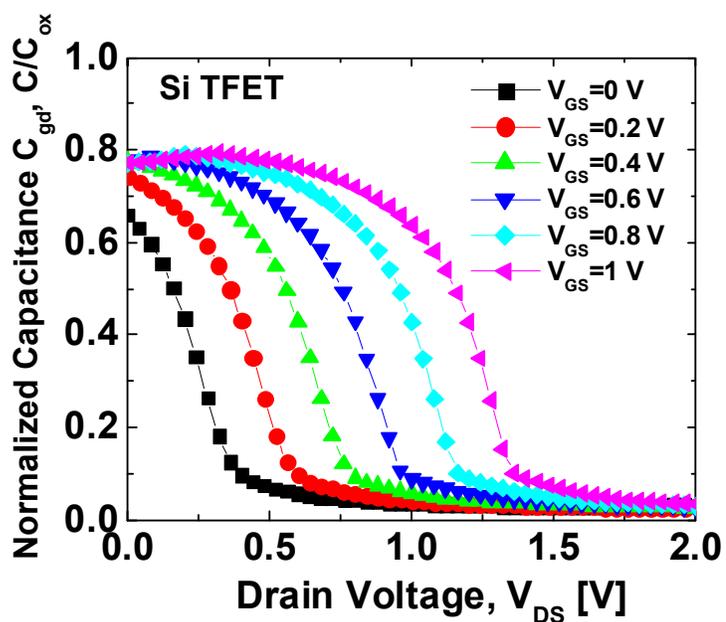
tunnel barrier, the extent of this overshoot can be calculated from the following charge conservation equation [56];

$$C_L V_{MAX} + C_M (V_{MAX} - V_{DD}) = (C_M + C_L) V_{DD}$$

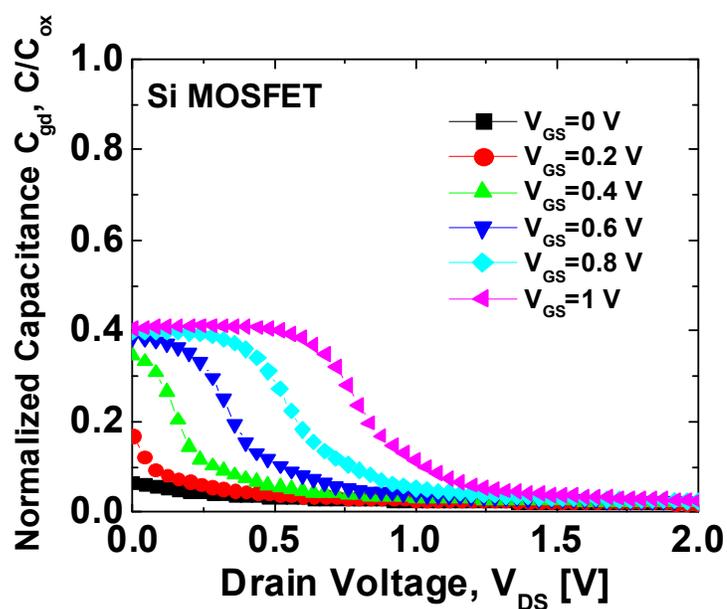
$$V_P = V_{MAX} - V_{DD} = \frac{C_M}{C_M + C_L} V_{DD} \quad (1)$$

where C_M is the miller capacitance connecting the input and output of the inverter comprising the gate to drain capacitance of both p-TFET and n-TFET and C_L is the load capacitance external to the device, V_{MAX} is the maximum voltage to which the output voltage rises, V_P is the peak value of the overshoot and V_{DD} is the supply voltage. This equation clearly shows the impact of higher Miller capacitance on the peak overshoot voltage in Silicon based TFETs.

Lower band gap InAs (indium arsenide) based TFETs have been recently proposed [34] as a promising candidate material for implementing TFET architecture at supply voltages of $V_{DD}=0.25$ V. InAs TFETs have high drive current (I_{ON}) at lower supply voltages due to its lower tunnel barrier height and width as well as lower tunneling mass, and its gate capacitance, C_{gg} , is limited by the quantum capacitance originating from its reduced density of states. Figure 3-4(a) illustrates the capacitance-voltage characteristics of InAs TFETs showing that the total gate capacitance (C_{gg}) is only 10% of the gate oxide capacitance (C_{ox}). Again C_{gd} is the dominant contributor to C_{gg} due to the inherent tunnel transistor architecture but the capacitance value is significantly lower than that of Si TFETs at $V_{DD}=1$ V. Further, the on-resistance of the InAs TFETs is considerably lower than that in Si TFETs. This lower feed forward miller capacitance along with higher drive current provided by the pull-down device at lower input voltages reduces the peak overshoot voltages in InAs TFET inverters to less than 20% of input peak voltage as shown in fig. 3-4(b). Figure 3-5 compares the effect of external capacitance loading (i.e. *electrical effort*) in Si and InAs based TFET inverter on the percentage voltage overshoot. Both

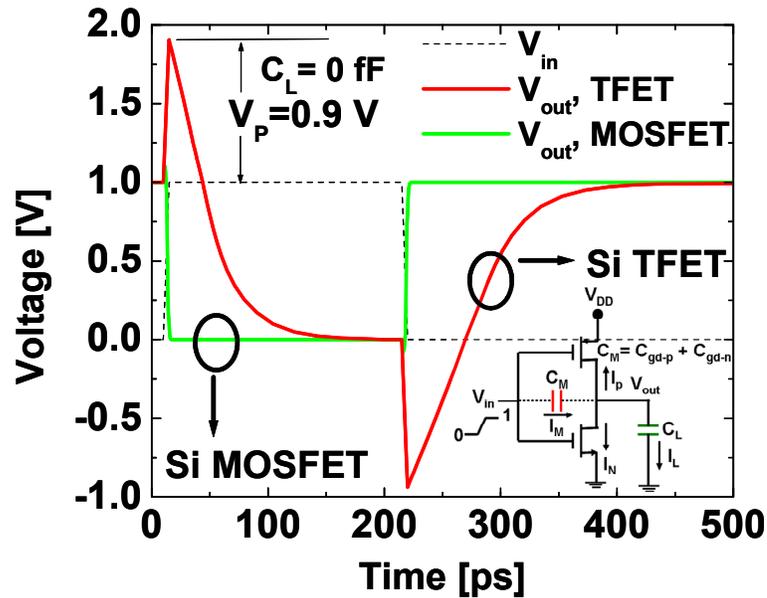


(a)

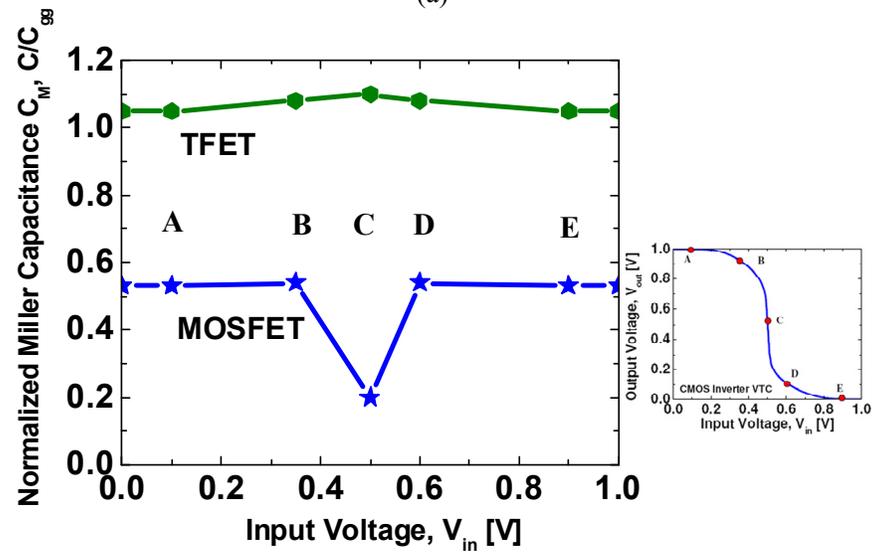


(b)

Figure 3-2. Normalized gate-to-drain capacitance, C_{gd} as a function of drain to source voltage, V_{DS} for different gate to source voltages, V_{GS} for (a) Si TFET and (b) Si MOSFET.



(a)



(b)

Figure 3-3. (a) Transient response of silicon TFET and MOSFET inverter for an input ramp of 0-1 V in 5 ps. The load capacitance, C_L , is set to zero in this simulation. TFETs exhibit a significantly higher voltage overshoot as well as undershoot due to higher miller capacitance, C_{gd} , and lower ON current. (b) Normalized miller capacitance for TFET/MOSFET inverter as a function of input voltage of the inverter. The demarcated regions A-E are based on the transitions in the device operating point on the MOSFET/TFET inverter DC transfer characteristics.

TFET inverters show a reduction in peak overshoot with increased capacitive loading as expected from equation (1) but the overshoot is significantly smaller for InAs based TFET inverter due to its smaller switching resistance (higher drive current at lower supply voltages) and reduced miller capacitance, C_{gd} .

Table 3-1: Miller capacitance $C_M = C_{gd,n} + C_{gd,p}$ for Si TFET/MOSFET inverter for various points along the DC transfer characteristics as shown in figure 3-3(b), here $C_{gg} = 0.8C_{ox}$.

	A	B	C	D	E
MOSFET	$0.5C_{gg} + 0.03C_{gg}$ (p-lin, n-cutoff)	$0.5C_{gg} + 0.04C_{gg}$ (p-lin, n-sat)	$0.2C_{gg}$ (p-sat, n-sat)	$0.5C_{gg} + 0.04C_{gg}$ (p-sat, n-lin)	$0.5C_{gg} + 0.03C_{gg}$ (p-cutoff, n-lin)
TFET	$C_{gg} + 0.05C_{gg}$ (p-lin, n-cutoff)	$C_{gg} + 0.08C_{gg}$ (p-lin, n-sat)	$1.1C_{gg}$ (p-sat, n-sat)	$C_{gg} + 0.08C_{gg}$ (p-sat, n-lin)	$C_{gg} + 0.05C_{gg}$ (p-cutoff, n-lin)

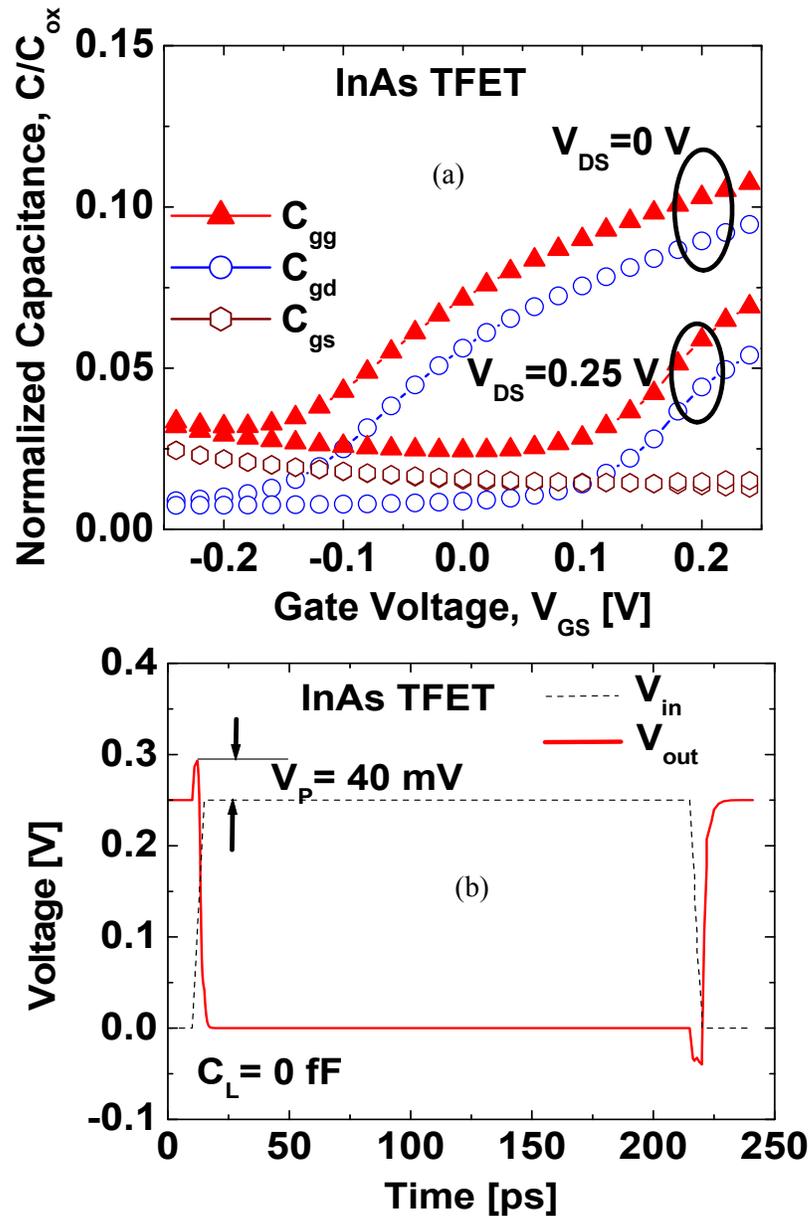


Figure 3-4. (a) Capacitance-voltage characteristics of an InAs TFET showing the gate (C_{gg}), gate-to-source (C_{gs}) and gate-to-drain (C_{gd}) capacitances as a function of gate to source voltage, V_{GS} . Note that the supply voltage is $V_{DD}=0.25$ V. (b) Transient response of an InAs TFET inverter for an input ramp of 0-0.25 V in 5 ps. InAs TFET exhibits a significantly smaller voltage overshoot/undershoot due to smaller Miller capacitance and higher I_{ON} compared to Si TFETs.

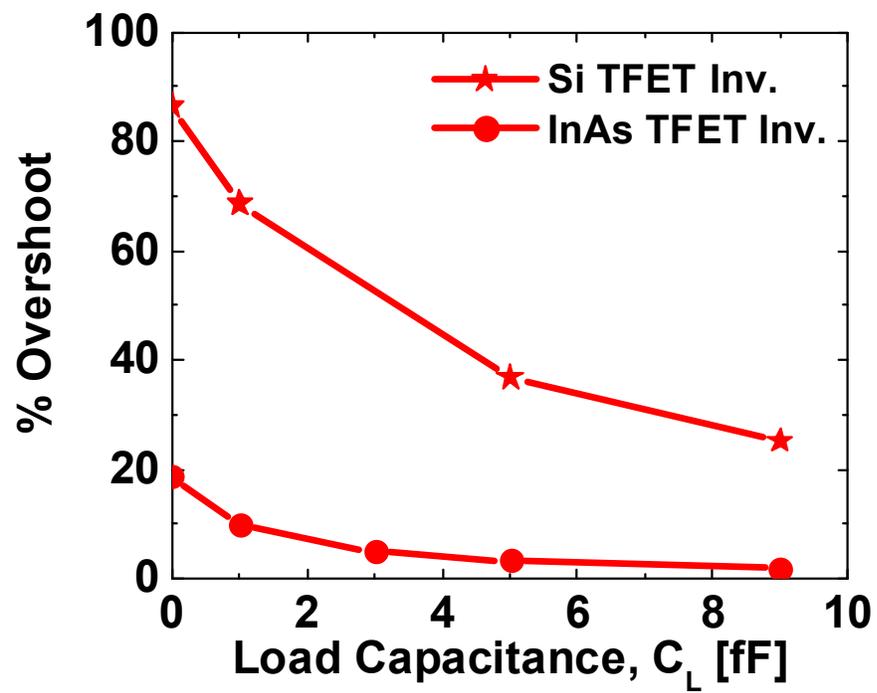


Figure 3-5. Percentage overshoot as a function of load capacitance (C_L) for Si and InAs TFET inverter.

3.2 Effective output capacitance and drive current

Table 3-2 compares the actual inverter fall delay obtained from inverter transient response (Figure 3-3 and 3-4) with some common metrics used to benchmark MOSFET inverter delay. For comparison the same metrics have also been applied for TFET inverters to understand its effectiveness in predicting TFET inverter performance. Here C_{gg} refers to the gate capacitance in the linear operation region ($V_{GS}=V_{DD}$ and $V_{DS}=0$ V) including the channel capacitance arising from the density of states limitation and is equal to $0.8C_{ox}$ for Si TFET/MOSFET and $0.1C_{ox}$ for InAs TFET while I_{ON} refers to the saturation drive current, I_{DSAT} , at $V_{GS} = V_{DS} = V_{DD}$. The commonly used metrics differ from the actual MOSFET inverter fall delay with an error which is unacceptable for today's scaled CMOS technologies with scaled threshold voltages. It was shown in [57] and [58] that an effective drive current (I_{EFF}) needs to be used to predict the actual delay of a MOSFET inverter instead of I_{ON} since the actual switching current could be significantly lower than the saturation current of an individual transistor. Analytical models were also suggested to calculate the average or effective drive current (I_{EFF}) by taking into account the actual inverter switching current trajectory. Table 3-2 clearly highlights the fact that the commonly used benchmarking metrics applied so far also significantly differ from the TFET inverter performance and, therefore, a need arises to accurately quantify the effective output capacitance and the effective switching current to predict the TFET performance. In this paper, we focus on accurately estimating the CV/I metrics in TFETs in two materials systems, Si and InAs, and present the Si MOSFET results only for comparison. Silicon and indium arsenide are chosen since they represent the high density-of-states (DOS) and low DOS materials categories, respectively.

We have analyzed the fall delay (high-to-low transition of the output voltage) to extract the effective load capacitance and the effective switching current. The fall delay is defined as the

Table 3-2: Comparison of actual inverter delay with commonly used benchmarking techniques

Delay [ps]	$\frac{C_{ox} V_{DD}}{2I_{ON}}$	$\frac{C_{gg} V_{DD}}{2I_{ON}}$	$\frac{Q_{ON} - Q_{OFF}}{I_{ON}}$	Inverter Fall Delay, τ_f
Si MOSFET	1	0.8	0.63	1.15
Si TFET	18.5	15	8	48
InAs TFET	3.5	0.38	0.3	1.1

time interval between the 50% of input voltage (V_{in}) to the 50% of output voltage (V_{out}) in the transient response. Figure 3-6 shows the fall delay for Si TFET, Si MOSFET and InAs TFET inverters for different values of load capacitance (C_L) obtained through detailed device level mixed mode simulations. It is clearly seen that the Si TFET exhibits an order of magnitude higher fall delay compared to the Si MOSFET and InAs TFET due to its low I_{ON} and the additional voltage overshoot due to the miller feed through effect. A simple RC model is often used to calculate the fall delay (τ_f) in CMOS inverters assuming a total load capacitance ($C_L + C_{EFF}$) discharging through a constant resistor (R_{sw}). The fall delay is expressed as:

$$\tau_f = 0.69R_{sw}(C_{EFF} + C_L) \quad (2)$$

$$R_{sw} = \frac{V_{DD}}{2I_{EFF}} \quad (3)$$

where C_{EFF} is the effective output capacitance of the unloaded inverter. C_{EFF} comprises of contributions from the intrinsic gate-to-drain capacitances (C_{gd}) of both the n and p type transistor, C_L is the additional load capacitance external to the device. R_{sw} is the effective switching resistance of the N-type TFET/MOSFET through which the total output capacitance ($C_{EFF} + C_L$) discharges, V_{DD} is the supply voltage and I_{EFF} is the effective switching current through R_{sw} pulling the output node of the inverter to ground. Equation (2) shows that the

effective switching resistance (R_{sw}) can be extracted from the slope of the fall delay (τ_f) v/s load capacitance (C_L) and the y-intercept will be the total capacitance between the output node of the inverter and ground which is intrinsic to the device (C_{EFF}). Once R_{sw} is obtained the effective drive current, I_{EFF} , can be easily extracted from equation (3). These extracted values are tabulated in table 3-3. It is important to note at this point that the large delay benefit ($\sim 45X$ at $C_L = 0$ fF) obtained in going from Si to InAs TFET inverters (Table 3-2) comes from both the 8X reduced effective output capacitance as well as 5.7X smaller switching resistance. The most notable difference between MOSFET and TFET shows up in the right most column of the effective output capacitance (C_{EFF}) in table III. The effective output capacitance for Si and InAs TFET inverters shows up as 2.6 times the gate capacitance, C_{gg} , as opposed to 0.9 times the gate capacitance, C_{gg} , for Si MOSFET. The fundamental cause of increased effective capacitance in TFET is due to the high gate-to-drain capacitance in TFETs which is enhanced by the Miller effect. A similar Miller effect effect has also been observed in Si MOSFET but the absolute value of gate to drain capacitance, C_{gd} , is much smaller in MOSFET compared to that in TFET [18]. The concept of this Miller effect is schematically illustrated in figure 3-7. The Miller effect in digital switching arises when time varying voltages are moving in opposite directions on both sides of a capacitor. This is the case for the gate-to-drain capacitance C_{gd} connected between the input terminal (gate) and the output terminal (drain) of an inverter, for both MOSFET and TFET. The effective capacitance at the output node is double this input to output capacitance, C_{gd} , due to the Miller effect. It is worth pointing out that $C_{EFF} \sim 2.6C_{gg}$ as extracted from figure 3-6 is slightly higher than $\sim 2.2C_{gg}$ expected from table I since the capacitances listed in table I have been extracted at fixed DC bias points under quasi-static assumption along the inverter VTC (figure 3-3(b)) as opposed to the actual capacitances that change in a non-quasistatic manner during transient switching of the inverter. Ignoring the impact of this enhanced output capacitance due to Miller effect would lead to severe underestimation of the TFET effective switching capacitance.

Similarly, the correct switching current also needs to be extracted from the output I-V characteristics of the TFET to estimate the fall delay. This current needs to be consistent with the effective current extracted from the simple RC model and enumerated in Table 3-3.

In order to ensure that the I_{EFF} extracted from the simple RC method resembles the actual current flowing through the pull-down transistor the real time drive current trajectory of the TFET is analyzed in greater detail. Figure 3-8 (a) and (b) show the real time drive current trajectory for Si and InAs TFET inverters superimposed on its DC I_{DS} - V_{DS} characteristics. Critical differences are seen in the switching current trajectories for the Si and InAs TFETs originating from the marked differences in the amount of the output voltage overshoot due to the capacitive feed forward effect. For Si TFET inverter, as the input voltage ramps to V_{DD} , the drain voltage of the n-TFET swings to V_{MAX} due the capacitive feed forward miller effect, forcing it into deep saturation. It is noted that the saturation current, I_{ON} at $V_{GS}=1$ V and $V_{DS}=1$ V, discharges the the entire drain overshoot voltage in Si TFETs. In contrast, for InAs TFET inverter, due to the lower overshoot voltage and high ON-current, the output drain voltage starts transitioning from V_{DD} before the input gate voltage reaches V_{DD} . Thus, the peak current never reaches the saturation current, I_{ON} , during switching. In MOSFETs often a 2-pt average [58] is used to approximate the effective drive current trajectory as $(I_H+I_L)/2$ where I_H (high current) is the drain current at $V_{GS}=V_{DD}=1$ V and $V_{DS}=V_{DD}/2=0.5$ V and I_L (low Current) is the drain current at $V_{GS}=V_{DD}/2=0.5$ V and $V_{DS}=V_{DD}=1$ V. It has been further shown that this 2-pt average is no longer adequate in predicting the effective drive current for non-traditionally scaled Si MOSFETs (with low threshold voltage, V_T) and novel devices like carbon nanotube FETs (CNFET) [58]. Likewise, due to the large overshoot in the transient response of Si TFETs a simple 2-pt model is inadequate and a 3 pt model is required to closely predict the average current flowing through the switching transistor. We propose the following general 3-pt model for Si and InAs TFETs taking into consideration the overshoot effects in the actual current trajectory:

$$I_{EFF} = \frac{I_L + I_P + I_H}{3} \quad (4)$$

where I_H and I_L have the same definitions as above while I_P is the peak current in the real time switching current trajectory. For Si TFETs I_P occurs at $V_{GS}=V_{DS}=1$ i.e. at $V_{GS}=V_{DS}=V_{DD}$ which is the saturation current (I_{ON}) while for InAs TFETs I_P is at $V_{GS}=V_{DS}=0.17$ V i.e. at $V_{GS}=V_{DS}=0.7V_{DD}$ and is significantly lower than its I_{ON} at $V_{GS}=V_{DS}=V_{DD}=0.25$ V. As can be seen in figure 3-8 this 3-pt average along the drive current trajectory approximates the effective current calculated using the simple RC model in equation (2) and (3) to within 8% for Si TFETs and to within 1% for InAs TFETs. A 2-pt model leads to errors greater than 10% for both InAs and Si TFET inverters. It is worth noting in figure 3-8 that the 3-pt average computed from equation (4) brings the I_{EFF} close to I_H but it is more physical to use a 3-pt average than a single point since it more closely tracks the actual switching current trajectory in the inverter.

In summary, we have shown a simple way to extract the effective output capacitance and effective switching current for an unloaded inverter from the y-intercept and the slope of the fall delay vs. load capacitance plot. It is shown that the effective output capacitance (C_{EFF}) of the unloaded TFET inverter is 2.6 times the gate capacitance, C_{gg} , due to the miller effect unlike mosfets where it is approximately equal to the gate capacitance (C_{gg}). The I_{EFF} extracted from the switching resistance, R_{sw} , reflected by the slope of the delay vs. load capacitance plot can be approximated by a 3-pt average of the actual switching current trajectory for Si and InAs TFET inverters to within 8% and 1% accuracy. The $C_{EFF} = 2.6 \times C_{gg}$ and $I_{EFF} = 0.33 \times (I_L + I_H + I_P)$ thus extracted from the capacitance-voltage and the output I-V characteristics of TFET at the device level can provide a more accurate prediction of its circuit level performance.

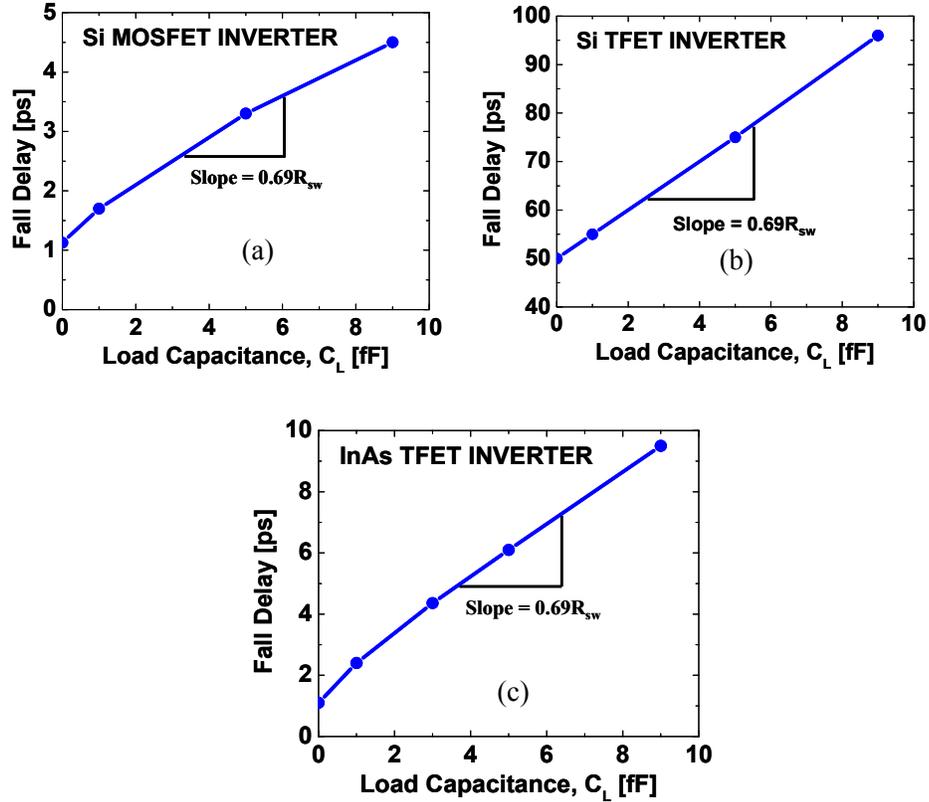


Figure 3-6 Fall time delay (τ_f) as a function of load capacitance, C_L , for (a) Si MOSFET inverter and (b) Si TFET and (c) InAs TFET inverter. Fall time delay is measured as the time interval between 50% of input (V_{in}) and 50% of output (V_{out}) voltage of the inverter in figure 3-3.

Table 3-3: Switching Resistance (R_{sw}), effective switching current (I_{EFF}) and output capacitance (C_{EFF}) extracted from figure 3-6 using the simple RC model defined in equation (1) and (2).

Inverter	Switching Resistance, R_{sw}	Effective switching current, I_{EFF}	Effective output capacitance, C_{EFF}
Si MOSFET	0.5 K Ω	0.93 mA	0.9 C_{gg}
Si TFET	7.4 K Ω	68 μ A	2.6 C_{gg}
InAs TFET	1.3 K Ω	97 μ A	2.6 C_{gg}

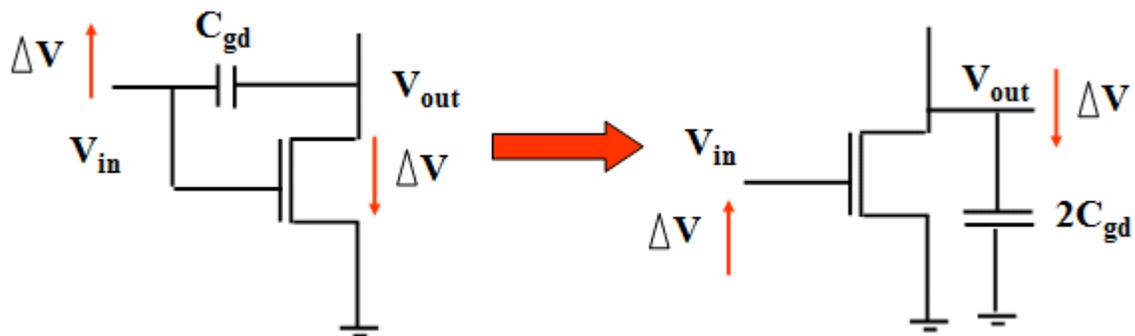
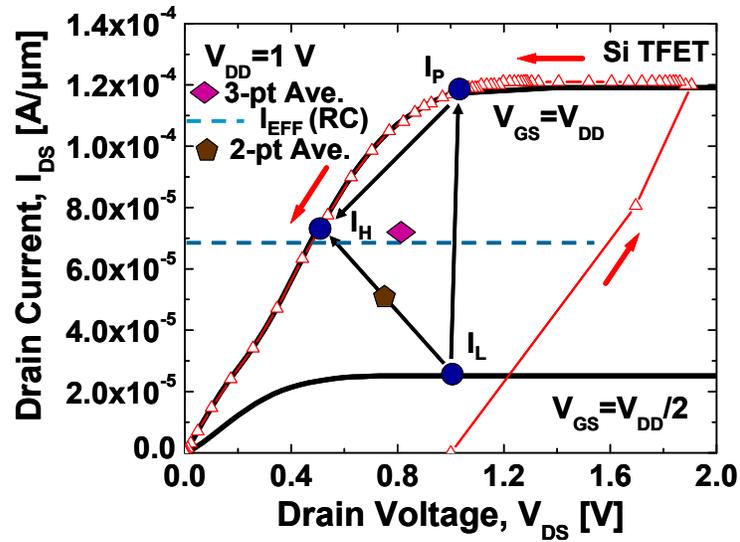
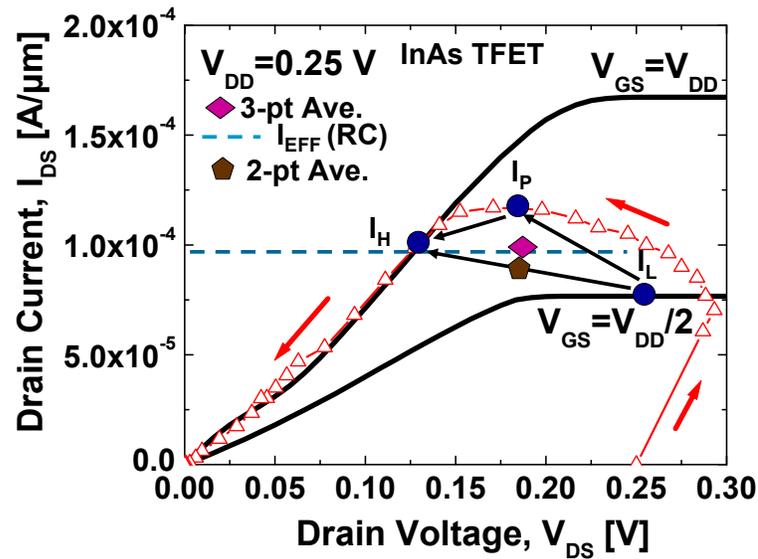


Figure 3-7. A capacitor experiencing identical but opposite voltage swing at both its terminal can be replaced by a capacitance to ground whose value is two times the original value. This is called the Miller effect. Due to this Miller effect the gate-to-drain capacitance contribution towards the effective output capacitance is doubled.



(a)



(b)

Figure 3-8. Real time drive current trajectory in the n-type TFET during inverter switching (Triangles) superimposed on its DC I_{DS} - V_{DS} (black line) characteristics at $V_{GS} = V_{DD}$ and $V_{DD}/2$ for (a) Si TFET and (b) InAs TFET inverter. I_L , I_P and I_H are three points along the current trajectory used to calculate the average switching current as defined in the text.

Chapter 4

TFET Fabrication and Characterization: Experiments

Section 4.1 presents the electrical characterization and fabrication details of homo-junction TFET. Based on temperature dependent electrical characterization of TFET, four uniquely different transport mechanisms have been identified giving key insight into its operating principle. In section 4.2 the fabrication and electrical characterization of a hetero-junction TFET is presented.

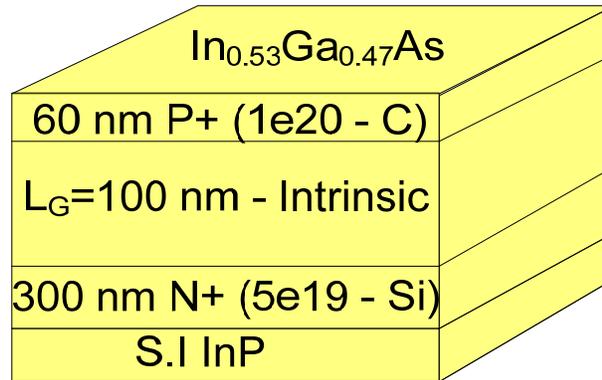
4.1 Homo-junction vertical TFET fabrication

This section will describe the fabrication of the first generation of tunnel transistors. We call this the first generation of transistors since this is neither surround gate and nor is it self-aligned. This section describes the fabrication of vertical $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ homo-junction tunnel transistor. Figure 4-1 shows schematically all the important process steps involved in the fabrication of the vertical TFET. This is followed by the detailed description of each process step. Figure 4-2 shows some of the important nuggets of process development. Figure 4-2(a) shows the excellent lift-off of the Ti/Pt/Au metal stack used for the source and drain metallization in TFET fabrication. Figure 4-2(b) shows the conformal deposition of the gate dielectric and metal on the (111) mesa sidewall etched on a dummy silicon wafer.

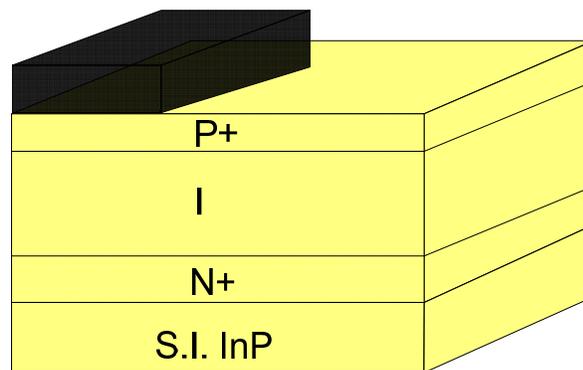
Figure 3-3 shows the mesa profile etched in $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and the conformal deposition of the gate dielectric and metal on the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ mesa sidewall. Figure 4-4 shows the SEM image of the fabricated $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ TFET clearly showing the gate air-bridge structure used to

gate the mesa sidewall. Details of the ALD (atomic layer deposition) dielectric deposition process is briefly described in section 4.1.2.

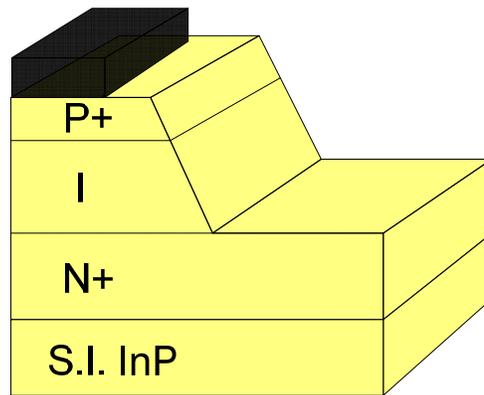
4.1.1 Fabrication process flow



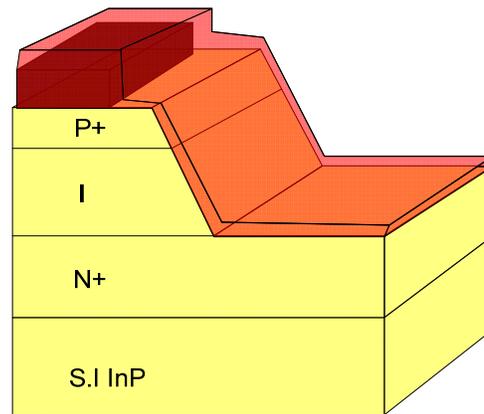
Step I: Layer structure. P^+ region is Carbon doped at $1\text{E}20 / \text{cm}^3$ while the N^+ region is silicon doped at $5\text{E}19 / \text{cm}^3$. This wafer is then thoroughly cleaned (Details described below)



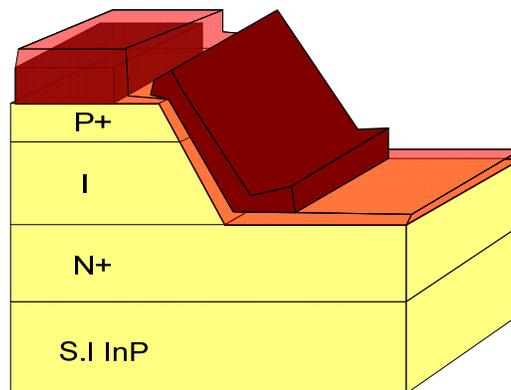
Step II: Source metal patterning (Ti/Pt/Au), evaporation and lift-off.



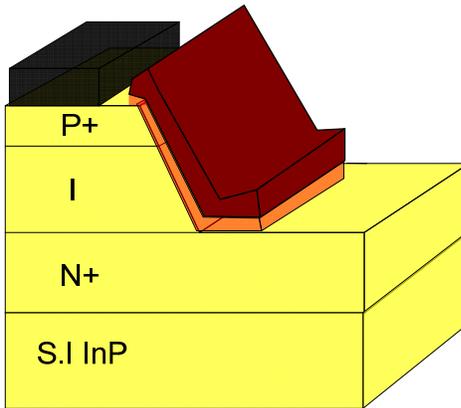
Step III: Mesa patterning and citric acid solution based preferential sidewall etching.



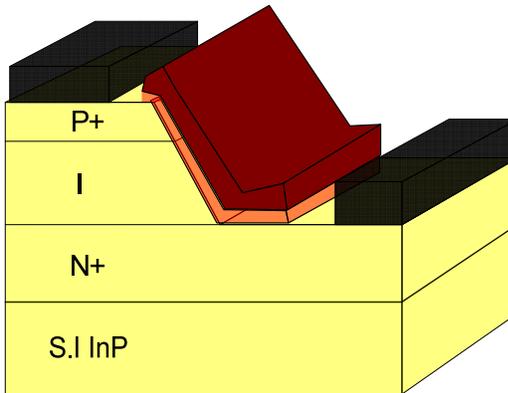
Step IV: Native oxide removal (29 %NH₄OH) followed by atomic layer deposition (ALD) of 10nm of alumina (Al₂O₃) at 300C.



Step V: Gate metal (Pt/Au) patterning, evaporation and lift-off.



Step VI: Wet etching of oxide (BOE (10:1) diluted 1:1 with DI water) from S/D regions



Step VII: Drain metal (Ti/Pt/Au) patterning, evaporation and Lift-off followed by isolation

Figure 4-1. Schematic of the various intermediate steps involved in the fabrication of homo-junction vertical TFET

Step I: Surface Cleaning

A. Degreasing:

- 10 min in partial boiling Acetone (Boiling point ~ 50C, Keep solution close to 30-40C).
- Soak for 10 min in partial boiling methanol (Boiling Point ~ 64.7C, Flash Point 11C, Heat Solution close to 30-40C)
- Soak for 5 min in IPA (Iso-Propyl Alcohol) at room temperature
- Rinse in DI water and blow dry with N₂

B. Native Oxide Removal:

- Soak in 29% NH₄OH for 3 min
- Rinse with DI water

Step II: Source metal patterning (Ti/Pt/Au), evaporation and lift-off

- Spin coat lift-off resist (LOR 5A) on the sample. D09.40.45 condition is used to spin coat the resist on the sample. See below for details of D09.40.45.
- Bake on hot plate at 175C for 10 min
- Cool sample for 1-2 min
- Spin coat shipley resist 3012 (SPR 3012) on the sample using the same condition of D09.40.45.
- Bake on hot plate at 95C for 1 min
- Cool sample for 1-2 min
- Expose the sample using the GCA i-line stepper
- Develop in CD-26 for 1.5 min. Rinse with DI water and blow dry with N₂ gun.
- Deposit Ti (20nm), Pt (20nm) and Au (100nm) using e-beam evaporation (Semicore)
- Soak in Remover PG heated to 60C for lift-off

Step III: Mesa patterning and citric acid solution based preferential sidewall etching

- Spin coat HMDS (adhesion layer)
- Bake on hot plate at 110C for 30 sec
- Spin coat shipley resist 3012 on the sample using the condition of D09.40.45.

- Bake on hot plate at 95C for 1 min
- Cool sample for 1-2 min
- Expose the sample using the GCA i-line stepper
- Develop in CD-26 for 1.5 min. Rinse with DI water and blow dry with N₂ gun.
- Dip in Citric acid solution for 4.5 min (to etch down to the n⁺ region) to etch the mesa sidewall preferentially along the (111) direction [59]. See below for details of how the citric acid solution was prepared.

D09.40.45: Dispense speed – 900 rpm for 15 sec, Ramp up speed – 2000 rpm for 5 sec, Casting speed – 4000 rpm for 45 sec, Ramp down speed – 100 rpm for 1 sec.

D09.20.60: Dispense speed – 500 rpm for 15 sec, Ramp up speed – 1000 rpm for 15 sec, Casting speed – 2000 rpm for 60 sec, Ramp down speed – 100 rpm for 1 sec (Used later)

Preparation of citric acid solution:

- Mix anhydrous citric acid with DI water in a ratio of 1:1 by weight. For this fabrication 200 ml of DI water was mixed with 200 gm of anhydrous citric acid. This solution was then stirred at 280 rpm for 45 min till it turned crystal clear. This solution was then left overnight.
- Next day, the above citric acid solution was mixed with hydrogen peroxide in a volume ratio of 20:1. This solution is manually stirred followed by a 15 min wait period before the sample is etched. (In_{0.53}Ga_{0.47}As etch rate ~ 1 nm/sec)

Step IV: Native oxide removal and ALD alumina deposition

- Soak in 29% NH₄OH for 3 min [60].
- Rinse with DI water and blow dry with N₂ gun.
- Immediately load sample into the Cambridge savannah ALD chamber. Deposit Al₂O₃ at 300C (100 cycles). Each ALD cycle comprises of (i) 15 ms pulse of DI water (ii) wait period – 3s (iii) 15 ms pulse of TMA (Tri Methyl Aluminum) (iv) wait period – 3s. Deposition rate – 1Å/cycle.

Step V: Gate metal patterning and lift-off

- Spin coat lift-off resist (LOR 5A) on the sample. D09.40.45 condition is used to spin coat the resist on the sample.
- Bake on hot plate at 175C for 10 min
- Cool sample for 1-2 min
- Spin coat shipley resist 3012 on the sample using the same condition of D09.40.45.
- Bake on hot plate at 95C for 1 min
- Cool sample for 1-2 min
- Expose the sample using the GCA i-line stepper
- Develop in CD-26 for 1.5 min. Rinse with DI water and blow dry with N₂ gun.
- Deposit Pt (20nm) and Au (100nm) using e-beam evaporation (Semicore)
- Soak in Remover PG heated to 60C for lift-off

Step VI: Wet etching of oxide from S/D regions

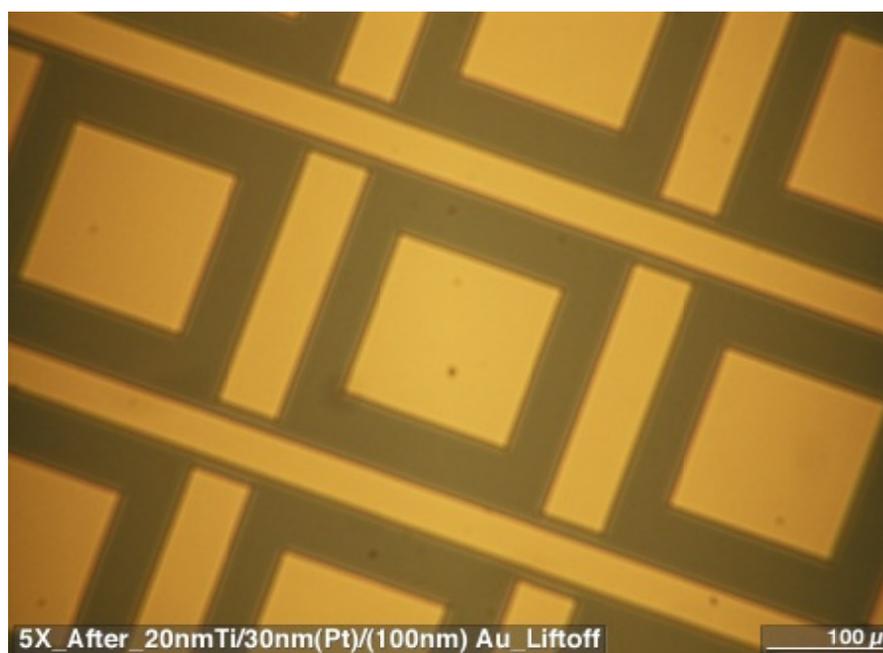
- Spin coat HMDS (adhesion layer)
- Bake on hot plate at 110C for 30 sec
- Spin coat shipley resist 3012 on the sample using the condition of D09.40.45.
- Bake on hot plate at 95C for 1 min.
- Cool sample for 1-2 min.
- Expose the sample using the GCA i-line stepper.
- Develop in CD-26 for 1.5 min. Rinse with DI water and blow dry with N₂ gun.
- Dip in 1:1 (10:1) BOE:DI water solution for 10 sec to etch oxide from the S/D regions.
- Rinse with DI water and soak in remover PG to strip resist.

Step VII: Drain metal (Ti/Pt/Au) patterning, evaporation and Lift-off

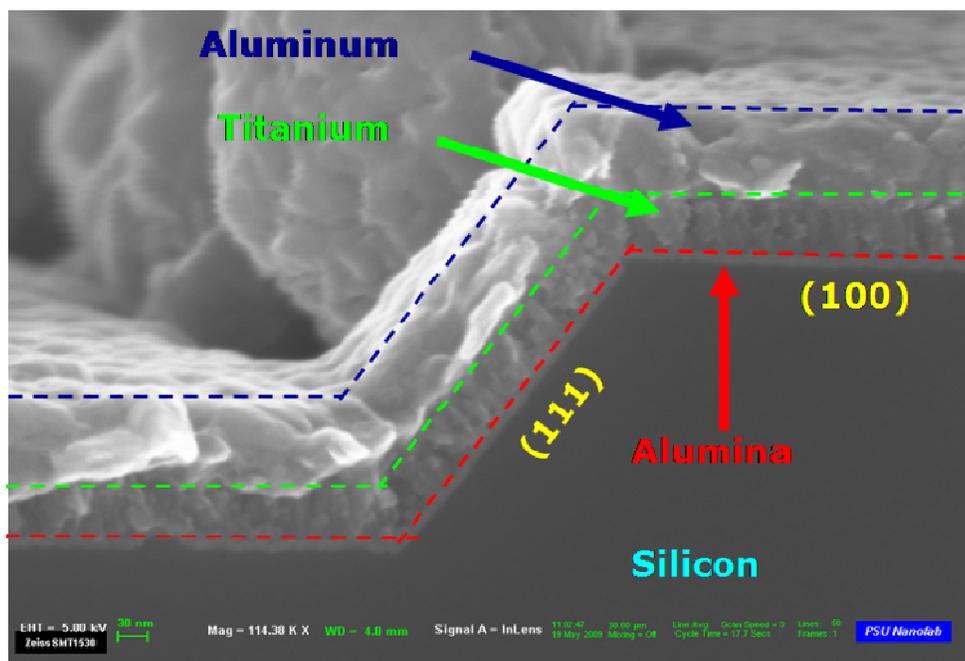
- Spin coat lift-off resist (LOR 5A) on the sample. D09.40.45 condition is used to spin coat the resist on the sample. See below for details of D09.40.45.
- Bake on hot plate at 175C for 10 min
- Cool sample for 1-2 min
- Spin coat shipley resist 3012 on the sample using the same condition of D09.40.45.
- Bake on hot plate at 95C for 1 min
- Cool sample for 1-2 min
- Expose the sample using the GCA i-line stepper
- Develop in CD-26 for 1.5 min. Rinse with DI water and blow dry with N₂ gun.
- Deposit Ti (20nm), Pt (20nm) and Au (100nm) using e-beam evaporation (Semicore)
- Soak in Remover PG heated to 60C for lift-off

Step VIII: Device Isolation

- Spin coat HMDS (adhesion layer)
- Bake on hot plate at 110C for 30 sec
- Spin coat shipley resist 3012 on the sample using the condition of D09.40.45.
- Bake on hot plate at 95C for 1 min.
- Cool sample for 1-2 min.
- Expose the sample using the GCA i-line stepper.
- Develop in CD-26 for 1.5 min. Rinse with DI water and blow dry with N₂ gun.
- Dip in Citric acid solution for 10 min (to etch down to the n⁺ region) to etch all the way down to InP.
- Rinse with DI water and blow dry with N₂ gun.



(a)



(b)

Figure 4-2. (a) Optical image of Ti/Pt/Au metallization on silicon showing its clean lift-off (b) Cross-sectional SEM (scanning electron microscope) image of (111) sidewall etched in dummy silicon (sample cleaved along [110] direction) wafer to check the conformality of the gate oxide and metal on the mesa sidewall. This was then replicated on $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$.

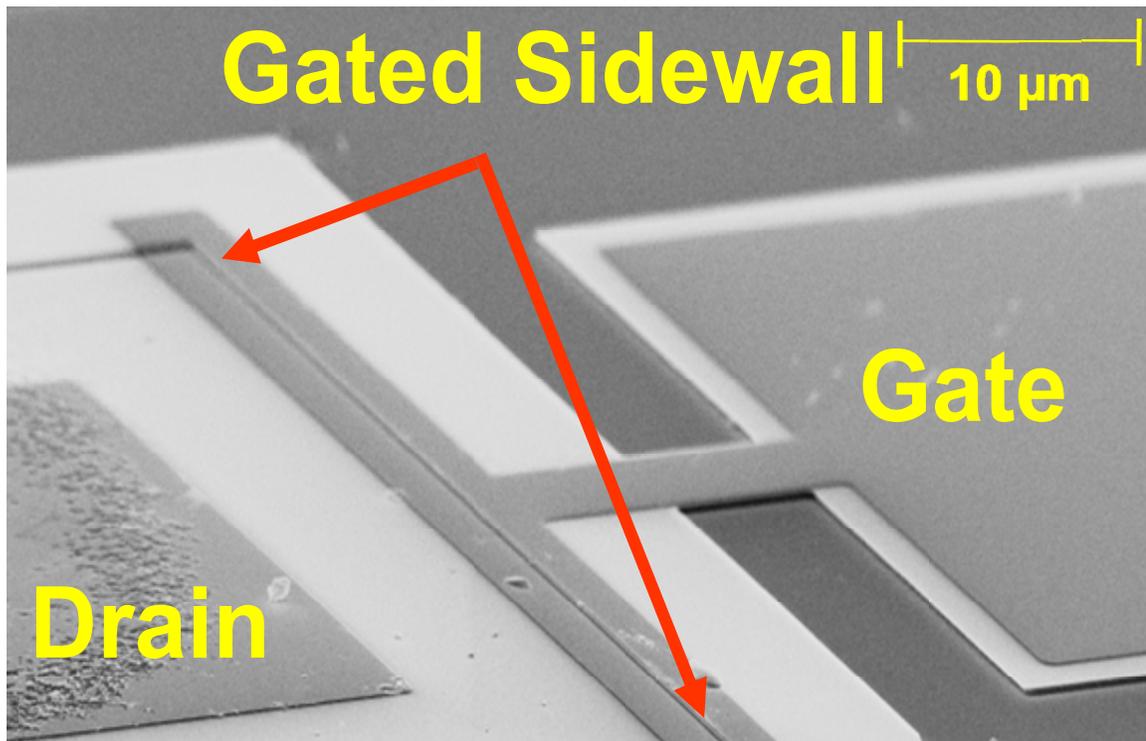
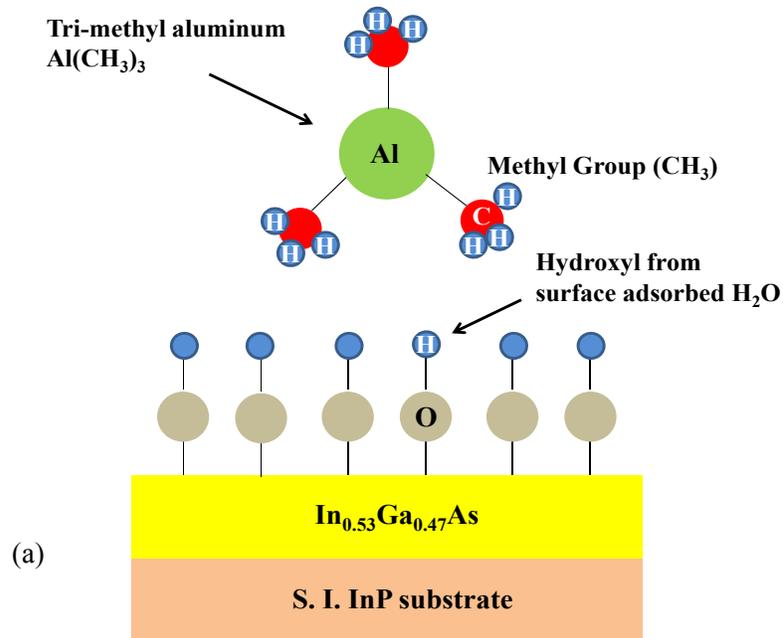


Figure 4-4. Tilted view SEM image of the fabricated homo-junction $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ TFET showing the gate air-bridge structure used to gate the mesa sidewall. The source metal is at the bottom (Not visible in the SEM image)

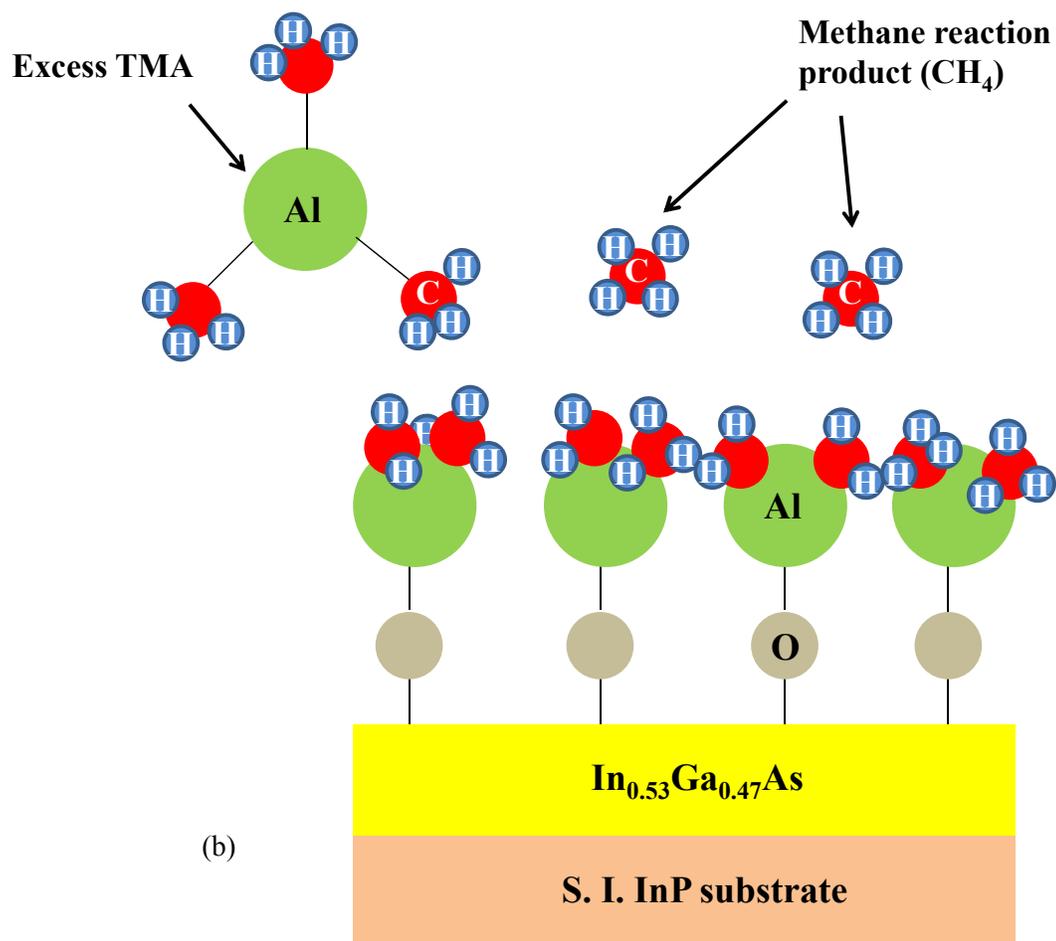
4.1.2 Atomic layer deposition (ALD)

In the vertical TFET fabrication process flow described above the gate dielectric is deposited via an atomic layer deposition (ALD) process. In this section we will look at the operating principle of ALD. The defining characteristics of ALD are (i) self-limiting atomic layer-by-layer growth and (ii) highly conformal coating.

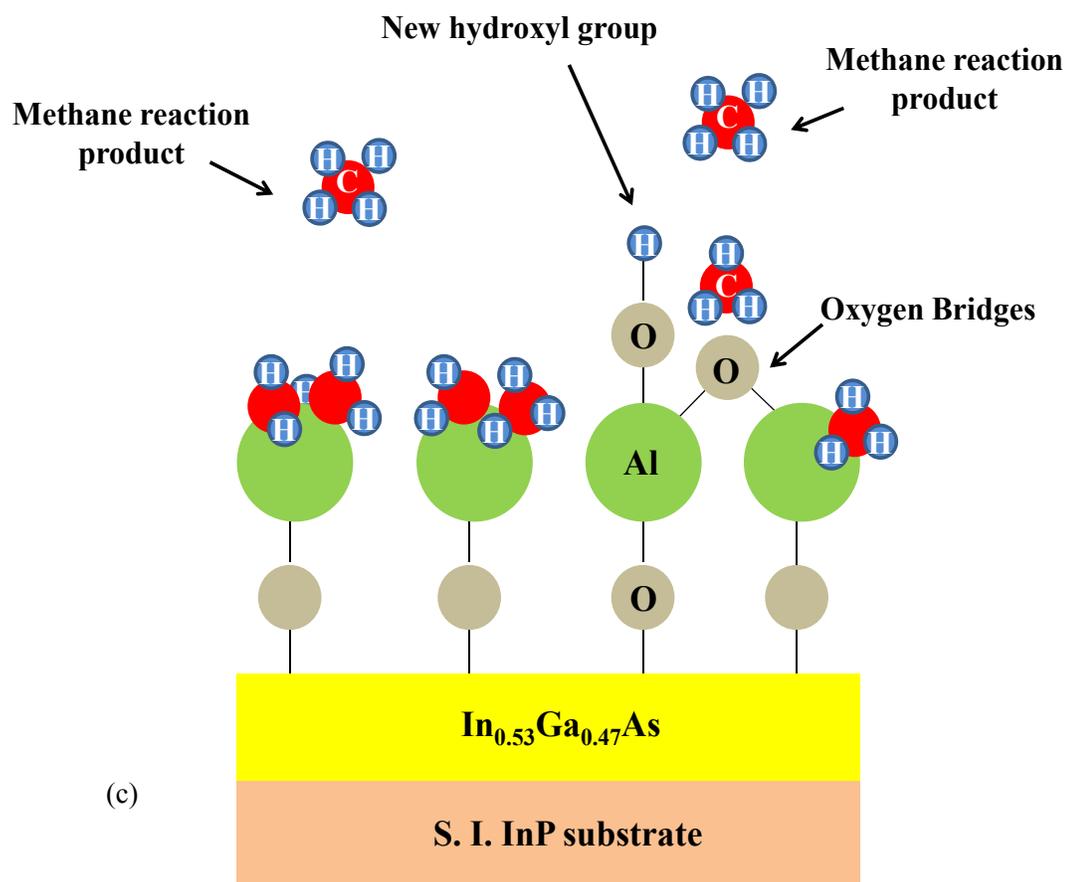
ALD involves sequential pulsing of chemical precursors, all of which together form one atomic layer and makes up one cycle. This results in pin-hole free conformal coating in deep pores, trenches and cavities. Figure 4-5 [61] below shows schematically the deposition of 1 cycle of Al_2O_3 .



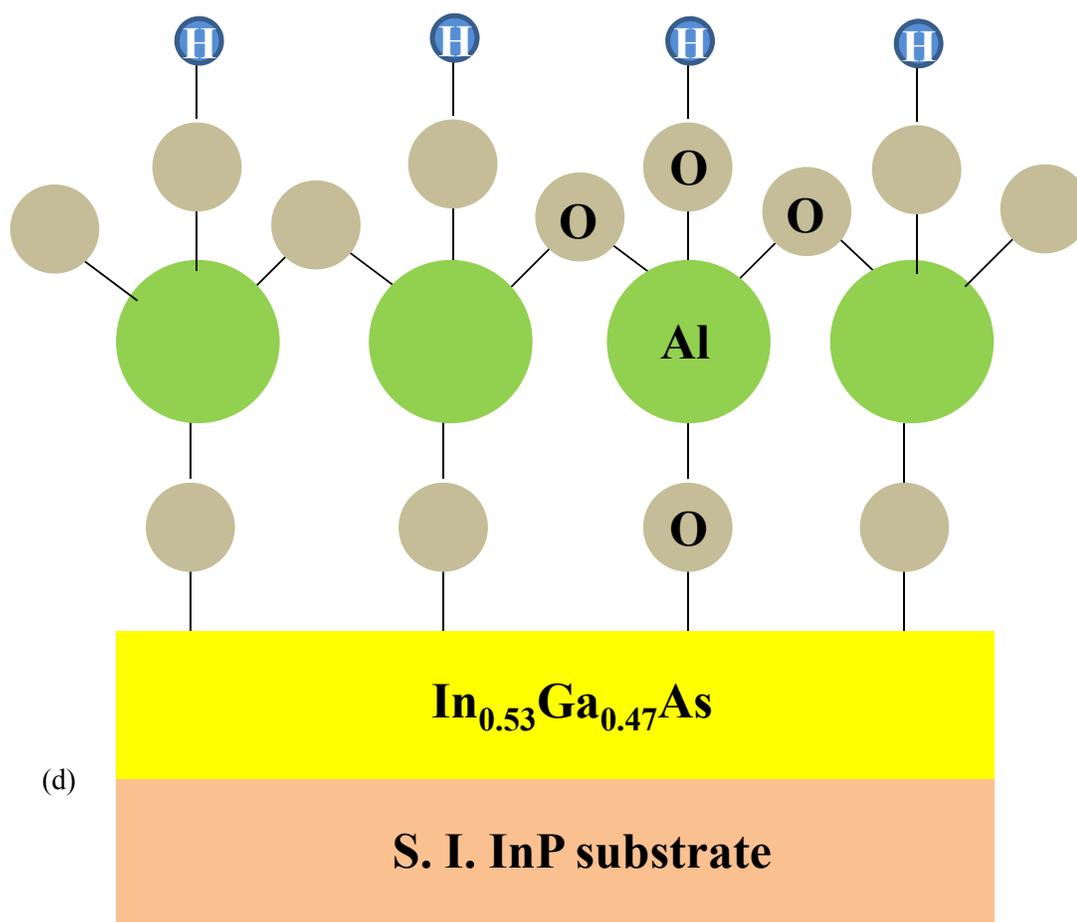
The sample is placed into the chamber at given temperature and water is pulsed causing hydroxyl groups to adsorb on the surface. This is followed by a TMA (Tri-Methyl Aluminum) pulse as shown in the above image.



Tri-methyl Aluminum (TMA) reacts with the adsorbed hydroxyl groups, producing methane as the reaction product. This continues until the surface is passivated. TMA does not react with itself, terminating the reaction to one layer. This causes the perfect uniformity of ALD. The excess TMA is pumped away with the methane reaction product.



After the TMA and methane reaction product is pumped away, water vapor (H_2O) is pulsed into the reaction chamber. H_2O reacts with the dangling methyl groups on the new surface forming aluminum-oxygen (Al-O) bridges and hydroxyl surface groups, waiting for a new TMA pulse. Again methane is the reaction product.



The reaction product methane is pumped away. Excess H₂O vapor does not react with the hydroxyl surface groups, again causing perfect passivation to one atomic layer. One TMA and one H₂O vapor pulse form one cycle

Figure 4-5. Chemical reaction involved during atomic layer deposition of 1 cycle of ALD Al₂O₃

4.1.3 Electrical characterization of homo-junction $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ TFET and its building blocks ($\text{P}^+\text{-I-N}^+$ diode and the semiconductor-dielectric interface)

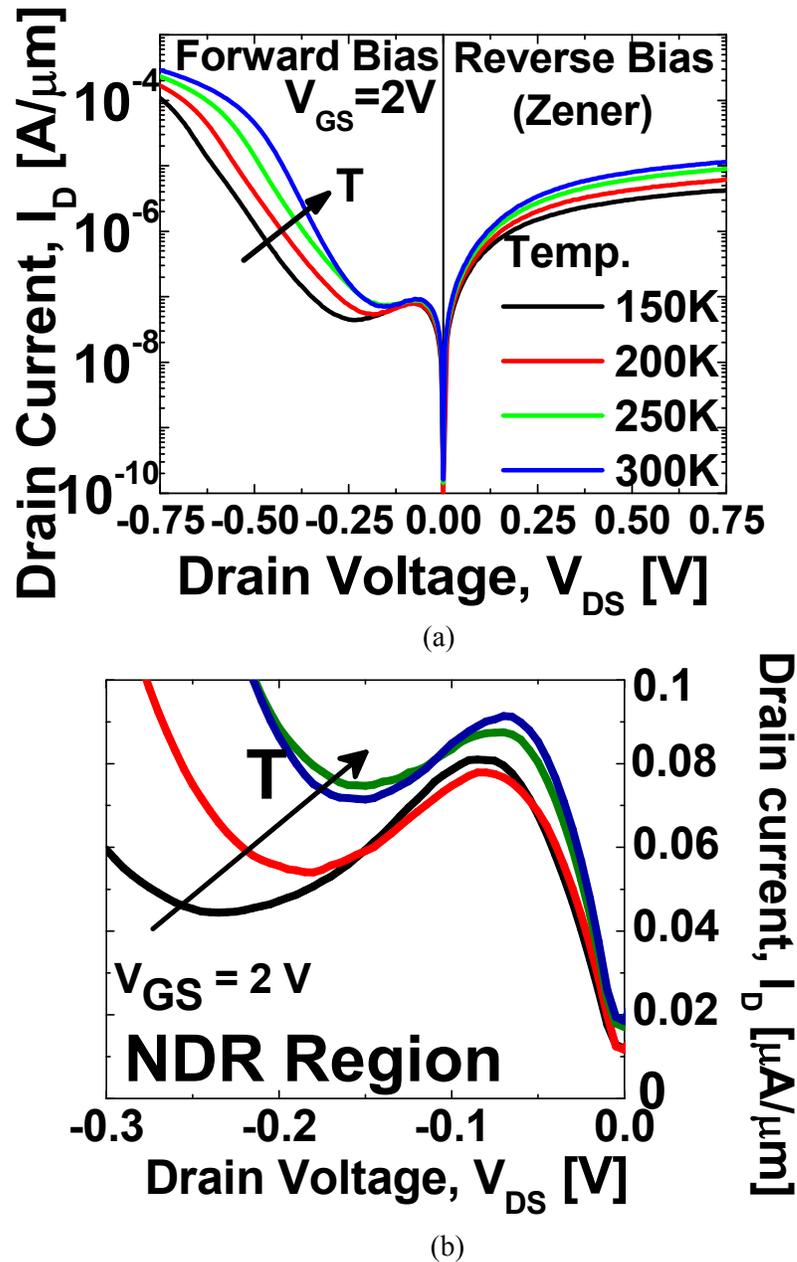
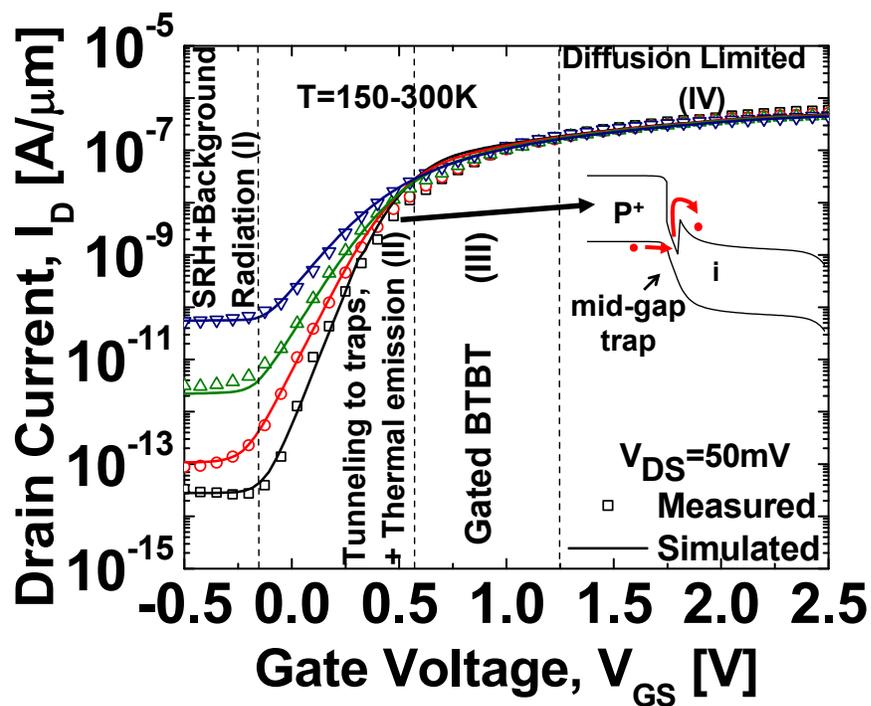


Figure 4-6. (a) Output characteristics (I_D - V_{DS}) of the fabricated vertical $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ TFET at $V_{GS}=2\text{V}$ for temperatures ranging from 150-300K. (b) Temperature dependence of NDR (Negative Differential Resistance) region in the forward bias region.

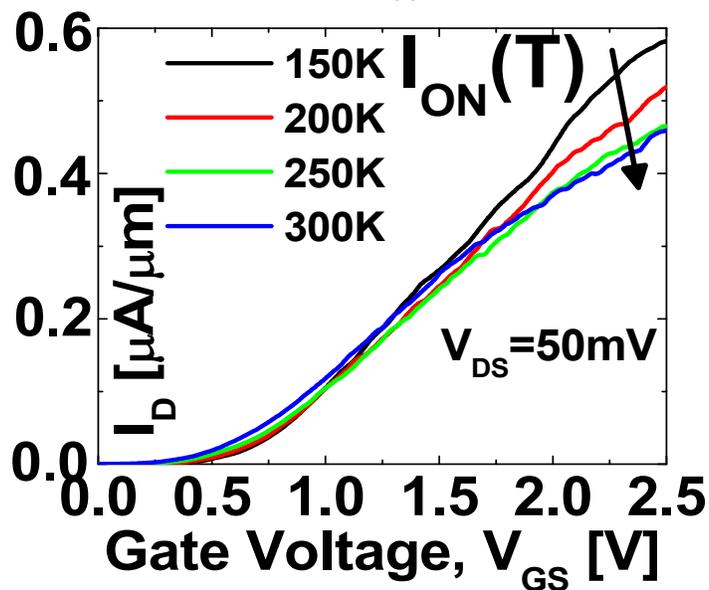
Figure 4-6(a) shows the output characteristics (I_D - V_{DS}) of the fabricated TFET for temperatures ranging from 150-300K at gate voltage, $V_{GS}=2V$. Gate modulated negative differential resistance (NDR) characteristics are visible in the forward bias regime (negative drain to source voltages) followed by regular diode turn on at more negative drain to source voltages. In the NDR region, the conduction occurs at the oxide- semiconductor interface via direct band-to-band tunneling from the conduction band in the channel to the valence band in the p+ source region. While the band to band tunneling current in the pre-NDR region shows very little temperature dependence, the valley current (Figure 4-6(b)) or the excess current is sensitive to the temperature, increasing with rise in temperature and suppressing the peak to valley current ratio. A maximum peak to valley ratio of 2 is obtained at 150K, which progressively degrades at higher temperatures. The origin of excess current is attributed to trap assisted tunneling at the oxide-semiconductor interface [62]. The diode turn-on at higher negative drain to source voltage shows a strong temperature dependence as expected for thermionic emission over the barrier. In the positive drain to source voltage region, the transport is related to reverse biased band to band tunneling (BTBT) and the temperature dependence of drain current arises due to band-gap reduction with rising temperature.

Figure 4-7(a) shows the measured transfer characteristics (I_D - V_{GS}) of the vertical $In_{0.53}Ga_{0.47}As$ TFET for temperatures ranging from 150 to 300K at $V_{DS} = 50$ mV. The temperature dependence of the transfer characteristics is a strong function of the gate bias indicating onset of various conduction mechanisms. Based on two dimensional numerical simulation with drift-diffusion transport, a non-local tunneling model [35][38] and physics based analytical modeling we identify 4 distinct regions of operation in the TFET transfer characteristics, as shown in figure 4-7(a).

In region I, the drain current is constant and shows no modulation with gate voltage. It sets the leakage floor (I_{OFF}) of the tunnel FET. I_{OFF} increases exponentially with rising temperature and is



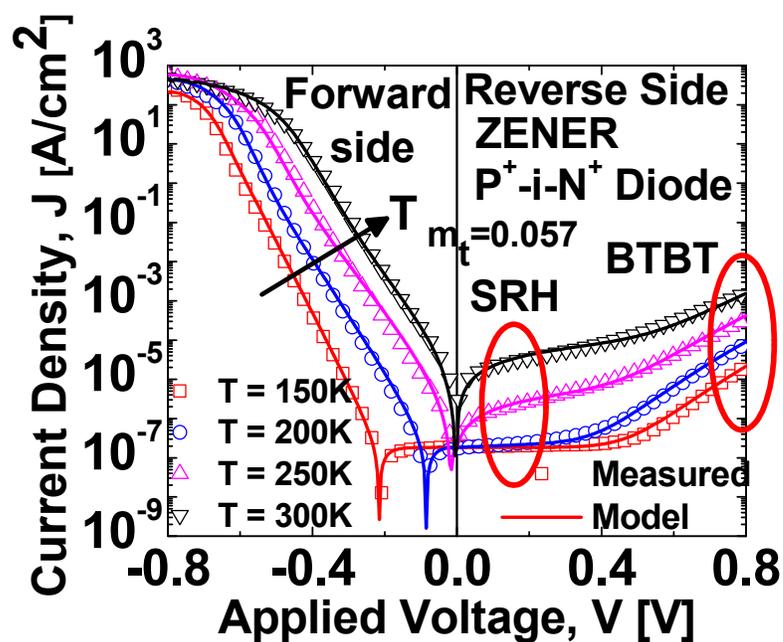
(a)



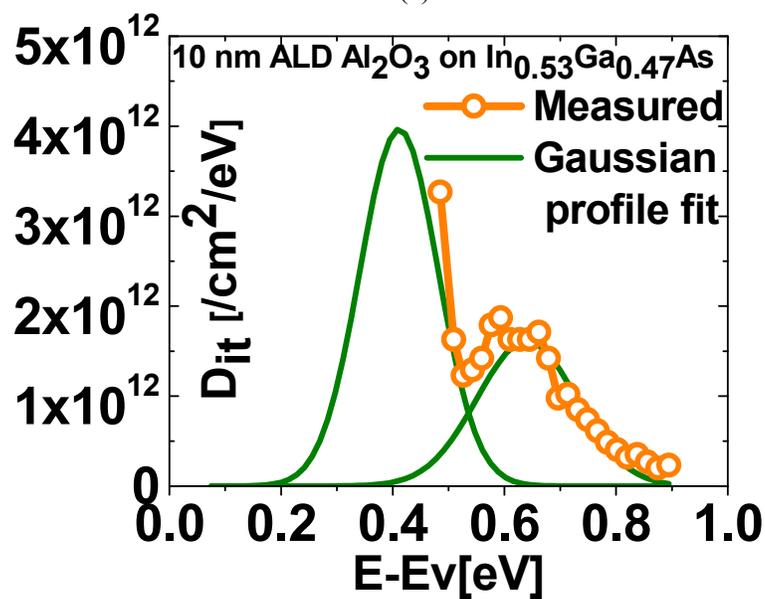
(b)

Figure 4-7. (a) Transfer (I_D - V_{GS}) characteristics of the fabricated TFET showing four regions with uniquely different temperature dependences. Each region identifies a distinct temperature dependent transport process (b) Transfer characteristics in linear scale showing the reduction in ON current with temperature in region IV.

determined by the SRH (Shockley-Read-Hall) generation-recombination current of the reverse biased $P^+ - I - N^+$ diode. The main contribution to the temperature dependence of this SRH dominated leakage floor arises from the intrinsic carrier concentration, n_i which is proportional to $\exp(-E_g/2kT)$ where E_g is the band-gap, k is the Boltzmann constant and T is the temperature. This is confirmed from the Arrhenius plot of figure 4-9(a) where an activation energy of 0.36 eV is extracted down to 200K consistent with half the band-gap of $In_{0.53}Ga_{0.47}As$. Below 200K the current is higher than that predicted by SRH and originates from the background thermal radiation effect [63]. The off current, I_{OFF} is proportional to the bulk $P^+ - I - N^+$ mesa area and, hence, the mesa area needs to be minimized to reduce the leakage floor in future ultra thin body TFETs. In region II, the drain current increases exponentially with gate voltage and represents the sub-threshold region of the transfer characteristics. The average sub-threshold slope (SS) is not $\text{sub-}kT/q$ or $\text{sub-}60 \text{ mV/dec}$ and progressively degrades from 100 mV/dec at 150K to 216 mV/dec at 300K. The strong positive temperature coefficient cannot be explained from the temperature dependence of band-gap alone and warrants a more careful investigation. We modeled the transport in this regime as a Poole-Frenkel (PF) mechanism [64] which involves field enhanced thermal excitation of carriers from the trap states located within the band-gap into the conduction band. Assuming PF transport mechanism, figure 4-9(b) extracts an effective thermal barrier height for trapped carriers, which turns out to be located at 0.4eV from the conduction band edge within the band-gap of $In_{0.53}Ga_{0.47}As$. For numerical simulation purpose, this is approximated as a potential well of depth 0.4eV immediately adjacent to the $P^+ In_{0.53}Ga_{0.47}As$ source region, as shown in the inset of figure 4-7(a). This notch in the conduction band edge profile is used to artificially simulate the effect of carriers tunneling into mid-gap trap states from the $P^+ In_{0.53}Ga_{0.47}As$ source region and their subsequent thermal emission into the conduction band, and is found to explain the experimental data quite well (figure 4-7(a)) at all temperatures. Thus, the physical transport mechanism in the sub-threshold region can be understood as tunneling of



(a)



(b)

Figure 4-8. (a) Un-gated $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ $\text{P}^+\text{-i-N}^+$ diode I-V characteristics (b) Extracted interface state density profile from n-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOSFET using split CV measurements.

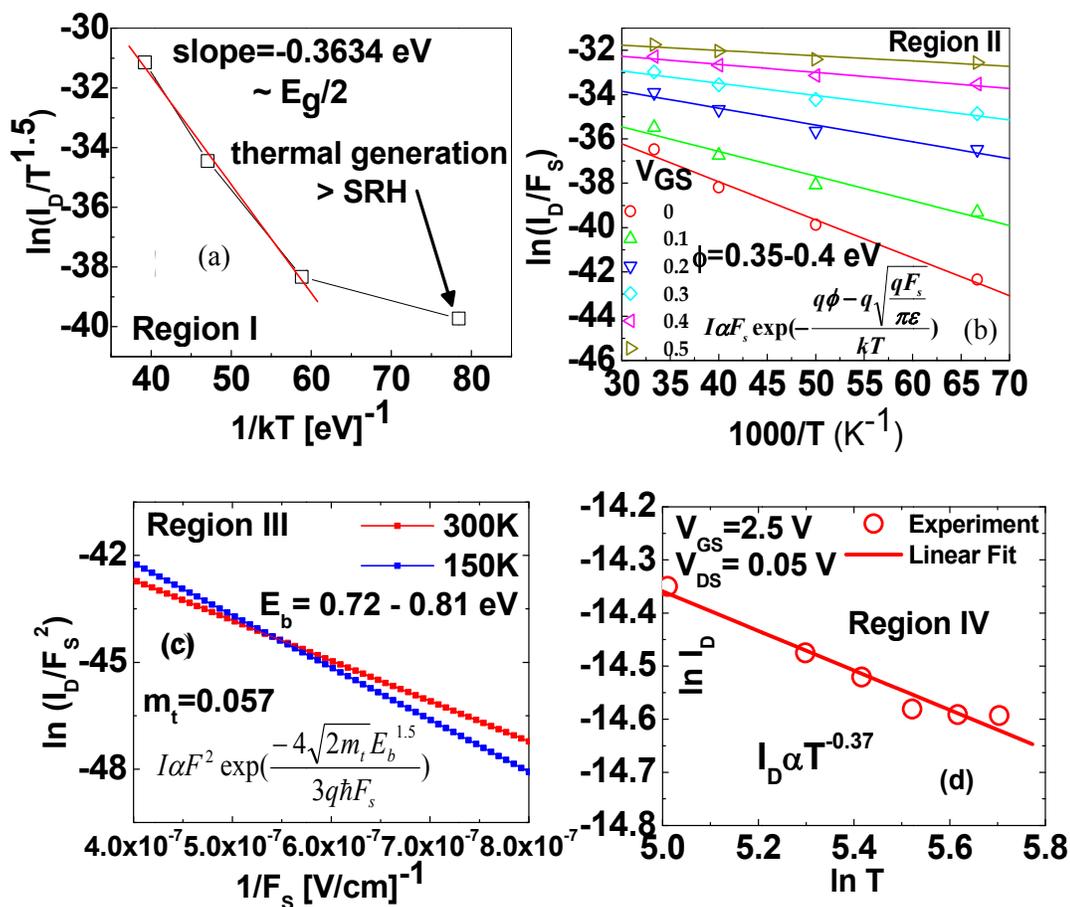


Figure 4-9. (a) An activation energy of $E_g/2$ extracted in region I confirms SRH generation-recombination current (b) A Poole-Frenkel barrier height extracted in region II highlights a dominant mid-gap trap (c) A direct band-to-band tunneling barrier height equal to the band gap in region III indicates negligible contribution from traps (d) In region IV the ON current exhibits negative temperature dependence ($\sim T^{-0.37}$), indicating a carrier diffusion limited transport in the channel.

carriers from the valence band in the P^+ source region to mid-gap traps and a subsequent thermal emission into the conduction band. It is this inherent thermal emission process that gives rise to the strong temperature dependence and dilution in sub-threshold slope.

To understand the origin and location (bulk v/s surface) of these mid-gap traps we fabricated and characterized ungated bulk P^+ -I- N^+ diode and N-type MOSFETs on $In_{0.53}Ga_{0.47}As$ with 10nm Al_2O_3 as the gate dielectric. The reverse biased bulk P^+ -I- N^+ diode characteristics shown in figure 4-8(a) could be explained by SRH generation- recombination currents at low voltages and BTBT at higher voltages with negligible contribution from mid-gap traps. On the other hand the interface state density extracted from admittance data obtained using split CV measurements [65] and shown in figure 4-8(b) clearly indicates a large interface state density peaking near the middle of the band-gap. This confirms the participation of mid-gap traps at the oxide semiconductor interface in the tunneling process causing a dilution in the sub-threshold slope and its strong temperature dependence. An improved surface passivation chemistry suppressing these dominant mid-gap traps will improve SS in future TFETs. In region III, the temperature sensitivity of drain current is weak indicating the presence of direct BTBT current. Figure 4-9(c) extracts an effective tunneling barrier height using Kane's direct BTBT model [19]. The barrier height E_b varies from 0.81eV at 150K to 0.72eV at 300K, which directly corresponds to the temperature variation of $In_{0.53}Ga_{0.47}As$ band-gap [66]. Here, the junction electric field, F_s , is extracted from the 2D numerical simulation of TFETs. In region IV, the TFET drain current dependence on temperature changes sign (Fig. 4-7(b)). Figure 4-9(d) plots the drain current, I_D , for different temperatures (T) showing a $T^{-0.37}$ dependence. Numerical simulation indicates that the lateral electric field in the TFET channel is very small causing the band to band tunneling generated carriers near the source to primarily diffuse through the channel towards the drain. This diffusion current can be expressed as $(kT/q) \times \mu \times dn/dx$ where μ is the electron mobility in the $In_{0.53}Ga_{0.47}As$ channel with a temperature (T) dependence of $T^{-1.5}$ due to LO phonon scattering

and dn/dx is the carrier concentration gradient in the channel. Thus the experimentally observed temperature dependence of $T^{-0.37}$ is close to the expected value of $T^{-0.5}$.

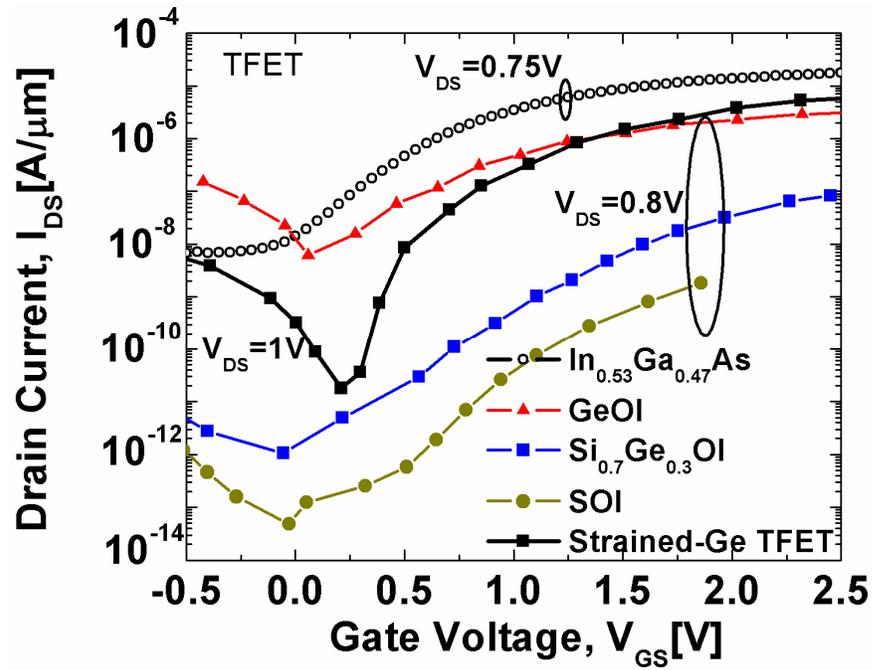


Figure 4-10. Measured 100nm L_G (gate length) $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ homo-junction TFET showing the highest drive current (I_{ON}) is benchmarked with Si , Ge , SiGe and strained- Ge TFET [32][33].

After understanding the transport mechanism in $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ homo-junction TFET it is worthwhile to compare its drive current (room temperature) with all the other TFETs that have been fabricated till date. Figure 4-10 compares the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ TFET drive current with all the other TFETs that have been fabricated till date. This homo-junction InGaAs TFET has the highest ON current that has been ever reported at $V_{D8}=0.75\text{V}$.

4.2 Hetero-junction TFET design and fabrication

The three most important issues that can be identified in the above homo-junction design are (i) The drive current is still low for high performance logic application (ii) The large $\text{p}^+\text{-i-n}^+$ mesa area results in large un-gated leakage current (I_{OFF}) and (iii) The dilution in sub-threshold slope arises from dominant mid-gap trap assisted tunneling. Each of the above issue has to be tackled independently in order to achieve high $I_{\text{ON}}/I_{\text{OFF}}$ ratio over a small supply voltage range.

Figure 4-11 shows the different schemes (band-gap engineering) that can be used to boost the ON current in TFET. Figure 4.11(a) is a homo-junction design with N^+ delta doped region sandwiched between the source-channel junction, figure 4.11(b) is a notched-gap TFET, figure 4.11(c) is a staggered gap system and figure 4.11(d) is a broken gap system. Each of these schemes reduce either/both the source-side tunneling barrier height and tunneling distance. The next sub-section will describe the design and fabrication of staggered band-gap based hetero-junction TFET.

Figure 4-12 depicts a novel device design to reduce the $\text{P}^+\text{-I-N}^+$ mesa area and hence the ungated reverse bias leakage current (I_{OFF}). In order to address the third major issue, passivation of the dielectric-semiconductor interface is explored via a combination of annealing and surface cleaning. Figure 4-13 shows the bulk $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ capacitance-voltage characteristics. In both

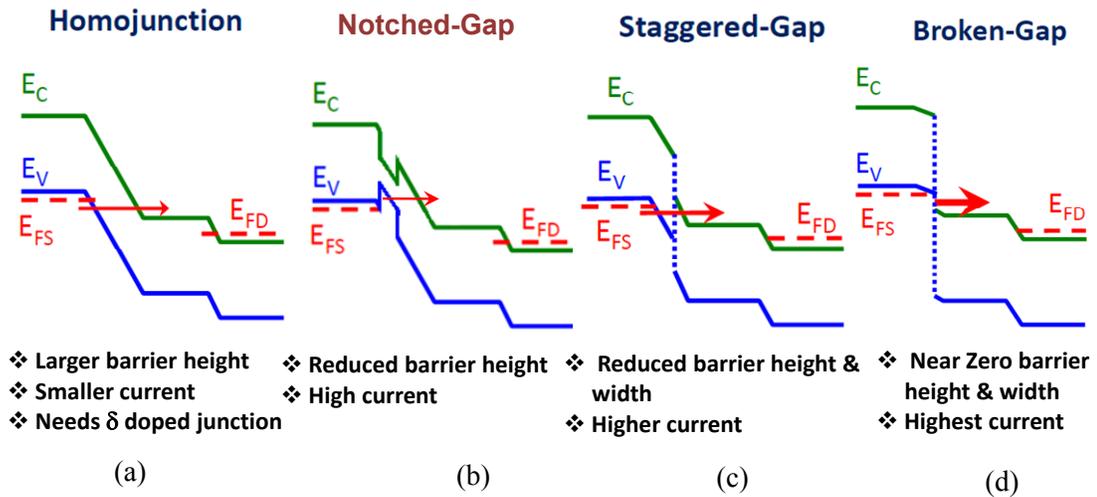


Figure 4-11. Different schemes to boost the I_{ON} (drive current) in TFET (a) Homo-junction TFET with delta-doped junction (b) Notched-gap TFET which involves a thin layer of low band-gap layer sandwiched between the source and channel junctions (Type -I band-alignment) (c) Staggered band-gap TFET (Type II band-alignment) and (d) Broken-gap TFET (Type III band-alignment).

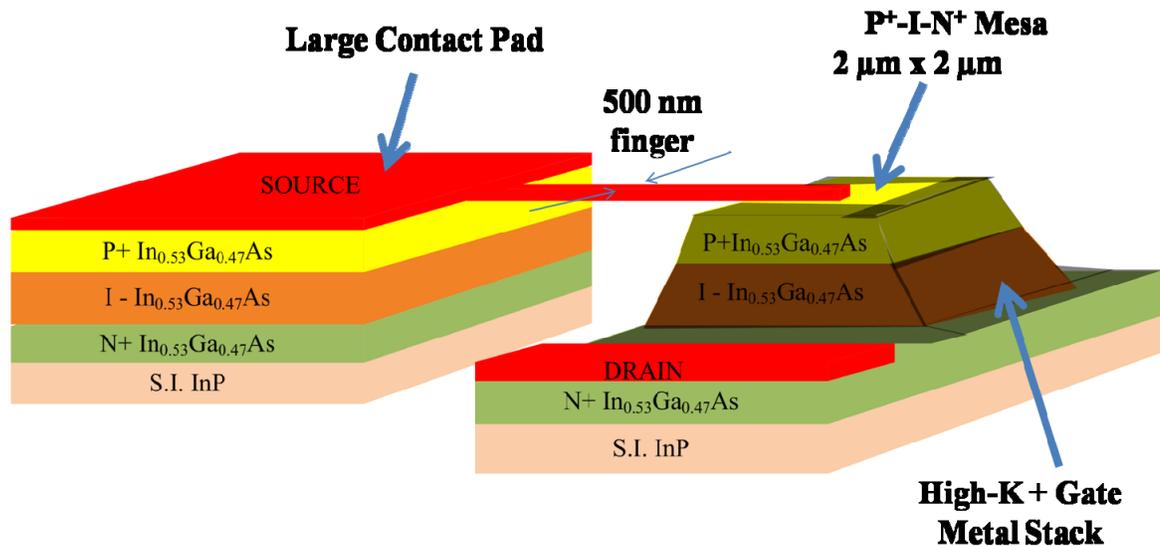


Figure 4-12. Proposed device schematic of the small mesa area TFET. A large pad with a small finger extension is used to contact the small mesa. This device also has a High-K + Gate metal stack.

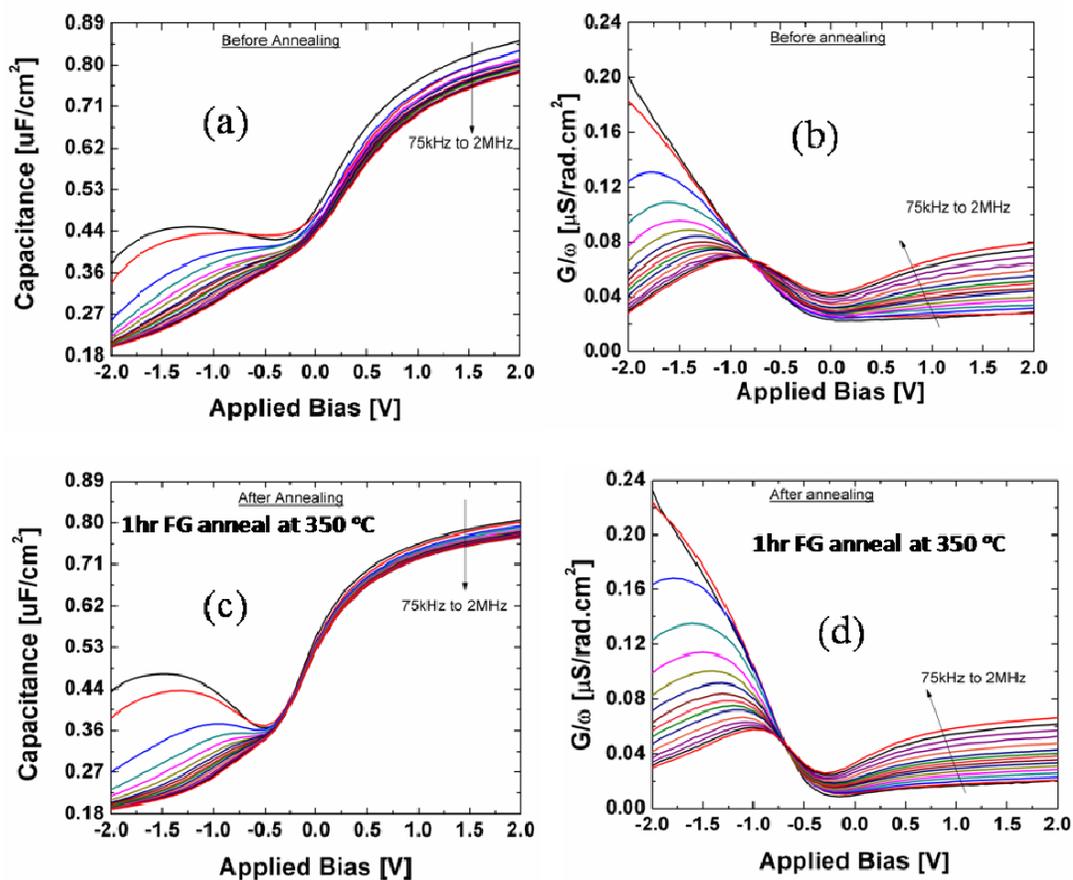


Figure 4-13. (a) Capacitance-Voltage characteristics before annealing (b) Conductance-Voltage characteristics before annealing (c) Capacitance-Voltage characteristics after forming gas (FG) annealing at 350C for 1 hour (d) Conductance-Voltage characteristics after FG annealing at 350C for 1 hour for (100) bulk $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitor with 5nm PE-ALD Al_2O_3 .

cases shown in figure 4-13 (with and without annealing) the native oxide is removed using 50:1 DI water: HF solution. Then the sample is annealed at 350C for 1 hour in forming gas [67].

It is clear from figure 4-13 that forming gas anneal reduces/passivates the traps close to the conduction band while the dominant mid-gap traps gets degraded. This can also be confirmed from the work of other researchers [68] who have seen that most commonly used semiconductor-dielectric interface passivation techniques only reduce the band-edge states while the mid-gap trap states remain unaffected. Therefore the origin of mid-gap traps seem to be much more fundamental and ways to suppress these traps need to be explored in greater detail.

Figure 4-14 shows the layer structure of the staggered band-gap system that is used for the fabrication of hetero-junction TFET.

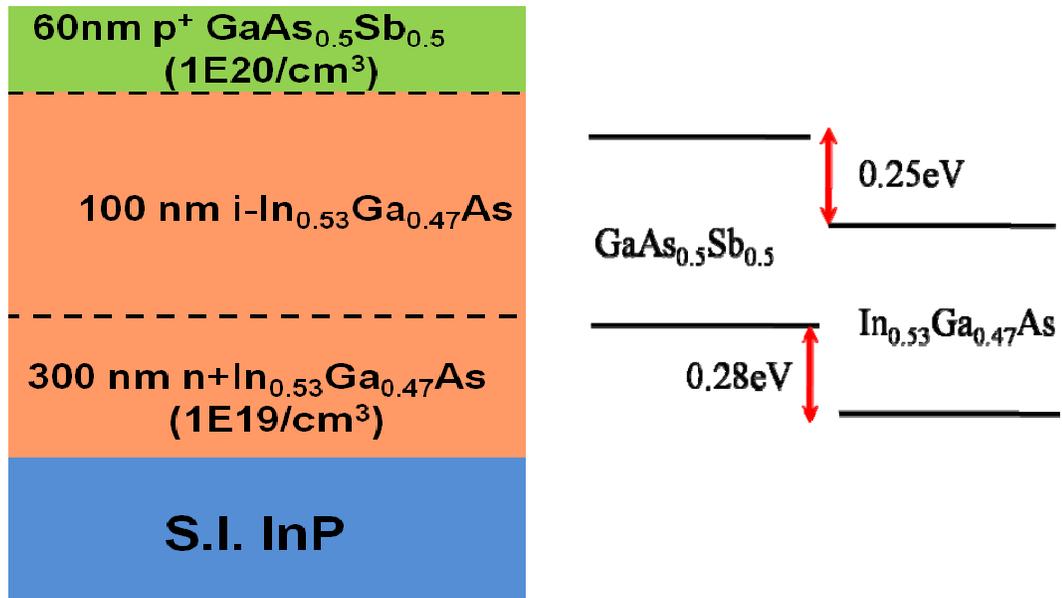


Figure 4-14. Layer structure to be used for the fabrication of hetero-junction TFET. The p⁺ source region is GaAs_{0.5}Sb_{0.5} while the channel (100nm intrinsic) and drain (n⁺) remain In_{0.53}Ga_{0.47}As. This is a lattice matched system. The conduction and valence band offset is also specified.

4.2.1 Hetero-junction TFET fabrication process flow

The process flow for hetero-junction TFET remains the same as the homo-junction TFET discussed earlier. The main difference is the use of e-beam lithography to define the source fingers and the small mesa area (figure 4-12). The details of the process flow are tabulated below.

Step I: Surface cleaning

A. Degreasing:

- 10 min in partial boiling Acetone (Boiling point ~ 50C, Keep Soln. Close to 30-40C)
- Soak for 5-10 min in boiling methanol (Boiling Point ~ 64.7C, Flash Point 11C, Heat Soln. Close to 30-40C)
- Soak for 5 min in IPA (Iso-Propyl Alcohol) at Room Temperature
- Rinse in DI water and blow dry with N₂

B. Native Oxide Removal:

- 1:50 HF:DI Water Dip for 30 sec
- Rinse with DI water

Step II: Source metal finger and pad definition

Sequence	Process	Material	Process Conditions
1.	E-beam Resist Coating (Bi-layer)	1. P(MMA-MAA) 8.5 Co-Polymer diluted with 5.5% Ethyl Lactate (EL) 2. PMMA (A3)	1.a Use D09.20.60 (~ 250 nm) 1.b Bake: 150C – 3 min 1.c Cool: 1-2 min 2.a Use D09.40.45 (100-120nm) 2.b Bake 180C – 3min 2.c Cool: 1-2 min
2.	Semicore Thermal Evaporation	10 nm Au film evaporation (Thermal Evaporation Only)	Follow the Semicore/Kurt-Leskar User Manual
3.	E-beam Lithography	Follow the Procedure for using the e-beam tool (No Alignment Needed since this is the first layer) • Create Separate .IWFL files for fingers and pads.	Dose - 700 $\mu\text{C}/\text{cm}^2$ (Fingers) Resolution = 10 nm (Beam size = 15nm, current - select from spot table) Dose - 280 $\mu\text{C}/\text{cm}^2$ (Pads) Resolution = 150 nm (Beam size = 180nm, current - select from spot table) Beam diameter should be 20% higher than resolution High Tension = 100kV
4.	Wet Etch Top Au Layer	Transcene Au Etchant - TFA	a. Dip for 30 sec b. Rinse with DI Water and dry

			with N ₂ gun
5.	Develop E-beam Resist	Develop the PMMA/MMA Bi-layer Resist	1. 1:1 MIBK: IPA – Dip for 1 min. 2. IPA – Dip for 15 sec 3. DI water Rinse (Check under Optical Microscope)
6.	Oxygen Discum	1.Oxygen Plasma RIE to remove remnant resist scum 2.Post RIE native oxide removal	1. Time: 20s, O ₂ – 45 sccm, Pressure- 100mTorr, Power – 100W (Plasma-Therm) 2. (1:50) HCl : DI water dip – 15 sec 3.Rinse in DI Water (Immediately Load Sample in Semicore for Metal Dep.)
7.	E-beam Evaporation (Semicore) and Lift-off	1.Ti/Pd/Au (20/20/60nm) metal stack 2. Lift-Off	1. Deposit Ti and Pd at 1.5A° /s and Au in three steps of 20 nm at 1.5A°/s. After each step allow sample cooling – 20 min 2. Dip in Remover PG – overnight if required. Heating Soln. to 60C might help.

Step III: Mesa patterning and etching

Sequence	Process	Material	Process Conditions
1.	E-beam Resist Coating (Bi-layer)	1. P(MMA-MAA) 8.5 Co-Polymer diluted with 5.5% Ethyl Lactate (EL) 2. PMMA (A3)	1.a Use D09.20.60 (~ 250 nm) 1.b Bake: 150C – 3 min 1.c Cool: 1-2 min 2.a Use D09.40.45 (100-120nm) 2.b Bake 180C – 3min 2.c Cool: 1-2 min
2.	Semicore Thermal Evaporation	10 nm Au film evaporation (Thermal Evaporation Only)	Follow the Semicore/Kurt-Leskar User Manual
3.	E-beam Lithography	Follow the Procedure for using the e-beam tool (Align to 1 st layer) • Create Separate .IWFL files for small and big mesa.	Dose - 320 $\mu\text{C}/\text{cm}^2$ (small area) Resolution = 10 nm (Beam size = 15nm, current - select from spot table) Dose - 320 $\mu\text{C}/\text{cm}^2$ (big area) Resolution = 150 nm (Beam size = 180nm, current - select from spot table) Beam diameter should be 20% higher than resolution High Tension = 100kV
4.	Wet Etch Top Au Layer	Transcene Au Etchant - TFA	a. Dip for 30 sec b. Rinse with DI Water and dry

			with N ₂ gun
5.	Develop E-beam Resist	Develop the PMMA/MMA Bi-layer Resist	1. 1:1 MIBK: IPA – Dip for 1 min. 2. IPA – Dip for 15 sec 3. DI water Rinse (Check under Optical Microscope)
6.	Mesa patterning	Reactive Ion Etching BCl ₃ /Ar based gas chemistry	Pressure - 2mTorr, Gas flow – 15/60 sccm BCl ₃ /Ar, RF1-50W and RF2-75W, Room Temp., 9min timed etch @ 20nm/min (Versalock tool is used) [69]
7.	Strip resist	Bi-layer resist removal	Dip in Remover PG – overnight if required. Heating Soln. to 60C will help.

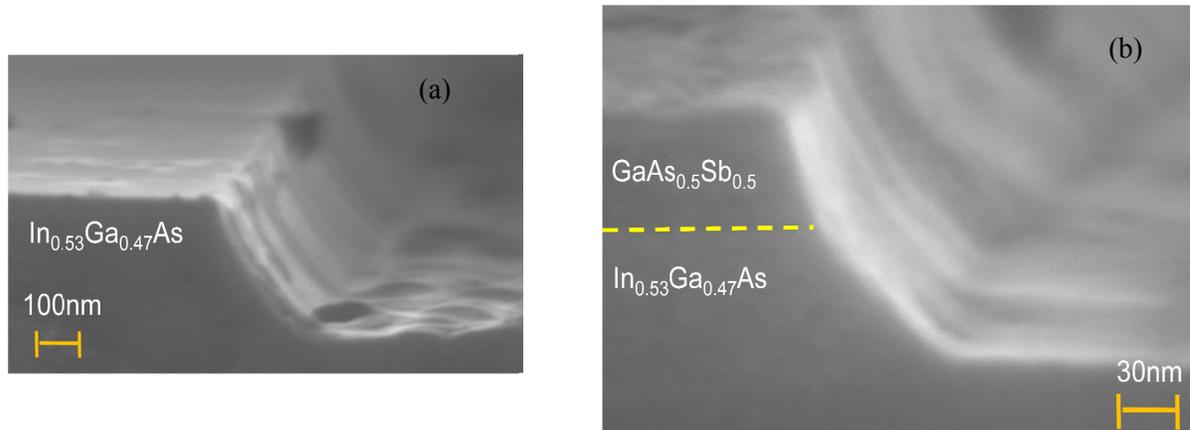


Figure 4-15. Mesa side-wall profile after (a) citric acid etch of homo-junction $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ (b) Reactive ion etch of the hetero-junction layer stack shown in figure 4-14. For comparison homo-junction TFET is also fabricated along with hetero-junction TFET with 5nm of Al_2O_3 as the high-K dielectric. The sidewall angle is large enough to ensure a conformal deposition of gate dielectric and metal.

Step IV: PE-ALD Al_2O_3 deposition

- Soak sample in 1:50 HF:DI Water for 30 sec
- Rinse with DI water
- Deposit 5 nm Al_2O_3 (This serves as the High-K dielectric)

Step V: Gate metal definition

Sequence	Process	Material	Process Conditions
1.	E-beam Resist Coating (Bi-layer)	1. P(MMA-MAA) 8.5 Co-Polymer diluted with 5.5% Ethyl Lactate (EL) 2. PMMA (A3)	1.a Use D09.20.60 (~ 250 nm) 1.b Bake: 150C – 3 min 1.c Cool: 1-2 min 2.a Use D09.40.45 (100-120nm) 2.b Bake 180C – 3min 2.c Cool: 1-2 min
2.	Semicore Thermal Evaporation	10 nm Au film evaporation (Thermal Evaporation Only)	Follow the Semicore/Kurt-Leskar User Manual
3.	E-beam Lithography	Follow the Procedure for using the e-beam tool (Align to 1 st layer)	Dose - 320 $\mu\text{C}/\text{cm}^2$ (Fingers) Resolution = 10 nm (Beam size = 15nm, current - select from spot table) Dose - 320 $\mu\text{C}/\text{cm}^2$ (Pads) Resolution = 150 nm (Beam size = 180nm, current - select from spot table) Beam diameter should be 20% higher than resolution High Tension = 100kV
4.	Wet Etch Top Au Layer	Transcene Au Etchant - TFA	a. Dip for 30 sec b. Rinse with DI Water and dry

			with N ₂ gun
5.	Develop E-beam Resist	Develop the PMMA/MMA Bi-layer Resist	<ol style="list-style-type: none"> 1. 1:1 MIBK: IPA – Dip for 1 min. 2. IPA – Dip for 15 sec 3. DI water Rinse (Check under Optical Microscope)
6.	E-beam Evaporation (Semicore) and Lift-off	<ol style="list-style-type: none"> 1. Pd/Au (20/60nm) metal stack 2. Lift-Off 	<ol style="list-style-type: none"> 1. Deposit Pd at 1.5Å^o/s and Au in three steps of 20 nm at 1.5Å^o/s. After each step allow sample cooling – 20 min 2. Dip in Remover PG – overnight if required. Heating Soln. to 60C will help.

Step VI: Removal of Al₂O₃ from S/D regions

Sequence	Process	Material	Process Conditions
1.	E-beam Resist Coating (Bi-layer)	1. P(MMA-MAA) 8.5 Co-Polymer diluted with 5.5% Ethyl Lactate (EL) 2. PMMA (A3)	1.a Use D09.20.60 (~ 250 nm) 1.b Bake: 150C – 3 min 1.c Cool: 1-2 min 2.a Use D09.40.45 (100-120nm) 2.b Bake 180C – 3min 2.c Cool: 1-2 min
2.	Semicore Thermal Evaporation	10 nm Au film evaporation (Thermal Evaporation Only)	Follow the Semicore/Kurt-Leskar User Manual
3.	E-beam Lithography	Follow the Procedure for using the e-beam tool (Align to 1 st layer) • Create Separate .IWFL files for small and big mesa.	Dose - 320 $\mu\text{C}/\text{cm}^2$ (small area) Resolution = 10 nm (Beam size = 15nm, current - select from spot table) Dose - 320 $\mu\text{C}/\text{cm}^2$ (big area) Resolution = 150 nm (Beam size = 180nm, current - select from spot table) Beam diameter should be 20% higher than resolution High Tension = 100kV
4.	Wet Etch Top Au Layer	Transcene Au Etchant - TFA	a. Dip for 30 sec b. Rinse with DI Water and dry

			with N ₂ gun
5.	Develop E-beam Resist	Develop the PMMA/MMA Bi-layer Resist	1. 1:1 MIBK: IPA – Dip for 1 min. 2. IPA – Dip for 15 sec 3. DI water Rinse (Check under Optical Microscope)
6.	Al ₂ O ₃ etching	Reactive Ion Etching Cl ₂ /Ar based gas chemistry	Pressure - 5mTorr, Gas flow – 10/40 sccm Cl ₂ /Ar, RF1-75W and RF2-500W, Room Temp., 30sec timed etch @ 3A°/sec (Versalock tool is used)
7.	Strip resist	Bilayer resist removal	Dip in Remover PG – overnight if required. Heating Soln. to 60C will help.

Step VII: Drain metal patterning

Sequence	Process	Material	Process Conditions
1.	E-beam Resist Coating (Bi-layer)	1. P(MMA-MAA) 8.5 Co-Polymer diluted with 5.5% Ethyl Lactate (EL) 2. PMMA (A3)	1.a Use D09.20.60 (~ 250 nm) 1.b Bake: 150C – 3 min 1.c Cool: 1-2 min 2.a Use D09.40.45 (100-120nm) 2.b Bake 180C – 3min 2.c Cool: 1-2 min
2.	Semicore Thermal Evaporation	10 nm Au film evaporation (Thermal Evaporation Only)	Follow the Semicore/Kurt-Leskar User Manual
3.	E-beam Lithography	Follow the Procedure for using the e-beam tool (Align to 1 st layer) • Create Separate .IWFL files for fingers and pads.	Dose - 320 $\mu\text{C}/\text{cm}^2$ (Fingers) Resolution = 10 nm (Beam size = 15nm, current - select from spot table) Dose - 280 $\mu\text{C}/\text{cm}^2$ (Pads) Resolution = 150 nm (Beam size = 180nm, current - select from spot table) Beam diameter should be 20% higher than resolution High Tension = 100kV
4.	Wet Etch Top Au Layer	Transcene Au Etchant - TFA	a. Dip for 30 sec b. Rinse with DI Water and dry

			with N ₂ gun
5.	Develop E-beam Resist	Develop the PMMA/MMA Bi-layer Resist	1. 1:1 MIBK: IPA – Dip for 1 min. 2. IPA – Dip for 15 sec 3. DI water Rinse (Check under Optical Microscope)
6.	Oxygen Discum	1.Oxygen Plasma RIE to remove remnant resist scum 2.Post RIE native oxide removal	1. Etch time: 20s, O ₂ – 45 sccm, Pressure- 100mTorr, Power – 100W (Plasma-Therm) 2. (1:50) HCl : DI water dip – 15 sec 3.Rinse in DI Water (Immediately Load Sample in Semicore for Metal Dep.)
7.	E-beam Evaporation (Semicore) and Lift-off	1.Ti/Pd/Au (20/20/60nm) metal stack 2. Lift-Off	1. Deposit Ti and Pd at 1.5A° /s and Au in three steps of 20 nm at 1.5A°/s. After each step allow sample cooling – 20 min 2. Dip in Remover PG – overnight if required. Heating Soln. to 60C might help.

Step VIII: Device isolation

Sequence	Process	Material	Process Conditions
1.	E-beam Resist Coating (Bi-layer)	1. P(MMA-MAA) 8.5 Co-Polymer diluted with 5.5% Ethyl Lactate (EL) 2. PMMA (A3)	1.a Use D09.20.60 (~ 250 nm) 1.b Bake: 150C – 3 min 1.c Cool: 1-2 min 2.a Use D09.40.45 (100-120nm) 2.b Bake 180C – 3min 2.c Cool: 1-2 min
2.	Semicore Thermal Evaporation	10 nm Au film evaporation (Thermal Evaporation Only)	Follow the Semicore/Kurt-Leskar User Manual
3.	E-beam Lithography	Follow the Procedure for using the e-beam tool (Align to 1 st layer) • Create Separate .IWFL files for small and big mesa.	Dose - 320 $\mu\text{C}/\text{cm}^2$ (small area) Resolution = 10 nm (Beam size = 15nm, current - select from spot table) Dose - 320 $\mu\text{C}/\text{cm}^2$ (big area) Resolution = 150 nm (Beam size = 180nm, current - select from spot table) Beam diameter should be 20% higher than resolution High Tension = 100kV
4.	Wet Etch Top Au Layer	Transcene Au Etchant - TFA	a. Dip for 30 sec b. Rinse with DI Water and dry

			with N ₂ gun
5.	Develop E-beam Resist	Develop the PMMA/MMA Bi-layer Resist	1. 1:1 MIBK: IPA – Dip for 1 min. 2. IPA – Dip for 15 sec 3. DI water Rinse (Check under Optical Microscope)
6.	Isolation etch	Reactive Ion Etching to remove the top GaAs _{0.5} Sb _{0.5} layer followed by citric acid etch to remove In _{0.53} Ga _{0.47} As all the way down to InP.	1. RIE: Pressure - 2mTorr, Gas flow – 15/60 sccm BCl ₃ /Ar, RF1-50W and RF2-75W, Room Temp., 4.5min timed etch @ 20nm/min (Versalock tool is used) 2. Wet Etch: Citric acid based wet etch chemistry (20:1) – 8 min
7.	Strip resist	Bilayer resist removal	Dip in Remover PG – overnight if required. Heating Soln. to 60C will help.

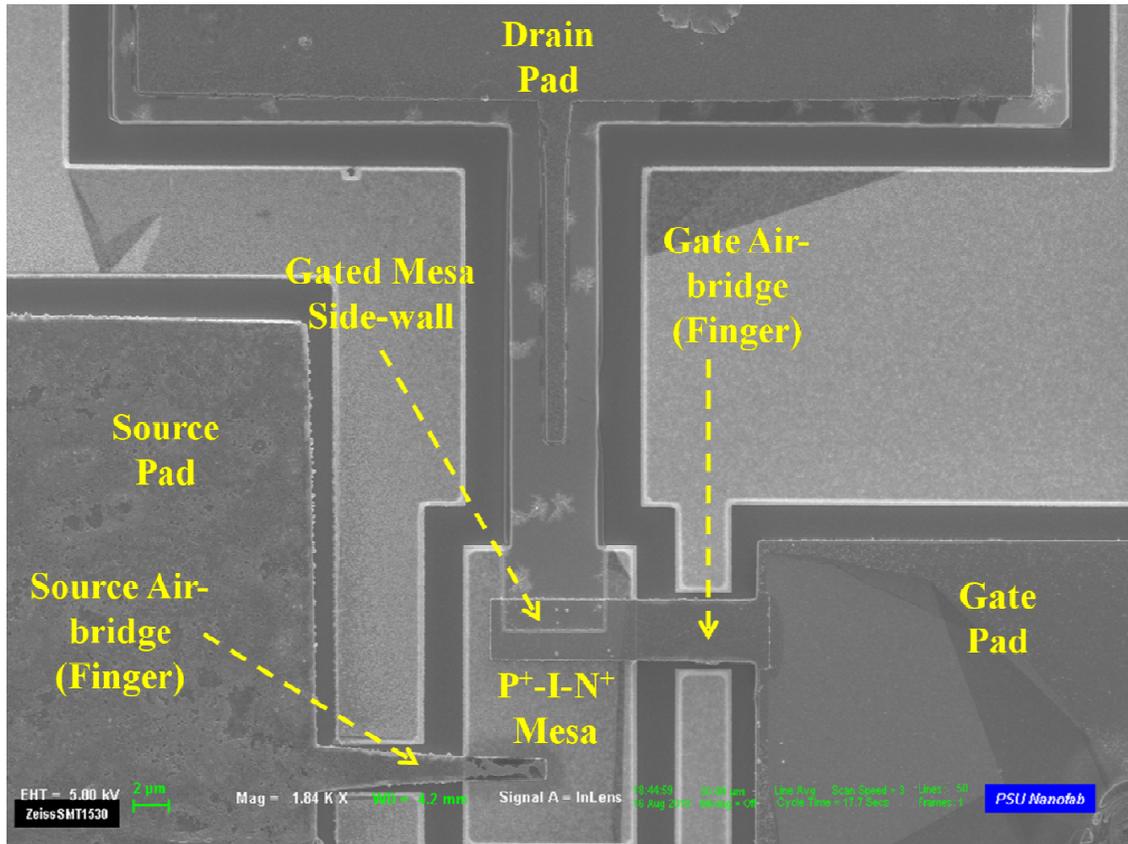
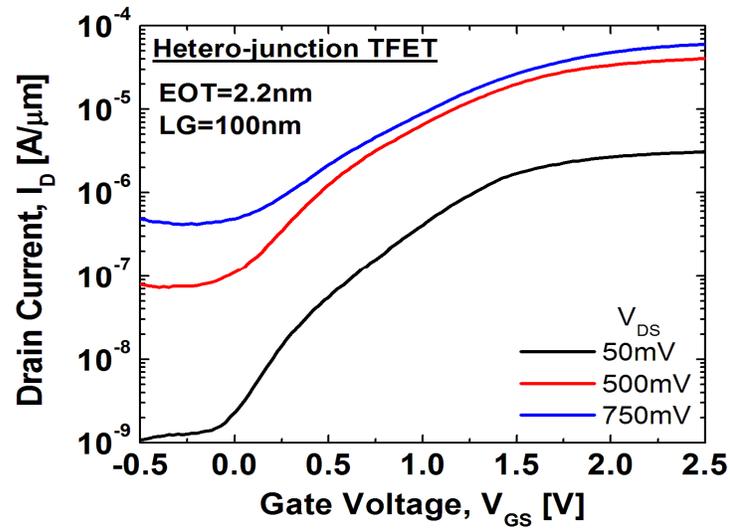
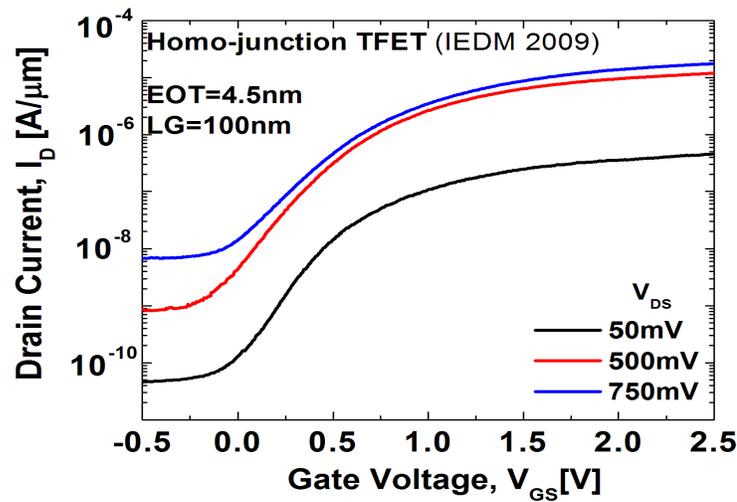


Figure 4-16. Scanning electron microscope image (SEM) of the fabricated hetero-junction TFET.

4.2.2 Electrical characterization of hetero-junction TFET

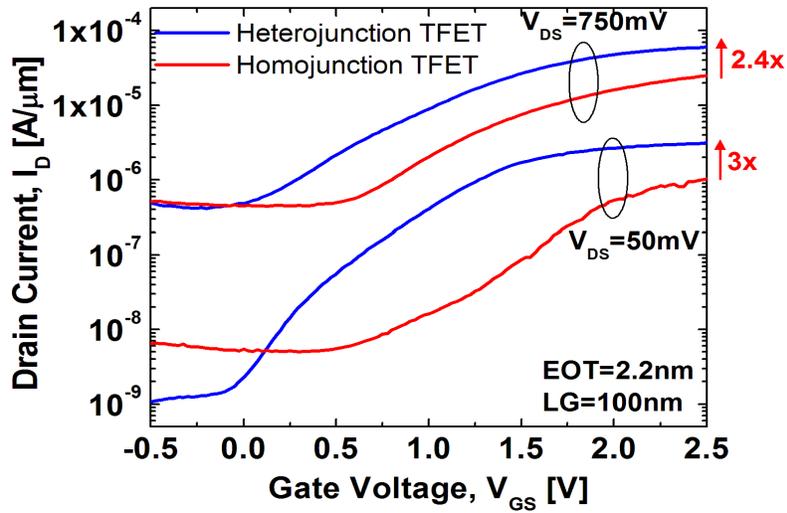


(a)

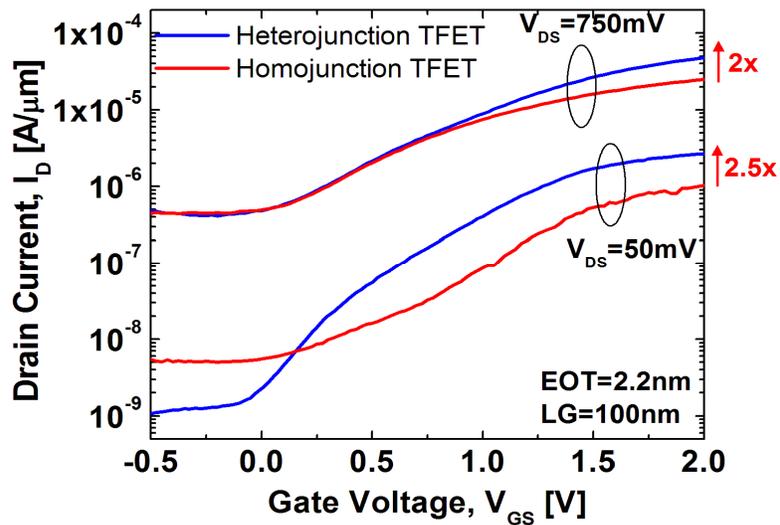


(b)

Figure 4-17. (a) Measured transfer characteristics of fabricated hetero-junction TFET at room temperature. No annealing has been done (b) Measured transfer characteristics of homo-junction InGaAs TFET at room temperature (from section 4.1)



(a)



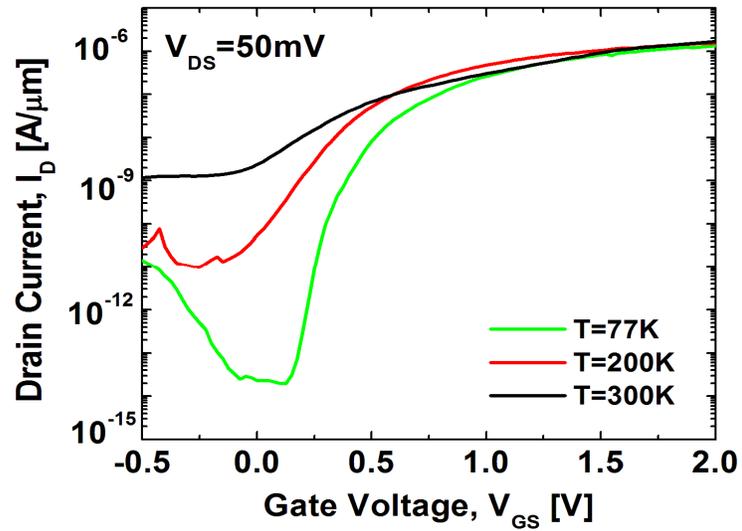
(b)

Figure 4-18. (a) Measured transfer characteristics of fabricated hetero-junction TFET is compared to homo-junction TFET. Both have an EOT=2.2nm No annealing has been done. (b) Measured transfer characteristics of homo and hetero-junction TFET is compared after work-function shift. This shows that the I_{ON} benefit is primarily arising from reduced tunneling barrier width in hetero-junction TFET.

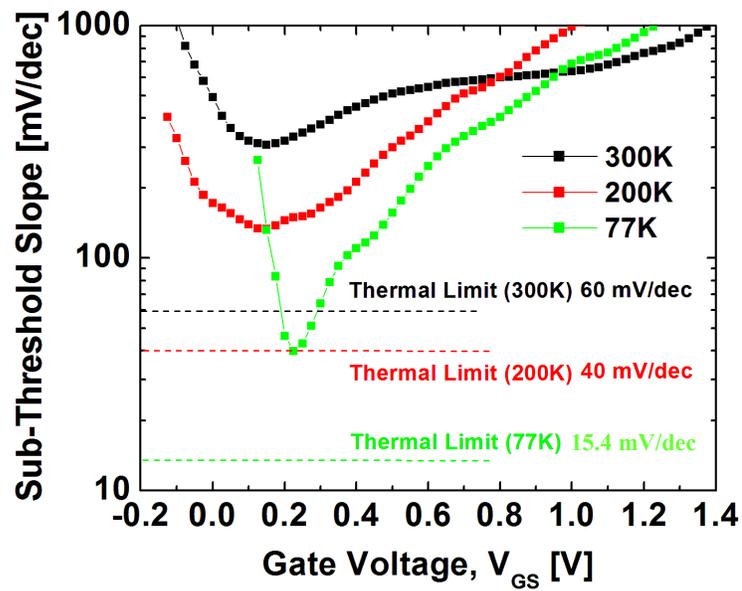
Again it is evident from figure 4-17(a) that the sub-threshold slope in hetero-junction TFET is significantly higher than 60mV/dec, degradation arising from trap assisted tunneling. We will discuss more about the degradation of sub-threshold slope when we study the temperature dependent characteristics in figure 4-19.

The drive current (I_{ON}) in this device is 60 $\mu\text{A}/\mu\text{m}$, 3X higher than the homo-junction TFET fabricated earlier with $EOT=4.5\text{nm}$. Figure 4-18 compares the transfer characteristics of homo and hetero-junction TFET with the same $EOT=2.2\text{nm}$. Fig 4.18(a) shows an I_{ON} enhancement of 2.5-3X (at $V_{DS}=0.75\text{V}$ and 0.05V respectively) for the hetero-junction case. After a careful look it seems as if the I_{ON} benefit in hetero TFET can be annulled with a work-function shift, even though the same gate metal (Pd/Au) is used for both the hetero and homo-junction TFET. Fig 4.18(b) compares the homo and hetero-junction TFET characteristics after a work-function shift, but even in this case hetero-junction TFET shows an I_{ON} enhancement of 2-2.5X over the homo-junction case.

Figure 4-19(a) plots the transfer characteristics of the hetero-junction TFET as a function of temperature. At low temperatures the mid-gap traps do not participate in the tunneling process resulting in a significant improvement in sub-threshold slope (figure 4-19(b)). In order to suppress the participation of slow mid-gap traps at room temperature pulsed I-V measurements can be done. This will be discussed in greater detail in chapter 5 of this dissertation.



(a)



(b)

Figure 4-19. (a) Measured transfer characteristics of fabricated hetero-junction TFET at three different temperatures (b) Point sub-threshold slope of fabricated hetero-junction TFET as a function of gate voltage for different temperatures ($V_{DS}=50$ mV). The minimum value is around 40 mV/dec at 77K.

Chapter 5

Conclusion and Future Work

The main goal of this research has been to design and fabricate the next electronic switch for future ultra-low power and high performance logic applications. In this regard, the concept of band-to-band tunneling field effect transistor (TFET) is introduced in chapter 1. In chapter 2, the material selection strategy for TFET fabrication is presented. Further, it is shown that TFET has the unique property of unidirectional (asymmetric) conduction in its output characteristics, unlike MOSFET which shows bidirectional (symmetric) conduction. This causes conventional 6T SRAM design with TFET to suffer from poor read and write noise margin. 7T SRAM designs have been proposed earlier (at the expense of higher area) to circumvent this issue of unidirectional conduction. In this work, a novel 6T SRAM design is proposed with stable read and write margin down to 0.3V. In chapter 3, the large signal digital switching behavior of TFET is studied in great detail. It is clearly shown that TFET inherently suffers from enhanced miller capacitance compared to MOSFET. This along with low I_{ON} in large band-gap materials (for e.g. silicon) adversely affects TFETs switching performance. It was clearly shown that in order to improve TFET performance (delay – CV/I), low band-gap materials (to achieve high I_{ON}) with low density of states (to limit miller capacitance) will have to be used.

In Chapter 4, the fabrication of homo-junction TFET along with its electrical characteristics is explained in great detail. From temperature dependent electrical characterization four uniquely different transport mechanisms were identified, giving key insight into TFETs operating principle. This study also led to the identification of three different knobs that can be used to improve the device performance. The three knobs are (i) The $p^+ - i - n^+$ mesa area can be

reduced to decrease the leakage floor (I_{OFF}) (ii) semiconductor-dielectric interface states (primarily mid-gap) need to be reduced/suppressed to improve the sub-threshold slope (by suppressing tunneling and subsequent thermal emission from mid-gap traps) in the transfer characteristics. Novel surface passivation schemes need to be identified. Pulsed IV measurements can also be used to bypass the contribution from these slow and dominant mid-gap traps, thus providing a means to experimentally observe sub-60 mV/dec of sub-threshold slope (at room temperature) in these devices. We will have more to discuss on pulsed IV measurement in the next section 5.1 (iii) The drive current (I_{ON}) can be increased by using a hetero-junction design, especially a staggered or a broken gap at the source-channel junction. A staggered band-gap TFET with EOT=2.2 nm is also fabricated. This device has the highest ON current ($60 \mu\text{A}/\mu\text{m}$ at $V_{DS}=0.75\text{V}$) among all the devices reported till date. In future, moving towards a broken-gap system and even smaller EOT should help in boosting the ON current beyond the $100 \mu\text{A}/\mu\text{m}$ range ($V_{DD}=0.5\text{V}$). The source-channel junction in a TFET involves a very field region, generating a lot of hot carriers in the process. The possibility of using these hot carriers in boosting the TFET ON current will be explored in section 5.2. Section 5.3 discusses an important issue with p-channel TFET design.

5.1 Pulsed I-V measurement

Figure 5-1 shows the admittance measurement (capacitance-voltage (CV) and conductance measurement) of $10^{17} /\text{cm}^3$ n-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ semiconductor and Al_2O_3 (EOT=2.2nm) dielectric interface. Both the capacitance and conductance measurement (Figure 5-1(a) and 5-1(b)) indicates the presence of large interface density of states near the middle of the band-gap. This is also confirmed from the extracted interface density of state [53] in figure 5-1(c). The extracted time constant is shown in figure 5-1(d). The trapping and de-trapping time

constant for a mid-gap trap is greater than $10\mu\text{s}$ while it is $1\mu\text{s}$ and $0.1\mu\text{s}$ for traps close to the conduction band for PE-ALD (Plasma Enhanced ALD) and ALD samples respectively.

The interface density of states for the fabricated TFET is still quite high (figure 5-1(c)) and this prevents experimental observation of sub-60mV/dec (at room temperature) of sub-threshold swing in these devices. Fortunately, all these interface traps have an associated time constant. By sweeping the gate voltage at a rate faster than the time response of these trap states, their contribution to the sub-threshold slope degradation can be suppressed. Pulsed IV measurements are ideally suited for such measurements. Figure 5-2 shows the experimental set-up for pulsed IV measurement.

Pulsed IV measurements have been widely used for studying the stress induced threshold voltage shift in MOSFETs, notably from the fast trapping/de-trapping states at the oxide-semiconductor interface and within the oxide during positive/negative bias temperature instability [70][71][72]. The oscilloscope measures the drain current and the input voltage (pulse) applied to the gate of the transistor. By virtual short circuit property of the op-amp (the voltage of two input terminals are forced to be equal), the drain voltage of the transistor is fixed at supplied by the voltage source, so no charging and discharging current flows through parasitic capacitances, this prevents the distortion of the measured drain current. A high-speed op-amp (for e.g. OPA655) with unity gain bandwidth can be used to achieve fast measurement. As most samples are measured in probe station environment, the op-amp circuit (enclosed by the dashed line in figure 5-2) is mounted immediately above the probe holder. Probe holders are modified and wire connection to the transistor source and drain terminal is made less than 10 cm to minimize parasitics.

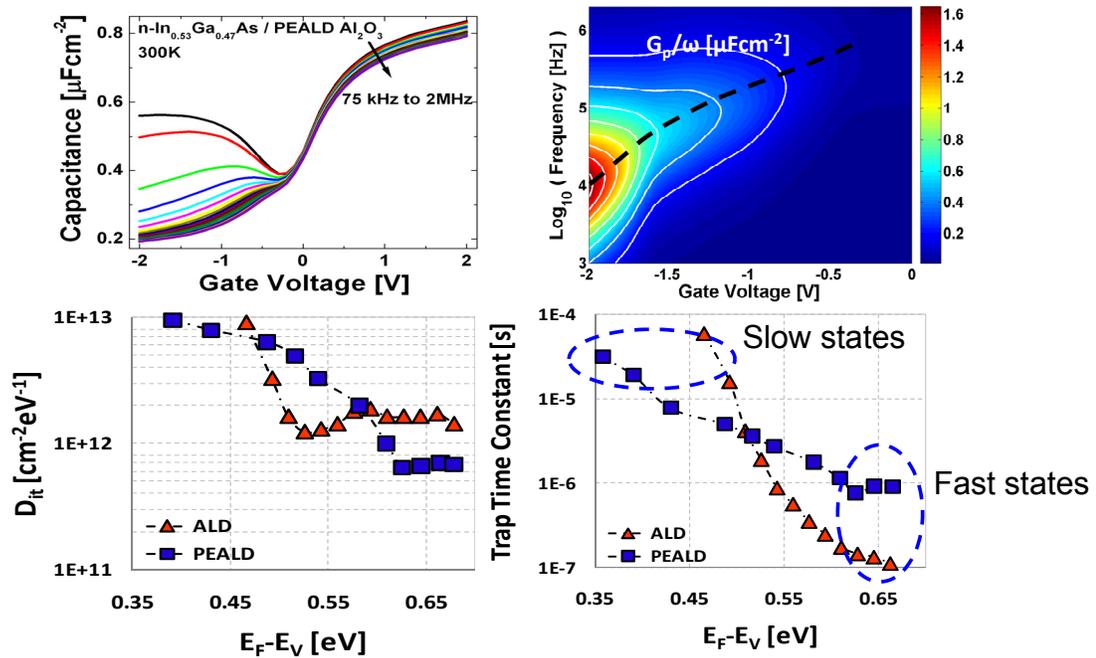


Figure 5-1. Admittance measurement of $10^{17}/\text{cm}^3$ n-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ semiconductor and Al_2O_3 (EOT=2.2nm) dielectric interface indicates the presence of slow and fast states. (a) Capacitance-Voltage (CV) measurement of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}-\text{Al}_2\text{O}_3$ dielectric interface (b) Conductance contour as a function of gate voltage and frequency. High conductance value at low frequency and low gate voltage indicates the presence of large interface density of states near the middle of the band-gap of the semiconductor (c) extracted semiconductor-dielectric interface density of states (d) Time constant of interface states as a function of its position in the band-gap of the semiconductor. (ALD-Atomic Layer Deposition, PE-ALD – Plasma Enhanced ALD)

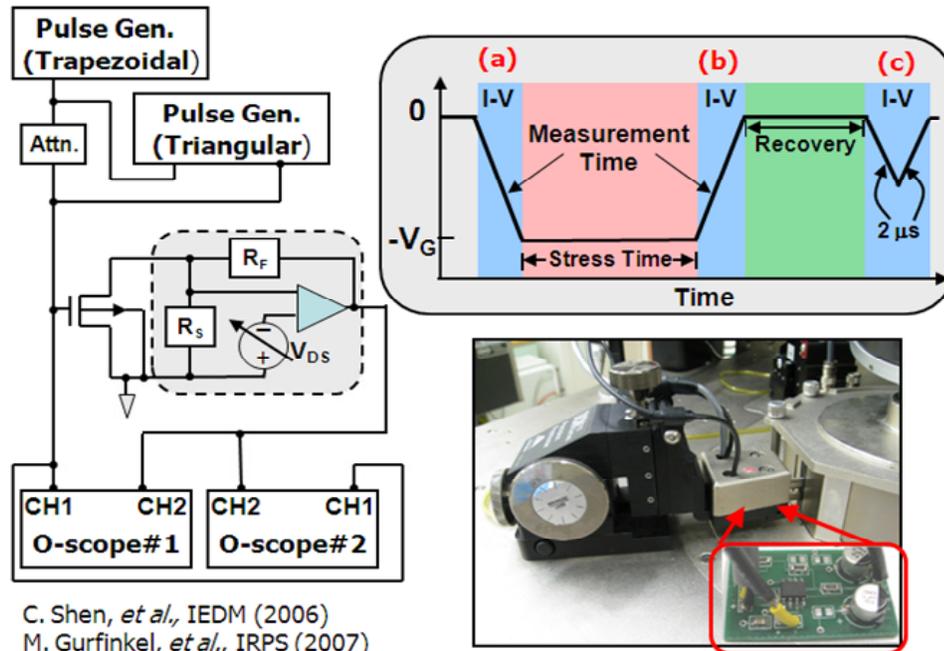


Figure 5-2. Ultra-fast I_D - V_{GS} measurement set-up. This particular set-up has been frequently used to study negative bias temperature instability (NBTI) in MOSFETs.

5.2 Band-gap engineered hot carrier generation for boosting TFET ON current

In this section we present the results from a preliminary study on the strong non-equilibrium character of the tunnel injected carrier population in the channel of TFET through detailed energy balance (EB) simulations [35][73] and its implication on TFET device design. Figure 5-3 explains the motivation behind this study. We specifically show that: (i) A large and highly inhomogeneous electric field at the source side tunnel junction at high gate voltage results in a non-equilibrium distribution of injected carriers in the TFET channel (ii) A novel source side hetero-junction design can potentially enhance and sharpen the source side electric field amplitude and shape resulting in greater carrier heating and band-to-band tunneling (BTBT) currents even at moderate gate voltages (iii) The energy relaxation process of the injected carriers on both sides of the tunnel barrier are studied as a function of bias conditions and is a strong function of the 2-dimensional electric field profile in the TFET channel.

Figure 5-4 compares the carrier energy distribution for Si TFET and MOSFET under high gate and drain bias ($V_{GS}=V_{DS}=1V$). An average value of 0.3 ps and 0.25 ps is used for the electron and hole energy relaxation rates in silicon. Figure 5-4(a) and 5-4(b) show that in a n-type Si MOSFET the carriers (electrons, unipolar device) are gradually heated in the channel via the drift field and finally relax on entering the drain. In contrast, TFET (Figure 5-4(c) and 5-4(d)) is a bipolar device with a large electric field at the source end resulting in a heated distribution of BTBT induced electrons in the channel conduction band and holes in the p^+ source region valence band.

Figure 5-5 compares the $I_{DS}-V_{GS}$ ($V_{DS}=1V$) characteristics computed via drift diffusion (DD) and Energy Balance (EB) simulation. EB predicts a 6X higher ON current for TFET (fig 5-5(a)) compared to DD. Figure 5-5(b) shows a lower band-gap source ($p^+ Si_{0.7}Ge_{0.3}$) TFET design with p- Si channel and n+ drain having a 2 nm gate-source and gate-drain overlap regions (the

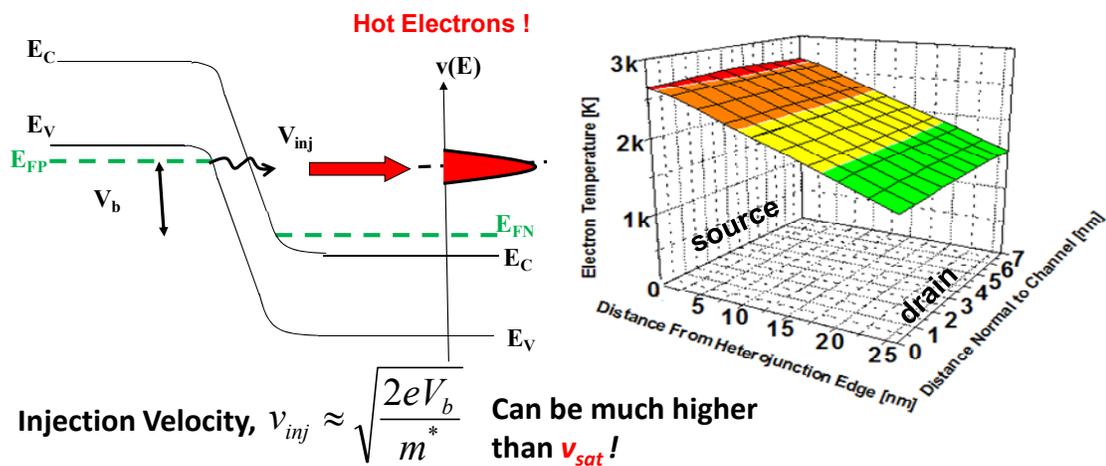


Figure 5-3. Band-to-band tunneling is a natural source of hot carriers. Carriers are injected by tunneling into a state of high kinetic energy where the potential energy V_b is converted into kinetic energy. This high kinetic energy results in higher injection velocity (v_{inj}) which can be much higher than the saturation velocity (v_{sat}). This high injection velocity is expected to boost the ON current in TFET. Can this source-side tunnel barrier be engineered to further enhance the injection velocity and hence the ON current in TFET ?

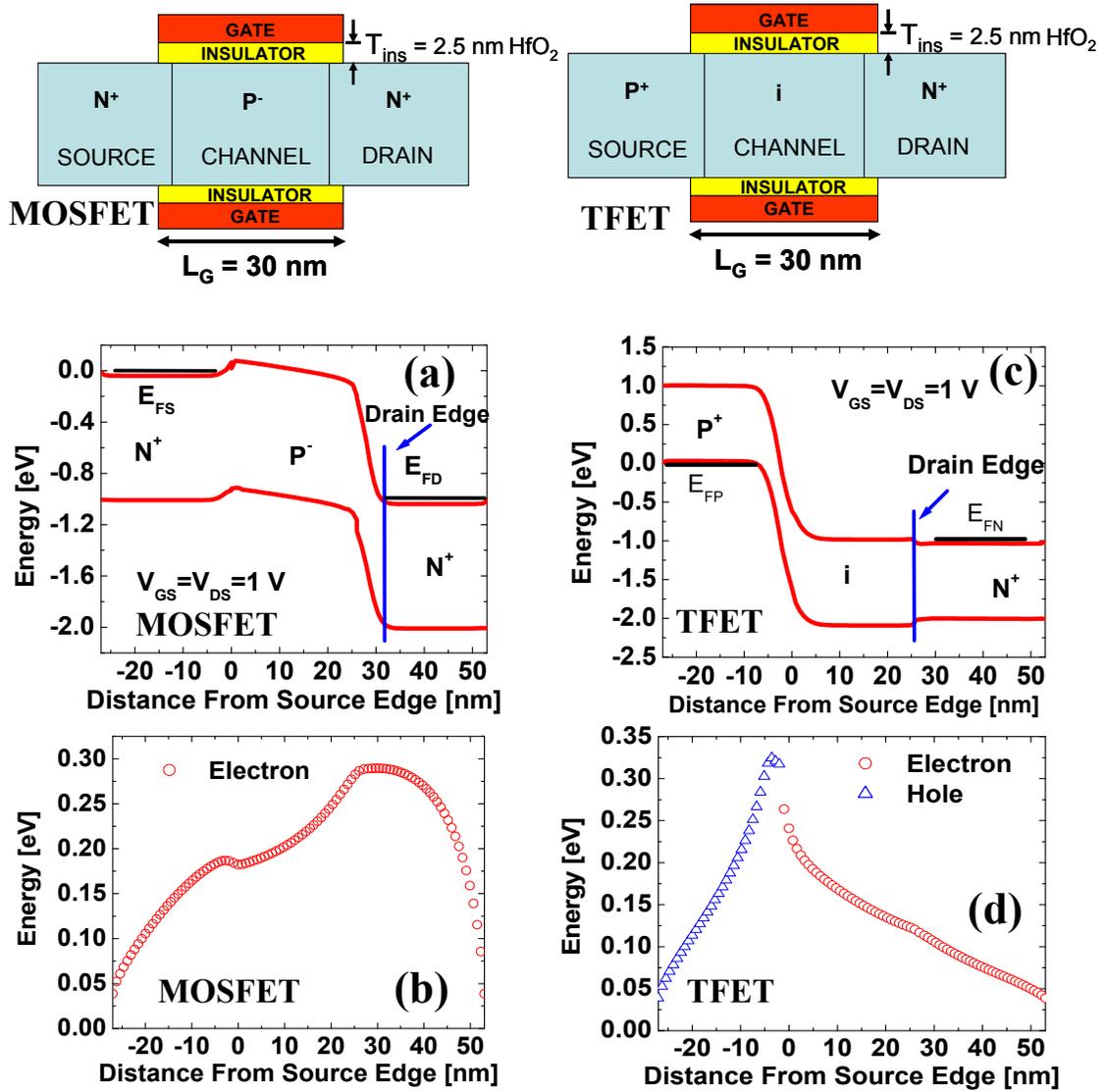


Figure 5-4. Simulated device schematic of a MOSFET and TFET (a) Si MOSFET band diagram under high gate and drain bias (b) Electron energy along the length of the device (c) Si TFET band diagram under high gate and drain bias (d) Electron and Hole energy along the length of the device.

SiGe source (SGS) design). Figure 5-5(b) compares the I_{DS} - V_{GS} characteristics obtained via DD and EB simulation, in this case EB predicts a 3.3X higher ON current. The carrier heating effects for SGS design begins at $V_{GS}=0.16$ V. In order to further reduce the characteristic gate bias for carrier heating a novel hetero-junction source design (Fig 5-5(c), Displaced SGS (DSGS)) is proposed, here the p+ doping is physically shifted from the hetero-junction edge by 2 nm. Figure 5-5(c) shows that the EB predicts a 3.2X higher ON current ($I_{ON} = 1.56$ mA/ μ m) compared to DD ($I_{ON} = 487$ μ A/ μ m) with the characteristic gate bias for carrier heating at $V_{GS}=0.08$ V. At $V_{GS}=0.16$ V, DSGS TFET design results in 10X improvement in ON current over SGS design due to enhanced carrier heating at lower gate biases. This is primarily due to the enhancement and sharpening of the electric field profile in the source side tunnel junction (figure 5-5(d)).

In conclusion, this study clearly elucidates the importance of non-equilibrium hot carrier transport in tunnel transistors through EB simulations and shows that unlike DD, a large and highly inhomogeneous electric field at the source tunnel junction leads to considerable carrier heating and non-equilibrium carrier distribution which results in enhanced band to band tunneling current for both low and high gate voltages. It is shown that novel hetero-junction source design like the DSGS TFET could be used to exploit this carrier heating effect and boost the ON-current of tunnel transistor. This work provides the incentive to study this hot carrier effect in greater detail and further explore novel device designs to realize the full potential of tunnel transistors.

Further, novel device structures have to be designed to experimentally study the distribution of hot carriers (velocity of carriers) arriving at the drain. Electron spectroscopic techniques can be used to analyze the energy distribution of ballistic electrons [74][75] arriving at the drain. A potential device structure for such a measurement is shown in figure 5-6. It consists of a zener tunnel junction as the generator of hot carriers. The barrier between the channel and drain is thick enough to serve as the electron spectrometer barrier. The injected hot-electron beam is energetic

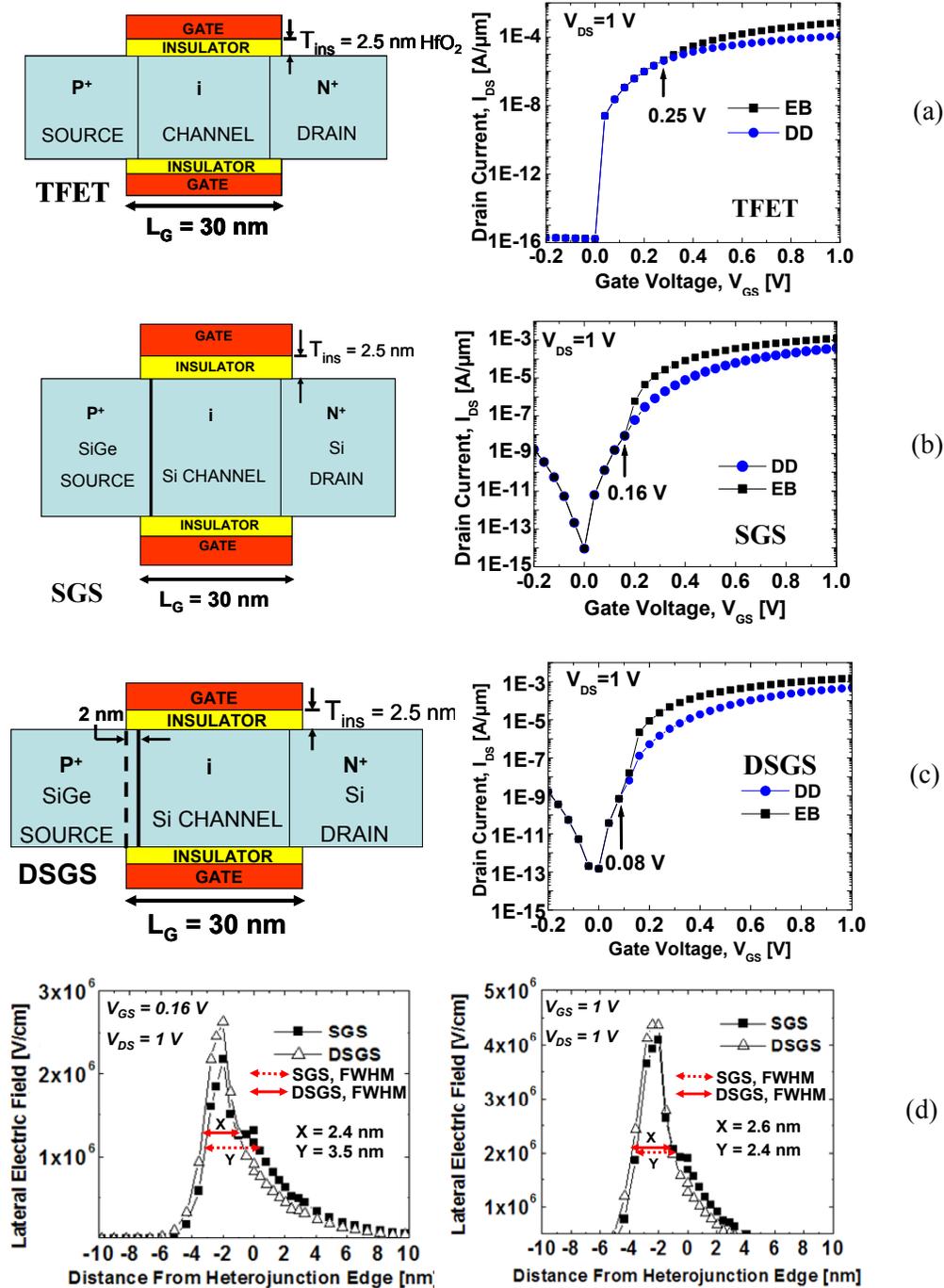


Figure 5-5. (a) Homo-junction TFET. $I_{DS}-V_{GS}$ with DD and EB simulation (b) Si_{0.7}Ge_{0.3} source (SGS) device schematic. SGS $I_{DS}-V_{GS}$ at $V_{DS}=1$ V for Energy Balance (EB) and Drift Diffusion (DD) simulation (c) Displaced Si_{0.7}Ge_{0.3} Source (DSGS) schematic wherein the doping edge is moved away from the hetero-junction edge by 2 nm. DSGS $I_{DS}-V_{GS}$ at $V_{DS}=1$ V for Energy Balance (EB) and Drift Diffusion (DD) simulation (d) Lateral Electric Field at the source side tunnel junction for low gate bias and high gate bias. FWHM (Full width half maximum) signifies the rapid change of the electric field profile at the tunnel junction.

enough to surmount the drain barrier almost independently of the drain voltage, resulting in a high differential output resistance. Reference [74] is an excellent review on such devices.

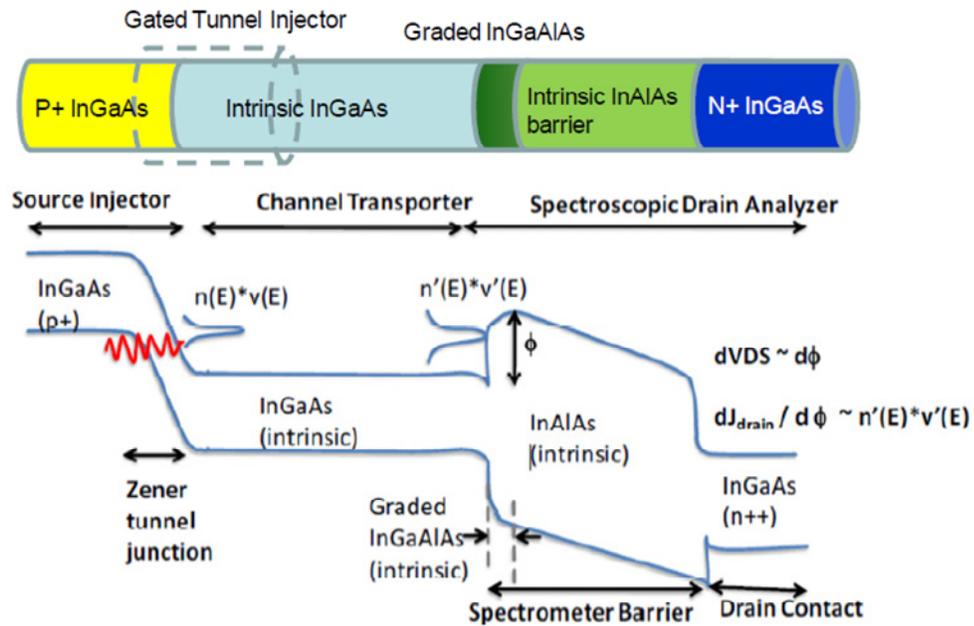


Figure 5-6. Design and band-diagram of a device to be used for analyzing the energy distribution of hot carriers arriving at the drain.

5.3 Challenges with complimentary p-channel TFET design [76][77]

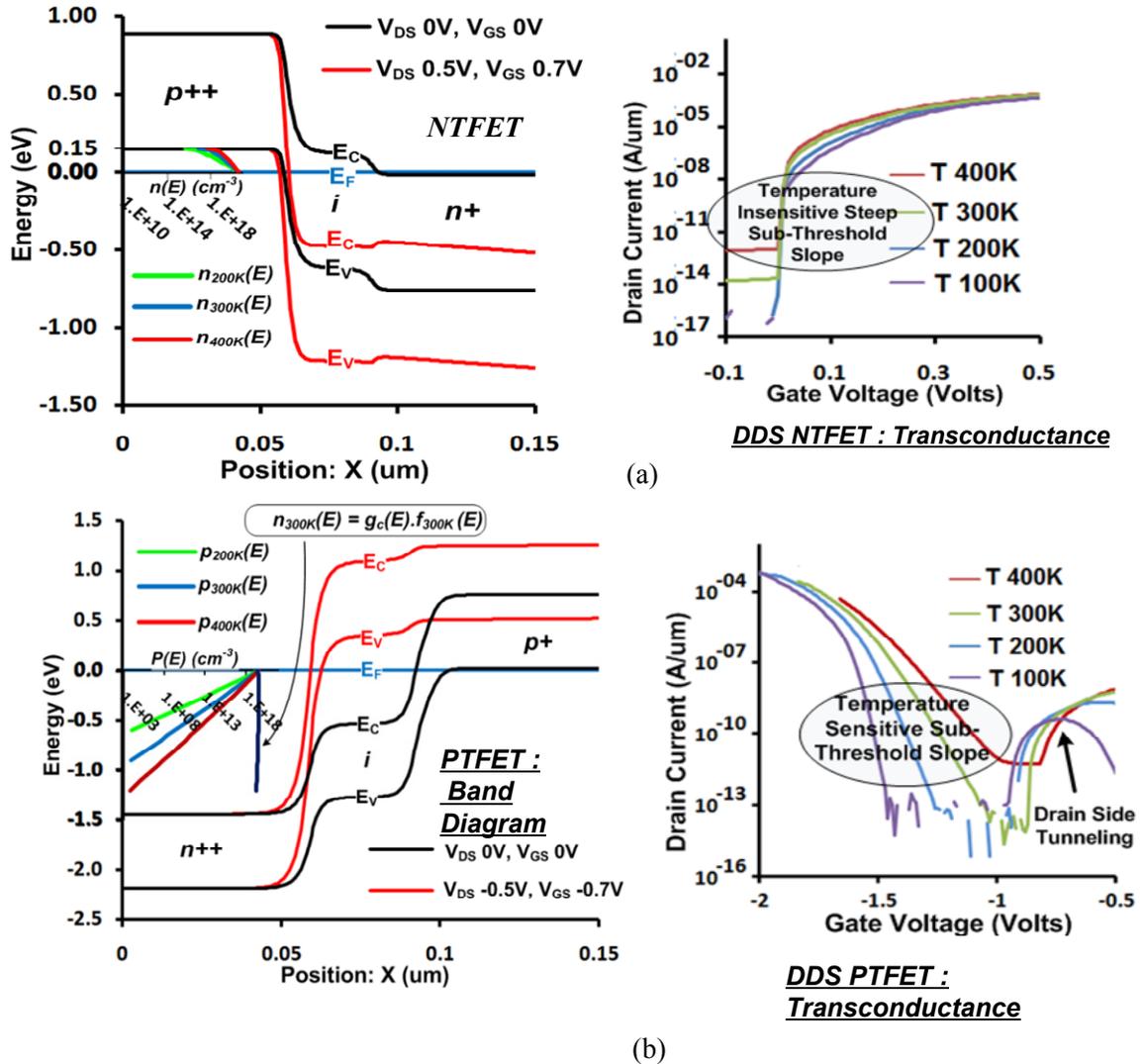


Figure 5-7. (a) $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ N-TFET band-diagram and transfer characteristics. In this case the source (P+ region) fermi level is very close to the valence band edge (due to high density of states for holes). This causes the high energy tail of the carrier distribution to be cut-off by the source band-gap. This results in the sub-threshold slope being fairly independent of temperature (b) In the P-channel case the Fermi level degeneracy in the n+ source region is quite high (Low density of states for electrons). The high energy tail limits the sub-threshold slope to 60mV/dec and gives rise to a strong temperature dependence similar to that of a MOSFET.

In this section we will briefly look at an important issue with p-channel devices. In $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ based p-channel devices due to the high degeneracy of the source (n^+ region) Fermi level the carriers in the high energy tail portion of the distribution gets uncovered and participates in the tunneling process giving rise to a strong temperature dependence in the sub-threshold slope, just like a MOSFET. This is schematically explained in figure 5-7.

In order to solve this problem a different material system will have to be used to suppress the fermi level movement deep into the bands. Figure 5-8 shows one such design with n^+ $\text{GaAs}_{0.1}\text{Sb}_{0.9}$ as the source. In this material the separation between the Γ (small density of states) and L (large density of states) valley is approximately 84 meV compared to 460 meV in $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$. This results in a significant population in the L-valley and thus prevents the fermi level from moving deep into the bands (higher energy). In figure 5-8 an additional δp^+ region is added to boost the ON current of p-channel TFET. In future, p-channel TFETs need to be fabricated with comparable performance to that of n-channel TFET.

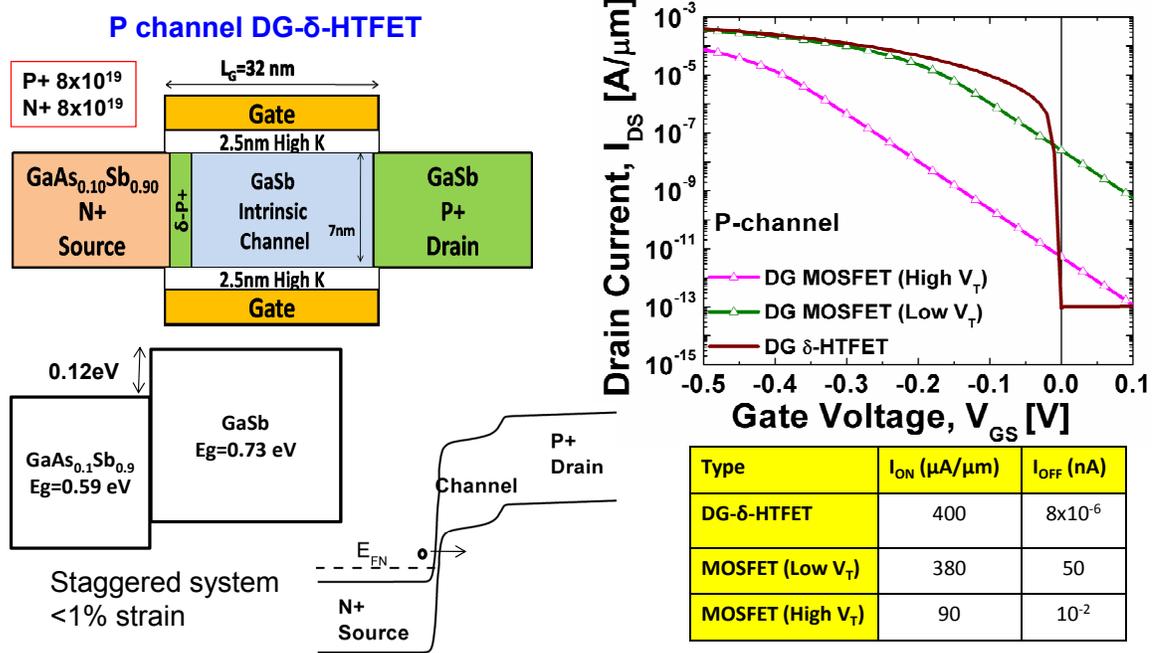


Figure 5-8. High performance p-channel TFET design. $\text{GaAs}_{0.1}\text{Sb}_{0.9}$ source with small Γ -L valley separation prevents fermi level movement deep into the bands. This along with a $\delta p+$ region next to the source-channel junction results in high ON current and sub-60mV/dec of sub-threshold slope.

Appendix

Tools Used for Device Fabrication



Laurell Resist Spin
Coater



GCA 8000 I-line
(Stepper) Lithography



Leica EBPG5-HR E-
Beam Lithography



Plasma-Therm 720 Reactive
Ion Etching (RIE)



Semicore E-beam/Thermal
Evaporator



Cambridge Savannah
200 Atomic Layer Deposition

Figure A-1. A partial list of tools used for device fabrication.

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PARTIAL PUBLICATION LIST

1. **S. Mookerjea** and S. Datta, "Comparative Study of Si, Ge and InAs Based Steep Subthreshold Slope Tunnel Transistors for 0.25V Supply Voltage Logic Applications," *66th Device Res. Conf.*, pp. 47-48, Jun. 2008. **(SELECTED FOR ORAL PRESENTATION)**
2. **S. Mookerjea**, R. Krishnan, A. Vallett, T. Mayer and S. Datta, "Inter-band Tunnel Transistor Architecture using Narrow Gap Semiconductors," *ECS Transactions*, vol. 19, no. 5, pp. 287-292, May 2009.
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6. **S. Mookerjea**, D. Mohata, R. Krishnan, J. Singh, A. Vallett, A. Ali, T. Mayer, V. Narayanan, D. Schlom, A. Liu and S. Datta, "Experimental Demonstration of 100nm Channel Length In_{0.53}Ga_{0.47}As-based Vertical Inter-band Tunnel Field Effect Transistors (TFETs) for Ultra Low-Power Logic and SRAM Applications," *IEDM Tech. Digest*, pp. 949-951, Dec. 2009. **(SELECTED FOR IEDM 2009 PRE-CONFERENCE PUBLICITY)**
7. J. Singh, R. Krishnan, **S. Mookerjea**, S. Datta, V. Narayanan, "A Novel Si TFET Based SRAM design for Ultra Low-Power 0.3V V_{DD} Applications," *15th Asia Pacific Design Automation Conference (ASP-DAC 2010)*. **(PATENT APPLICATION PENDING)**
8. V. Saripalli, D. K. Mohata, **S. Mookerjea**, S. Datta and V. Narayanan, "Low-Power Load-less 4T SRAM cell based on Degenerately Doped Source (DDS) In_{0.53}Ga_{0.47}As Tunnel FETs," *68th Device Res. Conf.*, pp. 101-102, Jun. 2010. **(PATENT APPLICATION PENDING)**
9. **S. Mookerjea**, D. Mohata, T. Mayer, V. Narayanan and S. Datta, "Temperature-Dependent I-V Characteristics of a Vertical In_{0.53}Ga_{0.47}As Tunnel FET (TFET)," *IEEE Electron Device Lett.*, vol. 31, no. 6, pp. 564-566, Jun. 2010.